VSC7998
Datasheet

SONET/SDH 10.7 Gbps Transimpedance Amplifier

Features

- Adjustable output offset
- 1.4 kΩ differential transimpedance
- –5.2 V power supply
- 2.0 mA peak-to-peak (p-p) maximum input current
- AC-coupled or DC-coupled outputs
- Known good die
- Low power: 390 mW typical
- Input sensitivity: –18.5 dBm typical

Applications

- 10.7 Gbps SONET OC-192/SDH STM-64 systems
- 10.3 Gbps Ethernet applications
- Small form factor transceivers
- Fiber optic transponders

General Description

The VSC7998 device is a 10.7 Gbps high-performance transmipedance amplifier (TIA) designed for use in optical communication networks, such as SONET OC-192, SDH, STM-64 installations. The device is intended for use with a PIN photodetector and is capable of amplifying input currents of up to 2.0 mA with low duty-cycle distortion. The outputs limit to a typical differential value of 1000 mV, p-p, for input signals greater than 1 mA, p-p. To provide flexibility in setting the decision threshold of the limiting amplifier, the VSC7998 uses output offset adjustment.

Block Diagram

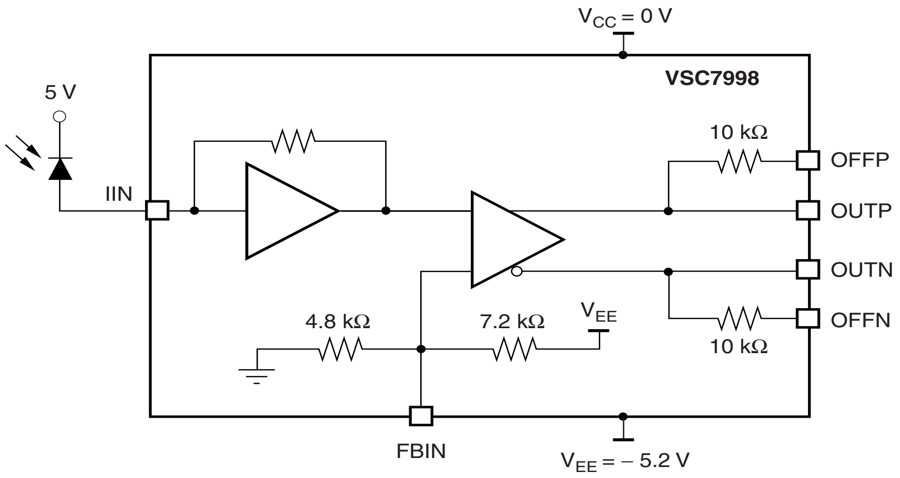


Figure 1. Block Diagram

Functional Descriptions

The VSC7989 amplifier consists of a transimpedance stage and a single-to-differential output stage with a gain of 11.4 dB (see Figure 1). An external photodetector is connected to the IIN input. Pins OUTP and OUTN are the complementary data outputs. Pins FBIN, OFFP, and OFFN are used for output offset control. The data output OUTP goes HIGH (OUTN goes LOW) when light is applied to the external PIN photodetector. The output is linear for inputs up to 1 mA, p-p.

For higher inputs, the output limits at 1000 mV, p-p differential (typical), increasing the dynamic range of the system by reducing the possibility of exceeding the input voltage range of the limiting amplifier or clock and data recovery circuit.

Figure 2 shows the relationship between input current and output voltage.

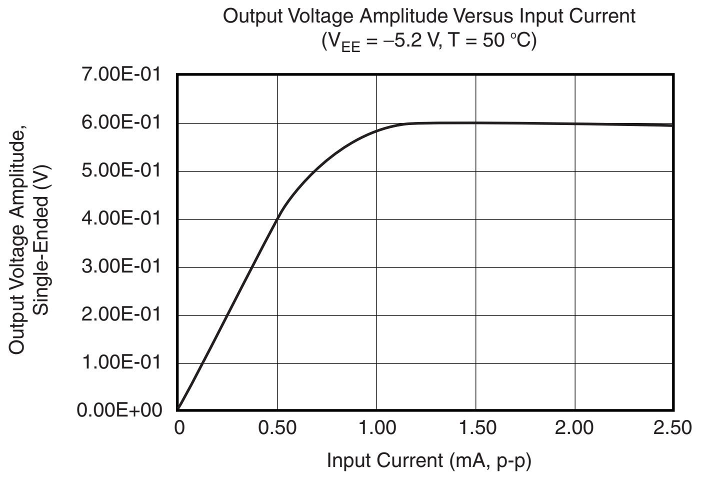


Figure 2. Output Voltage vs. Input Current

Power Supply

The VSC7998 requires –5.2 V for operation. Connect all V_{EE} pins to –5.2 V and all V_{CC} pins to ground.

Data Outputs

The VSC7998 can be AC-coupled or DC-coupled. For AC-coupled designs, the value of the capacitor determines the low-frequency cutoff for the system.

Output Offset Control

The VSC7998 provides flexibility in setting the decision threshold of the limiting amplifier or the clock and data recovery circuit by providing DC output offset control of OUTP and OUTN. The OFFP and OFFN outputs, connected to ground through 100 nF capacitors, provide the user with the DC component of the OUTP and OUTN data outputs. An external circuit can be used to sense the OFFP and OFFN outputs and then generate the appropriate DC voltage at the FBIN input to set the DC offset between OUTP and OUTN.

Figure 3 illustrates the relationship between the DC offset of OUTP, OUTN, and $F_{BIN.}$ Figure 4 shows a typical application for the VSC7998 used in conjunction with a VSC8174 device.

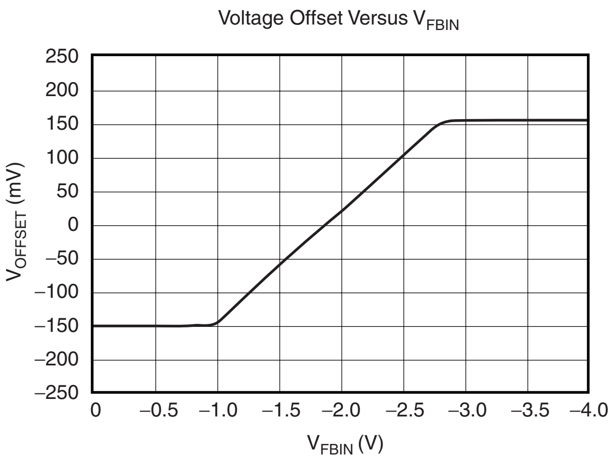


Figure 3. V_{OFFSET} vs. V_{FBIN}

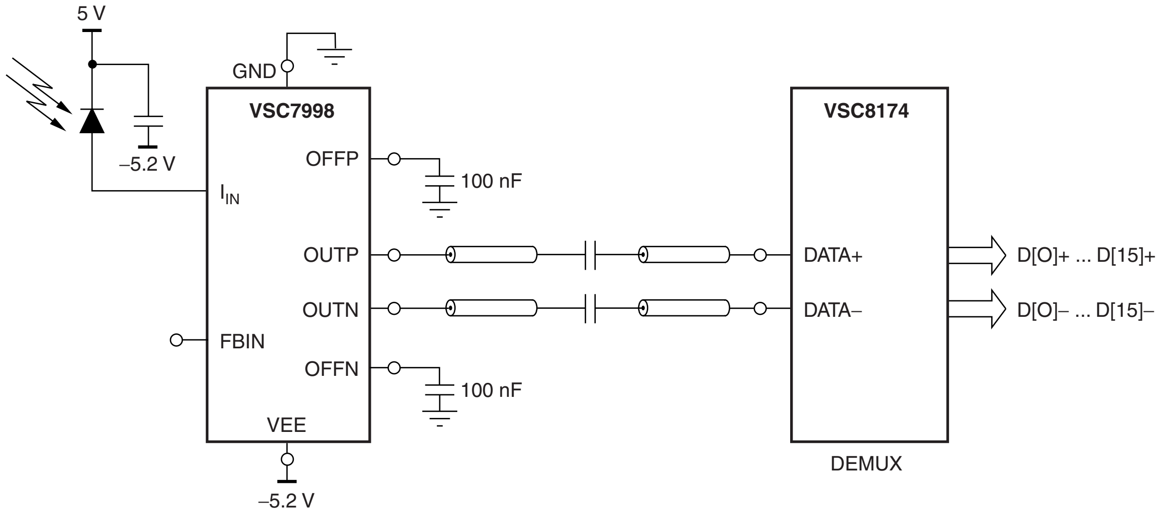


Figure 4. Typical Application for the VSC7998

Electrical Specifications

This section contains the DC characteristics, AC characteristics, operating conditions, and stress ratings.

DC Characteristics

Table 1 contains the specifications for the DC characteristics. Table 2 provides the output offset adjustment.

Table 1. DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{EE}	Power supply voltage	–4.9	–5.2	–5.5	V	
I_{CC}	Power supply current		75	90	mA	
V_{INBIAS}	Input bias voltage		V_{EE} + 1.7		V	
V_{OUT_CM}	Common-mode output voltage	GND – 0.7	GND – 0.45	GND – 0.2		50 Ω termination to ground
V_{OUT_CM}	Common-mode output voltage	GND – 1.4	GND – 0.90	GND – 0.4		100 Ω line-to-line termination

Table 2. Output Offset Adjustment

Symbol	Parameter	Minimum	Typical	Unit	Condition
V_{OFFSET}	$V_{OUTP} - V_{OUTN}$, $V_{OFFP} - V_{OFFN}$	150		mV	DC voltage
V_{OFFSET_NEG}	$V_{OUTP} - V_{OUTN}$, $V_{OFFN} - V_{OFFP}$	150		mV	DC voltage
V_{FBIN_MIN}	V_{FBIN} for maximum positive offset		–3	V	V_{OFFSET} = 150 mV
V_{FBIN_NOM}	V_{FBIN} for zero offset		–2.0	V	V_{OFFSET} = 0 mV
V_{FBIN_MAX}	V_{FBIN} for maximum negative offset		–1	V	V_{OFFSET} = –150 mV
R_{FBIN}	F_{BIN} input impedance		2.88	kΩ	

AC Characteristics

This section contains the specifications for the AC characteristics. Table 3 lists the specifications that are production-tested in a 50 Ω environment. These specifications are guaranteed over the recommended operating conditions listed in Table 5. Certain parameters, such as bandwidth, are expected to improve when properly designed into the optical environment. For expected performance in an optical environment, see Table 4.

Table 3. AC Characteristics for Die in Probe Environment

Symbol	Parameter	Minimum	Typical(1)	Maximum	Unit	Condition
Z_{T_SE}	AC single-ended transimpedance gain(2)	550	720	1250	Ω	50 Ω load probe environment
Z_{T_DIFF}	AC differential transimpedance gain(2)	1100	1440	2500	Ω	50 Ω load probe environment
BW_{TZ}	Transimpedance upper –3 dB bandwidth	7.5	8.0	10	GHz	50 Ω probe card at 25 °C
f_L	Lower –3 dB cutoff frequency		25	40	kHz	With 0.1 µF AC-coupling capacitor at output
I_{PK_MAX}	Maximum peak input current	2.0	2.6		mA	r_e = infinity
I_{ND}	Input noise current	1.0	1.5	2.2	µA	100 kHz to 10 GHz at 25 °C
V_{OD}	Maximum differential output swing		1000	1400	mV	AC-coupled output, terminated to 50 Ω on each side, probe environment
V_{OS}	Maximum single-ended output swing		500	700	mV	AC-coupled output, terminated to 50 Ω on each side, probe environment
J_T	Peak-to-peak jitter		0.12		UI	$PRBS^{31}$, 10.7 Gbps, 3 mA input current
R_{OUT}	Output impedance	42	50	58	Ω	
S_{22}	Output return loss			–10	dB	50 Ω load probe environment

1. *Typical conditions of 25 °C at backside and 3.3 V supply.*
2. *The transimpedance gain is defined as* $Z_T = 50 \cdot S_{21} / (1 - S_{11})$ *at 500 MHz.*

The specifications listed in Table 4 are based on a photodetector with the following properties: photodetector capacitance (C_{PD}) = 0.2 pF, photodetector bond wire inductance (L_{IN}) = 0.7 nH, photodetector small signal bandwidth (BW_{PD}) = 15 GHz referenced to 500 MHz. Effective bond wire inductance between detector cathode and decoupling capacitor (or V_{PD}) is 400 pH.

Table 4. AC Characteristics for an Optical Environment

Symbol	Parameter	Typical[(1)]	Unit	Condition
Z_{T_SE}	AC single-ended transimpedance gain(2)	720	Ω	50 Ω load, 5 MHz
Z_{T_DIFF}	AC differential transimpedance gain(2)	1440	Ω	50 Ω load, 5 MHz
$BW_{OPTICAL}$	Minimum optical upper –3 dB bandwidth	8.5	GHz	Measured on optical characterization board at 25 °C
$P_{OVERLOAD}$	Maximum peak input optical power	1	dBm	Measured p-p
S_{AVG}	Average optical sensitivity	–19	dBm	R = 0.9 A/W, r_e = 9 dB, BER $1E^{12}$
V_{OD}	Maximum differential output swing	1000	mV	Measured p-p, AC-coupled output, terminated to 50 Ω on each side
V_{OS}	Maximum single-ended output swing	500	mV	Measured p-p, AC-coupled output, terminated to 50 Ω on each side
Peak	Peaking	1.2	dB	1 GHz to $f_{–3dB}$
t_{GD}	Group delay (p-p) deviation	40	ps	1 GHz to $f_{–3dB}$

1. *Typical conditions of 25 °C at backside and 3.3 V supply.*
2. *The transimpedance gain is defined as $Z_T = V_{OUT(p\text{-}p)} / I_{IN(p\text{-}p)}$, where V_{OUT} is the p-p output voltage and I_{IN} is the p-p input current.*

Operating Conditions

This section contains the recommended operating conditions for the VSC7998 device.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{EE}	Power supply voltage	–4.9	–5.2	–5.5	V
T	Operating temperature(1)	–40		85	°C

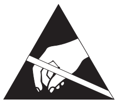
1. Lower limit of specification is ambient temperature, and upper limit is die backside temperature.

Stress Ratings

Stresses listed under the stress ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 6. Stress Ratings

Symbol	Parameter	Minimum	Maximum	Unit
V_{EE}	Power supply voltage	0.5	–6	V
I_{IN}	DC input current	0	3	mA
FBIN	Offset adjustment	0.5	–6	V
OFFP/OFFN	Output DC level	0.5	–6	V
OUTP/OUTN	Data output	–1.5	1.5	V
T_J	Junction temperature	–40	125	°C
T_S	Storage temperature	–55	140	°C
V_{ESD}	Electrostatic discharge voltage, human body model IIN high-speed input pin All other pins	 –50 –1000	 50 1000	 V V



ELECTROSTATIC DISCHARGE

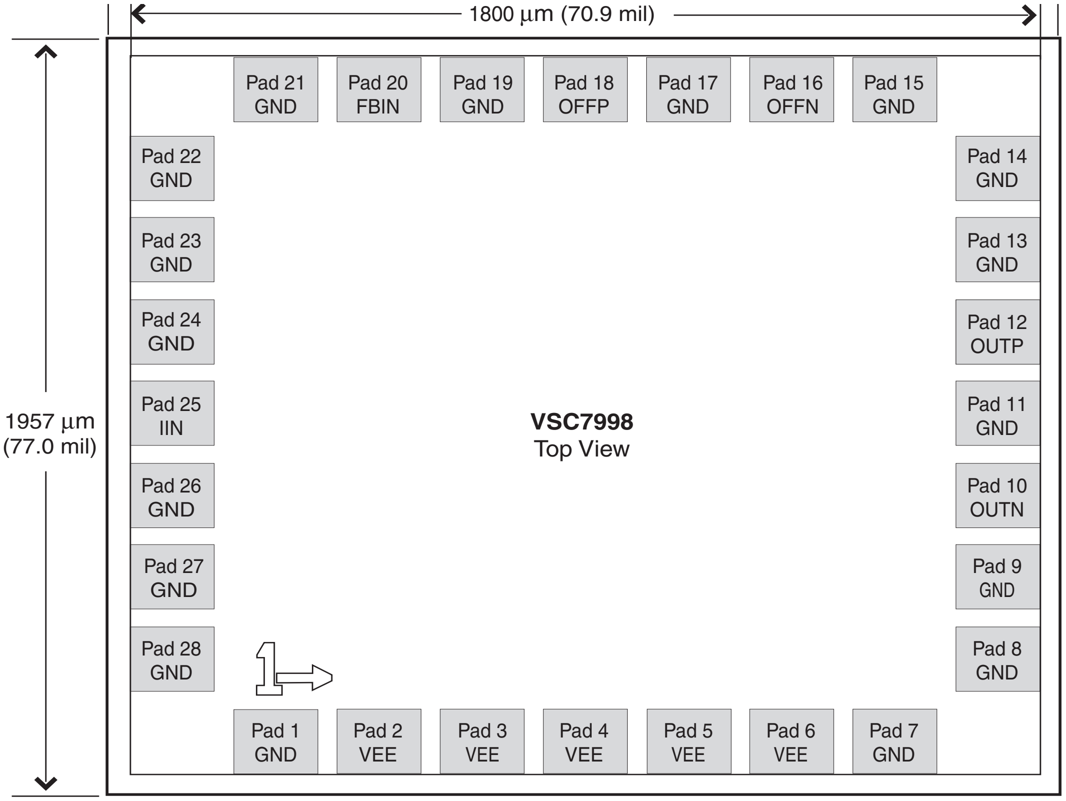
This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

Die Information

This section contains the pad diagram and pad identifications.

Pad Diagram

The following figure shows the pad diagram.



Die Size Including Scribe:	1957 µmx 1957 µm (77.0 mil x 77.0 mil)
Die Size Not Including Scribe:	1800 µm x 1800 µm (70.9 mil x 70.9 mil)
Pad Size:	94 µm x 94 µm (3.7 mil x 3.7 mil)
Pad Passivation Opening:	80 µm x 80 µm (3.1 mil x 3.1 mil)
Die Thickness:	279 µm (11 mils)

Connect die backside to V_{EE} or leave unconnected.

Figure 5. Pad Diagram

Pad Identifications

This following table lists the pad identifications.

Table 7. Pad Identifications

Signal	Pad Number	Coordinates (µm)		Description
		X	Y	
GND	1	292.2	88.9	Ground.
VEE	2	491.1	88.9	Negative power supply.
VEE	3	689.9	88.9	Negative power supply.
VEE	4	888.8	88.9	Negative power supply.
VEE	5	1087.7	88.9	Negative power supply.
VEE	6	1286.5	88.9	Negative power supply.
GND	7	1485.4	88.9	Ground.
GND	8	1689.1	253.0	Ground.
GND	9	1689.1	519.1	Ground.
OUTN	10	1689.1	690.2	Negative output.
GND	11	1689.1	889.1	Ground.
OUTP	12	1689.1	1087.9	Positive output (HIGH for optical input).
GND	13	1689.1	1259.0	Ground.
GND	14	1689.1	1525.0	Ground.
GND	15	1485.4	1689.1	Ground.
OFFN	16	1286.5	1689.1	OUTN DC Level. Connect 100 nF capacitor to ground.
GND	17	1087.7	1689.1	Ground.
OFFP	18	888.8	1689.1	OUTP DC Level. Connect 100 nF capacitor to ground.
GND	19	689.9	1689.1	Ground.
FBIN	20	491.1	1689.1	Offset control between OUTP and OUTN. Set to –2 V for no offset. See Figure 4.
GND	21	292.2	1689.1	Ground.
GND	22	99.1	1525.0	Ground.
GND	23	99.1	1326.1	Ground.
GND	24	99.1	1127.2	Ground.
IIN	25	99.1	889.1	Input from PIN diode.
GND	26	99.1	650.7	Ground.
GND	27	99.1	451.9	Ground.
GND	28	99.1	253.0	Ground.

Design Guidelines

Figure 6 shows a VSC7998 photodetector wire bonding diagram.

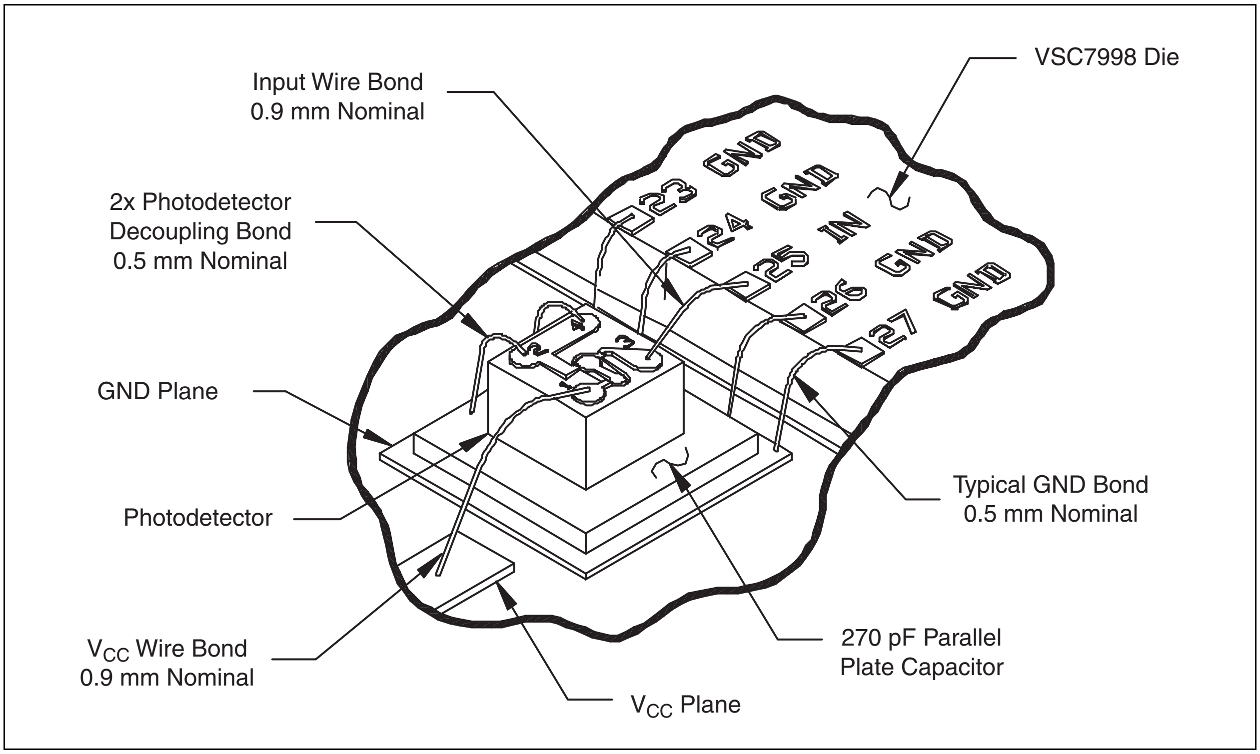


Figure 6. VSC7998 Photodetector Wire Bonding Diagram

Ordering Information

The following table provides the ordering information for the VSC7998 device.

Table 8. VSC7998 SONET/SDH 10.7 Gbps Transimpedance Amplifier

Part Number	Description
VSC7998-W	Dice in waffle pack

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