

TB62717NG, TB62717FG

24 Bit Constant Current Drivers (3 × 8 Bit Shift Register & Latch)

The TB62717NG/FG are specifically designed constant current driver for LED & LED DISPLAY.

This constant-current output-circuits is able to set up at an external resistor.

This IC is monolithic integrated circuit designed to be used together with Bi-CMOS process.

The devices builds in three block composed by the shift register circuit of eight bits, the latch-circuit of eight bits, the AND gate circuit of eight bits and the constant-current output circuits of eight bits.

This device has a SERIAL-IN terminal and a SERIAL-OUT terminal three blocks to each, and has a CLOCK terminal and a LATCH terminal three blocks to the commonness.

The TB62717NG/FG complies with RoHS regulation.

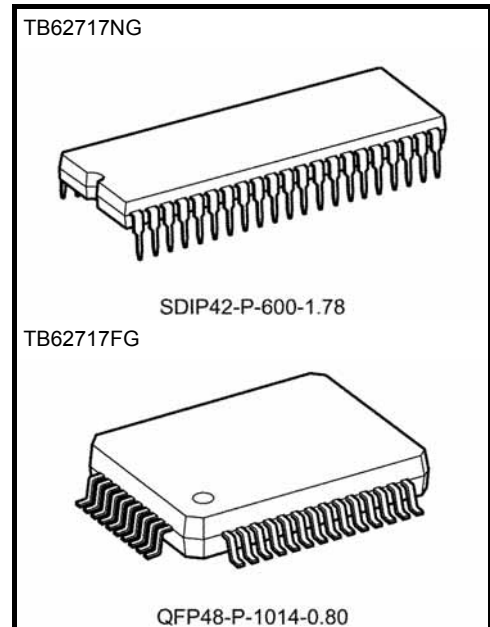
Features

- Constant current output
: Able to set up at an external resistor for 2 to 50 mA.
- Schmitt triggered input
- Recommended operating condition
 - Maximum clock Frequency
: $f_{CLK} = 10.0$ MHz (cascade connected)
 - IC supply voltage: $V_{DD} = 4.5$ to 5.5 V
 - Output voltage: $V_{OUT} = 0.4$ to 17 V
 - Operating temperature: $T_{opr} = -40$ to 85°C

Constant Output Current Matching

Output-GND Voltage	Current Matching	Output Current
≥ 0.4 V	$\pm 6.0\%$	50 mA

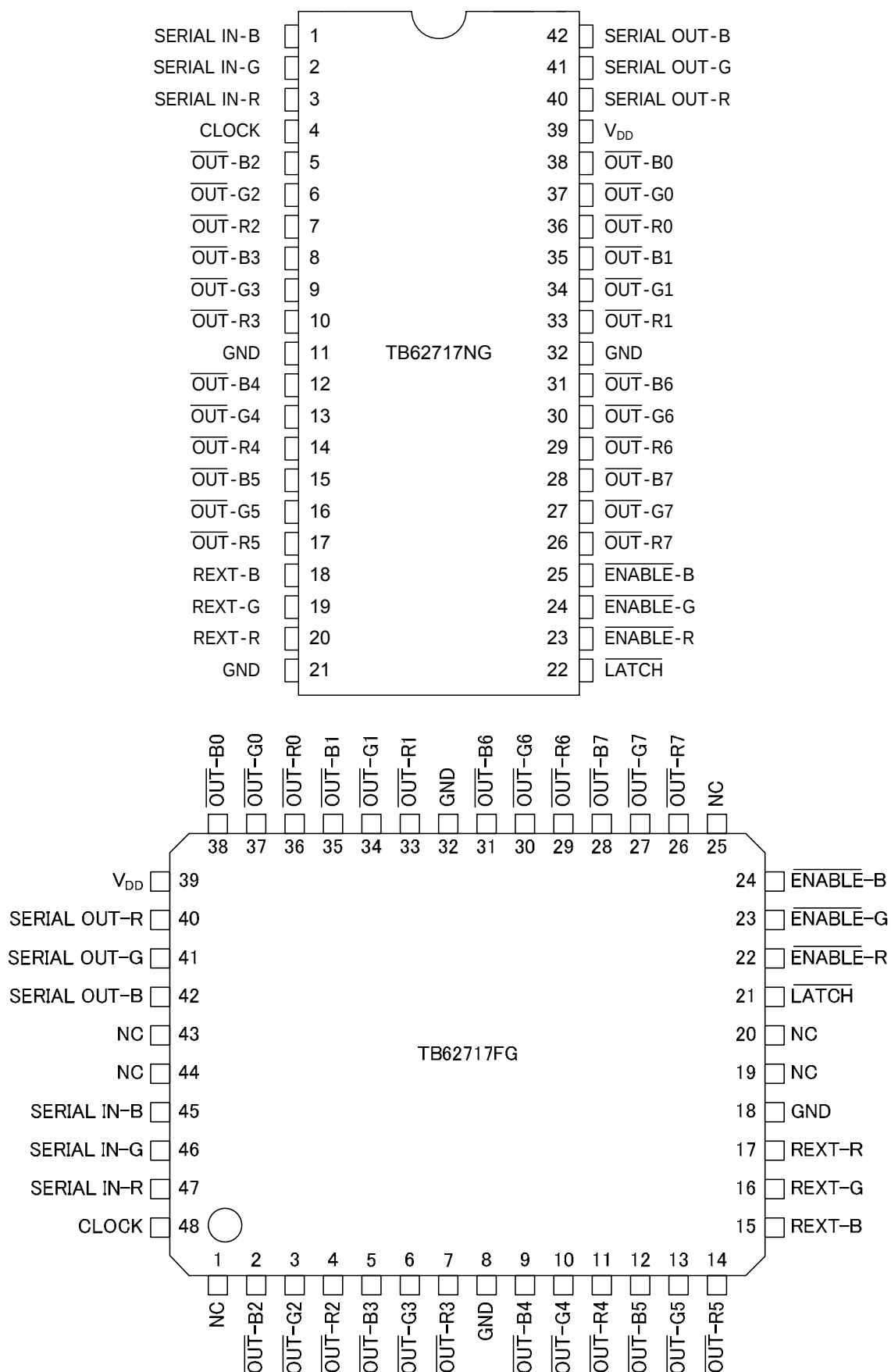
- 5 V CMOS Compatible Input
- Package: NG type SDIP42-P-600-1.78
FG type QFP48-P-1014-0.80



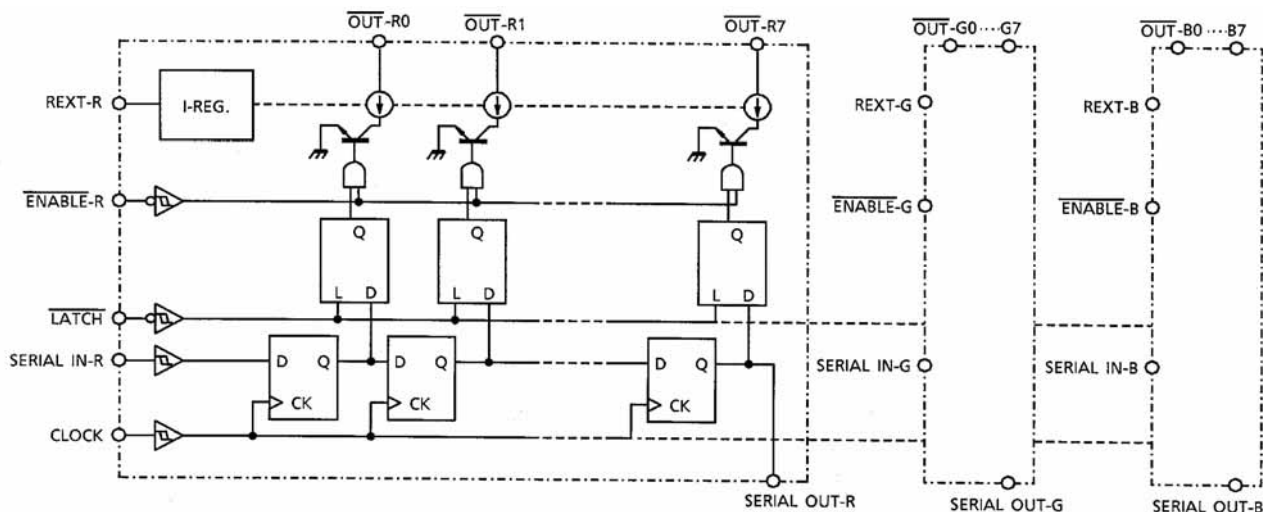
Weight

SDIP42-P-600-1.78: 4.13 g (typ.)
QFP48-P-1014-0.80: 0.83 g (typ.)

Pin Connection (top view)



Block Diagram



Note: $I_{OUT} = 30 \text{ mA/bit (max)}$ in 24 bit output activate

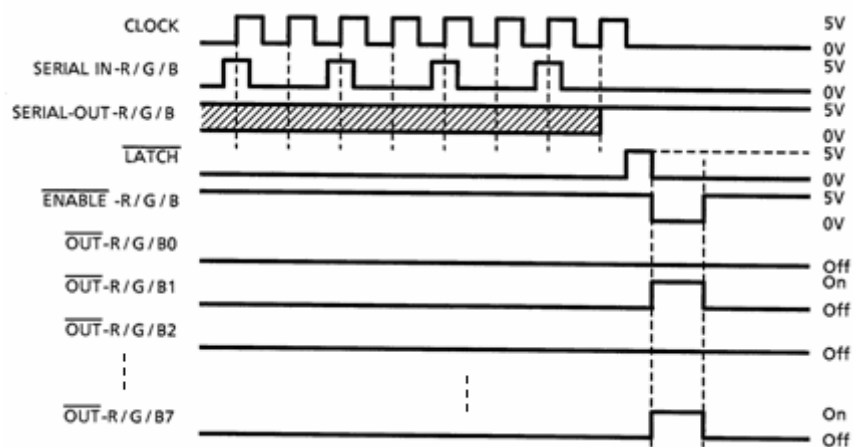
Truth Table

CLOCK	LATCH	ENABLE R/G/B	SERIAL-IN R/G/B	$\overline{OUT} - \dots \overline{OUT} - \dots \overline{OUT} -$ R/G/B0 R/G/B3 R/G/B7	SERIAL-OUT R/G/B
UP	H	L	D_n	$D_n \dots D_{n-3} \dots D_{n-7}$	D_{n-7}
UP	L	L	D_{n+1}	No Change	D_{n-6}
DOWN	H	L	D_{n+1}	$D_{n+1} \dots D_{n-2} \dots D_{n-6}$	D_{n-6}
—	X	L	D_{n+2}	No Change	D_{n-6}
—	X	H	D_{n+3}	All Off	D_{n-6}

Note: $\overline{OUT} - R/G/B0$ to 7 = on in case of $D_n = H$ level and $\overline{OUT} - R/G/B0$ to 7 = off in case of $D_n = L$ level.

A resistor is connected with R-EXT and GND accompanied with outside, and it is necessary that a correct power supply voltage is supplied.

Timing Diagram



Note: LATCH is level sensitive, not rising edges sensitive and not synchronous CLOCK.

Input of LATCH –terminal to “H” level, data passes latches, and input to “L” level, data hold latches.

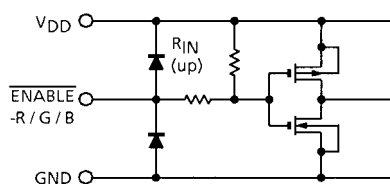
Input of ENABLE –terminal to “H” level, all output do off.

Terminal Explanation

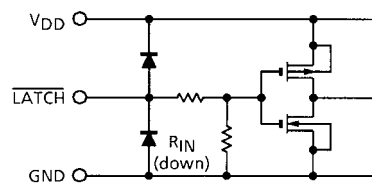
Numbers		Name	Explanation
NG	FG		
36 to 38	36 to 38	$\overline{\text{OUT}} - \text{R/G/B0}$	This terminal is the constant-current output of the 1st bit of each block. An output terminal is high-active in the input data.
33 to 35	33 to 35	$\overline{\text{OUT}} - \text{R/G/B1}$	This terminal is the constant-current output of the 2nd bit of each block. An output terminal is high-active in the input data.
5 to 7	2 to 4	$\overline{\text{OUT}} - \text{R/G/B2}$	This terminal is the constant-current output of the 3rd bit of each block. An output terminal is high-active in the input data.
8 to 10	5 to 7	$\overline{\text{OUT}} - \text{R/G/B3}$	This terminal is the constant-current output of the 4th bit of each block. An output terminal is high-active in the input data.
12 to 14	9 to 11	$\overline{\text{OUT}} - \text{R/G/B4}$	This terminal is the constant-current output of the 5th bit of each block. An output terminal is high-active in the input data.
15 to 17	12 to 14	$\overline{\text{OUT}} - \text{R/G/B5}$	This terminal is the constant-current output of the 6th bit of each block. An output terminal is high-active in the input data.
29 to 31	29 to 31	$\overline{\text{OUT}} - \text{R/G/B6}$	This terminal is the constant-current output of the 7th bit of each block. An output terminal is high-active in the input data.
26 to 28	26 to 28	$\overline{\text{OUT}} - \text{R/G/B7}$	This terminal is the constant-current output of the 8th bit of each block. An output terminal is high-active in the input data.
11, 21, 32	8, 18, 32	GND	These three terminals are GND terminals. We recommend that it is grounded (this terminal all).
1 to 3	45 to 47	SERIAL IN-R/G/B	This terminal is a serial-data input of each block.
4	48	CLOCK	This terminal is the clock signal input which is common to each block.
22	21	$\overline{\text{LATCH}}$	This terminal is latch signal input. This terminal is a level latch. Therefore, input data are held while input of a L level is being maintained. It only passes through the data on the output side in the case of the H level.
23 to 25	22 to 24	$\overline{\text{ENABLE}} - \text{R/G/B}$	This terminal is output control signal input. When input of a L level is maintained, an output terminal drives this terminal corresponding to the input data. Output is made a non-drive independently with the input data in the case of the H level.
18 to 20	15 to 17	REXT- R/G/B	This terminal is for the resistance connection which the output electric current value of each block is set up to. Resistance with the outside is connected between this terminal and GND. Output electric current is set up in the value corresponding to the re
39	39	V_{DD}	This terminal is input of a power supply voltage 5 V.
40 to 42	40 to 42	SERIAL OUT - R/G/B	This terminal is a serial-data output of each block.
-	1,19~20 25,43~44	NC	terminal is a unconnection.

Equivalent Circuit About the Input and Output Terminal

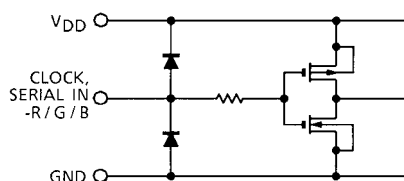
1. The terminal of the $\overline{\text{ENABLE}}\text{-R/G/B}$



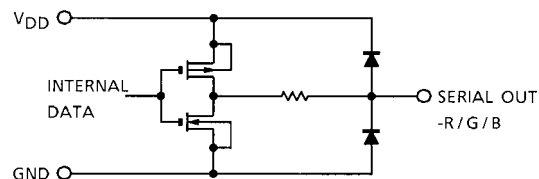
2. The terminal of the $\overline{\text{LATCH}}$



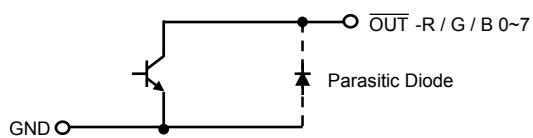
3. The terminal of the CLOCK and SERIAL IN-R/G/B



4. The terminal of the SERIAL OUT-R/G/B



5. The terminal of the $\overline{\text{OUT}}\text{-R/G/B0~7}$



Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Supply voltage		V _{DD}	+7.0	V
Input voltage		V _{IN}	−0.4 to V _{DD} + 0.4	V
Output current		I _{OUT}	+50	mA
Output voltage		V _{OUT}	−0.5 to +17.0	V
Clock frequency		f _{CLK}	15	MHz
GND terminal current (Note 1)		I _{GND}	1200	mA
Power dissipation	TB62717N	P _D	1.78 (ON PCB)/1.56 (FREE AIR)	°C/W
(Note 2)	TB62717F		1.38 (ON PCB)/0.86 (FREE AIR)	
Thermal resistance	TB62717N	R _{th} (j-a)	70 (ON PCB)/80 (FREE AIR)	°C/W
(Note 2)	TB62717F		90 (On PCB)/145 (FREE AIR)	
Operating temperature		T _{opr}	−40 to +85	°C
Storage temperature		T _{stg}	−55 to +150	°C

Note 1: Use all GND-terminals.

Note 2: Ambient temperature delayed the above 25°C with the type NG with 14.2 mW/°C and the type FG with 11.1 mW/°C in on PCB (Glass Epoxy PCB 50 × 50 × 1.6 mm Cu 36%).

Recommended Operating Condition (Ta = 25°C unless otherwise noted)

Characteristics	Symbol	Condition	Min	Typ.	max	Unit
Supply voltage	V _{DD}	—	4.5	5.0	5.5	V
Output voltage	V _{OUT}	—	0.4	—	15.0	V
Output current	I _{OUT}	DC 1 circuit	—	—	35	mA
	I _{OH}	SERIAL-OUT	—	—	-1.0	
	I _{OL}	SERIAL-OUT	—	—	1.0	
Input voltage	V _{IH}	—	0.7 V _{DD}	—	V _{DD} + 0.3	V
	V _{IL}	—	-0.3	—	0.3 V _{DD}	
CLOCK pulse width	t _{wCLK}	V _{DD} = 4.5~5.5V, CLOCK = "H" or "L"	50	—	—	ns
LATCH pulse width	t _{w/LATCH}	V _{DD} = 4.5 to 5.5 V	100	—	—	ns
ENABLE pulse width	t _{w/EN}		4500	—	—	ns
Set-up time for DATA	t _{setup(D)}		60	—	—	ns
Hold time for DATA	t _{hold(D)}		20	—	—	ns
Set-up time for LATCH	t _{setup(L)}		100	—	—	ns
Hold time for LATCH	t _{hold(L)}		60	—	—	ns
Clock frequency	f _{CLK}	V _{DD} = 4.5~5.5V, Cascade operation	—	—	10.0	MHz
Power dissipation	P _D	Ta = 85°C (SDIP42 on PCB)	—	—	0.92	W
		Ta = 85°C (QFP48 on PCB)	—	—	0.71	

Electrical Characteristics (Ta = 25°C unless otherwise noted)

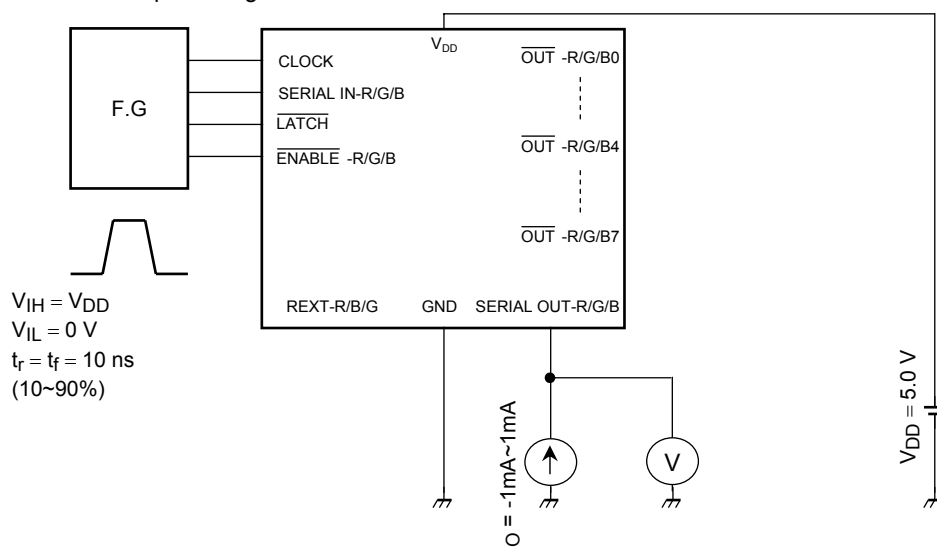
Characteristics		Symbol	Test Circuit	Condition	Min	Typ.	Max	Unit
Input voltage	"H" level	V _{IH}	-	Ta = -40 to 85°C	0.7 V _{DD}	—	V _{DD}	V
	"L" level	V _{IL}			GND	—	0.3 V _{DD}	
Output leakage current		I _{OH}	5	V _{OH} = 15.0 V	—	—	10	μA
Output voltage	SOUT-R/G/B	V _{OL}	1	I _{OL} = 1.0 mA	—	—	0.4	V
		V _{OH}		I _{OL} = -1.0 mA	4.6	—	—	
Output current		I _{OL}	5	V _{CE} = 0.4 V	25.5	30.0	34.5	mA
	Current skew	Δ _{OL}		I _{OL} = 30 mA, V _{CE} = 0.4 V R _{EXT} = 660 Ω	—	±1.5	±6.0	
Supply voltage regulation		%/V _{DD}	5	R _{EXT} = 660 Ω Ta = -40~85°C	—	1.5	5.0	%/V
Pull-up resistor		R _{IN} (up)	3	—	150	300	600	k Ω
Pull-down resistor		R _{IN} (down)	2	—	150	300	600	k Ω
Supply current	"OFF"	I _{DD} (off) 1	4	R _{EXT} = OPEN	—	1.2	2.4	mA
		I _{DD} (off) 2		All output off	7.0	12.0	16.0	
	"ON"	I _{DD} (on) 1		R _{EXT} = 660 Ω	15.0	28.0	40.0	
				All output on				

Switching Characteristics (Ta = 25°C unless otherwise noted)

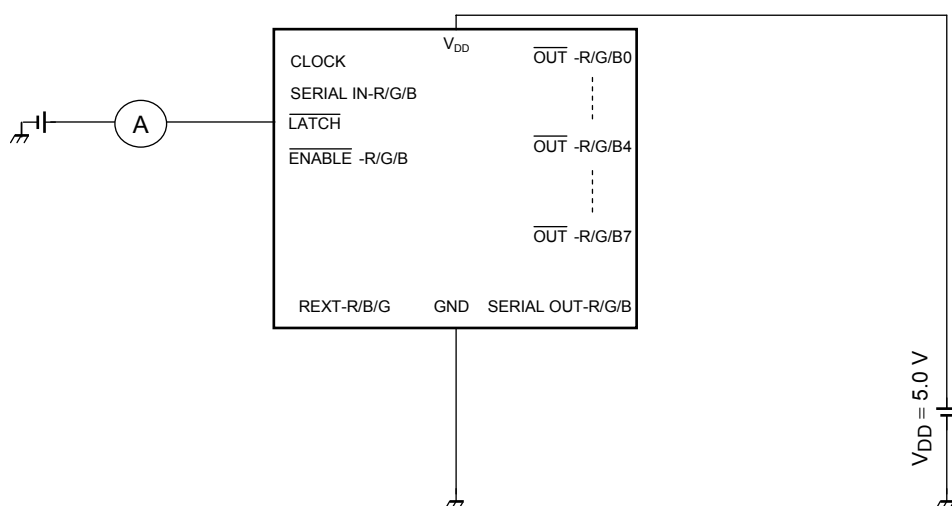
Characteristics		Symbol	Test Circuit	Condition	Min	Typ.	Max	Unit
Propagation delay time ("L" to "H")	CLK - $\overline{\text{OUTn}}$	t _{PLH1}	6	V _{DD} = 5.0 V V _{CE} = 0.4 V V _{IH} = V _{DD} V _{IL} = GND R _{EXT} = 660 Ω V _L = 3.0 V C _L = 10.5 pF	—	1200	1500	ns
	$\overline{\text{LATCH}}$ - $\overline{\text{OUTn}}$	t _{PLH2}			—	1200	1500	
	$\overline{\text{EN}}$ - $\overline{\text{OUTn}}$	t _{PLH3}			—	1200	1500	
	CLK - SOUT	t _{PLH4}			—	30	70	
Propagation delay time ("H" to "L")	CLK - $\overline{\text{OUTn}}$	t _{PHL1}			—	700	1000	
	$\overline{\text{LATCH}}$ - $\overline{\text{OUTn}}$	t _{PHL2}			—	700	1000	
	$\overline{\text{EN}}$ - $\overline{\text{OUTn}}$	t _{PHL3}			—	700	1000	
	CLK - SOUT	t _{PHL4}			—	30	70	
Maximum CLOCK rise time		t _r			—	—	10	μs
Maximum CLOCK fall time		t _f			—	—	10	
Output rise time		t _{or}			300	600	1000	ns
Output fall time		t _{of}			150	300	600	

Test Circuit

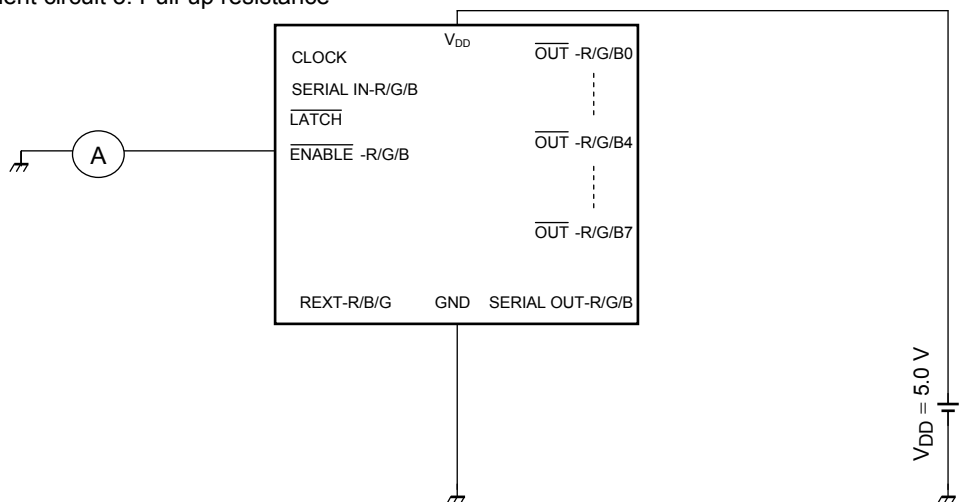
Measurement circuit 1: Output voltage



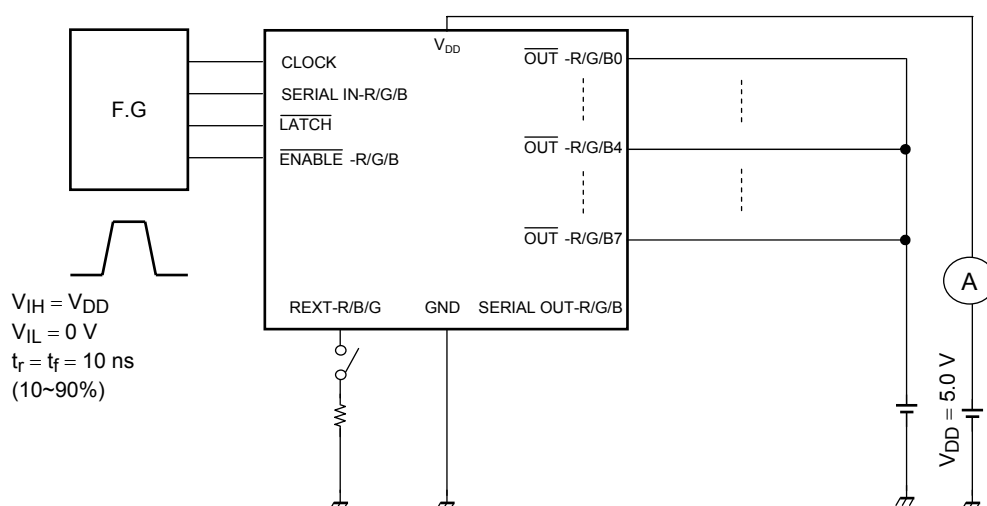
Measurement circuit 2: Pull-down resistance



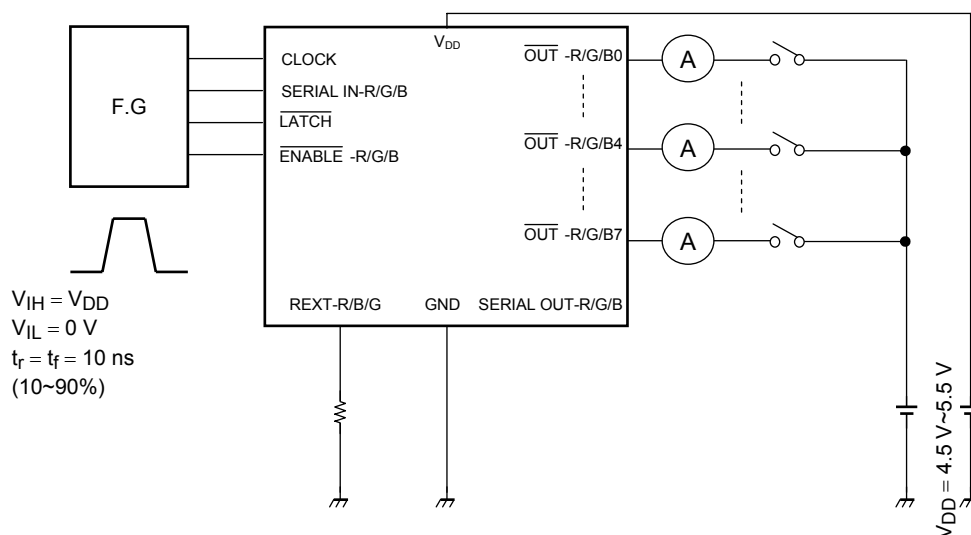
Measurement circuit 3: Pull-up resistance



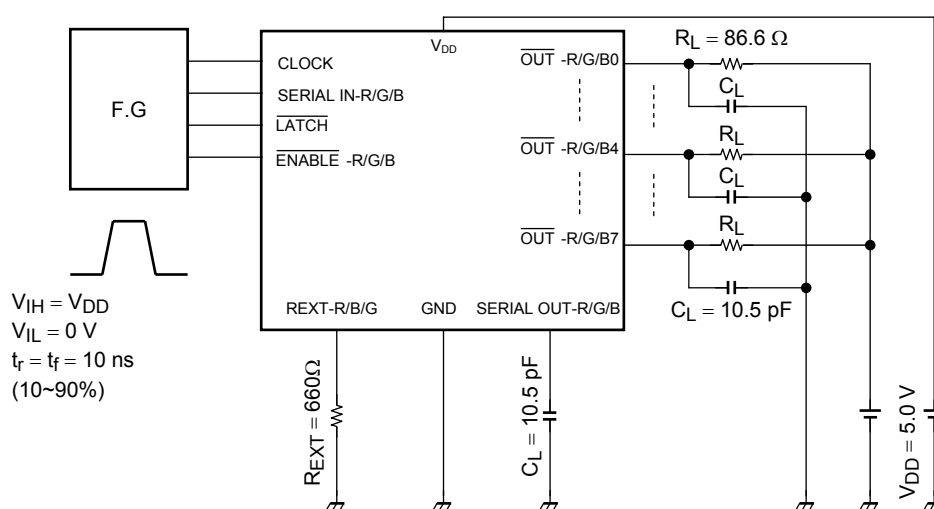
Measurement circuit 4: Supply current



Measurement circuit 5: Output leakage current / Output current / Output current skew / Supply voltage regulation

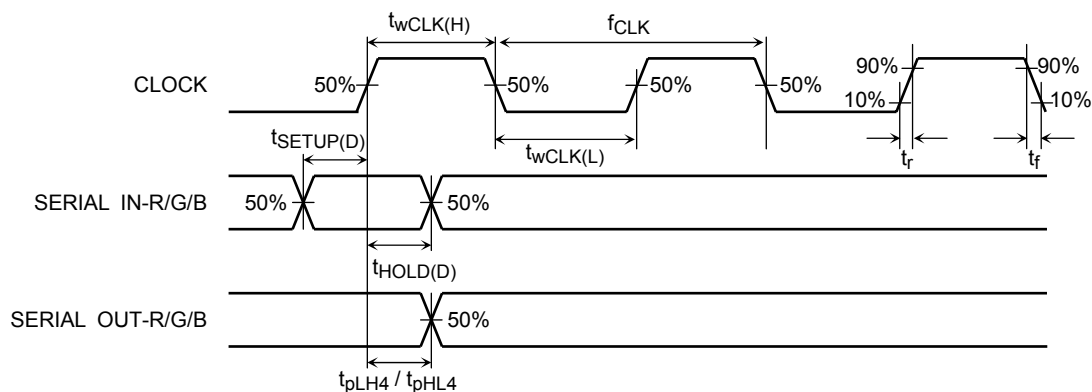


Measurement circuit 6: Switching Characteristics

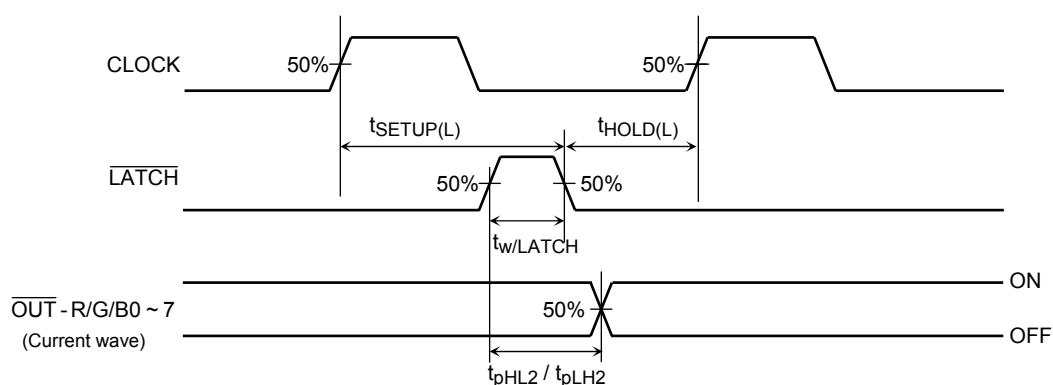


Timing Waveform

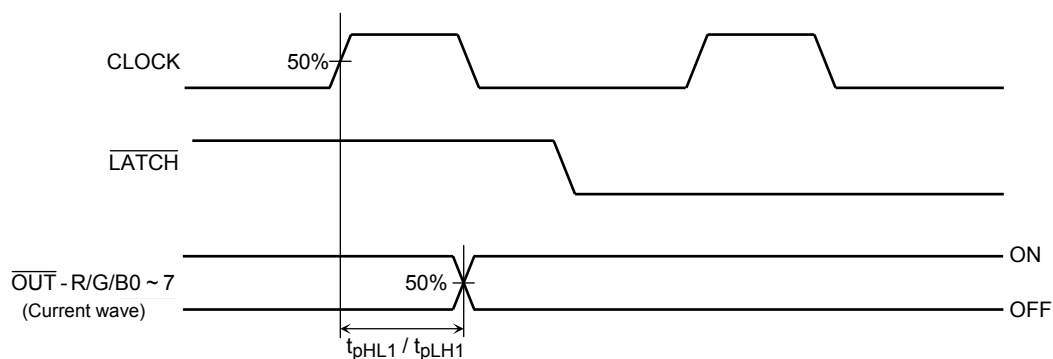
1. CLOCK, SERIAL IN - R/G/B, SERIAL OUT - R/G/B



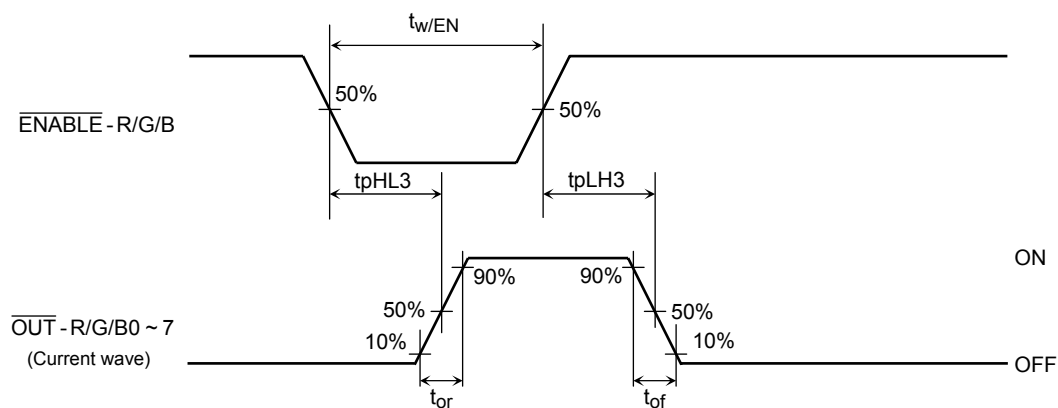
2. CLOCK, $\overline{LATCH}$, $\overline{OUT}$ - R/G/B0 ~ 7

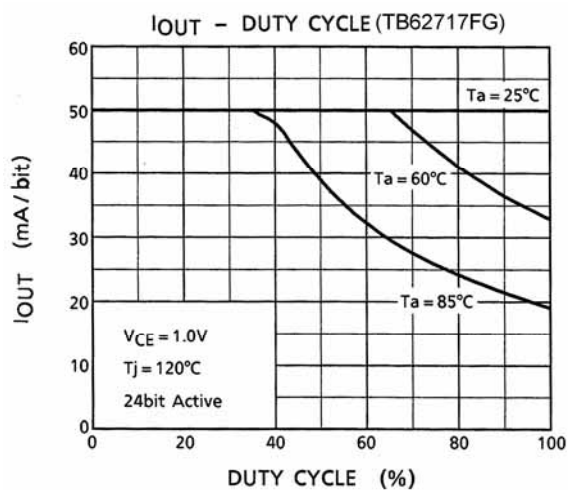
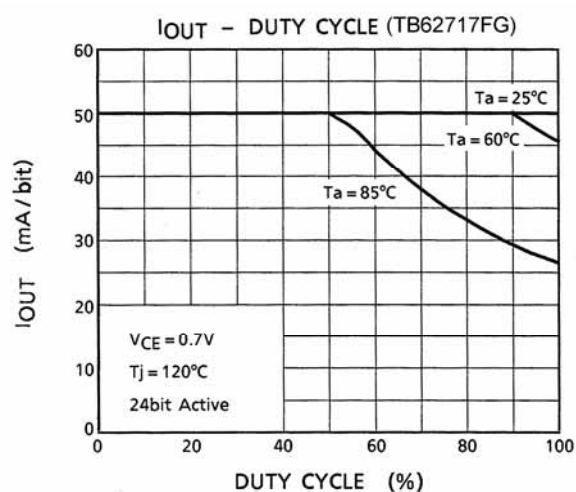
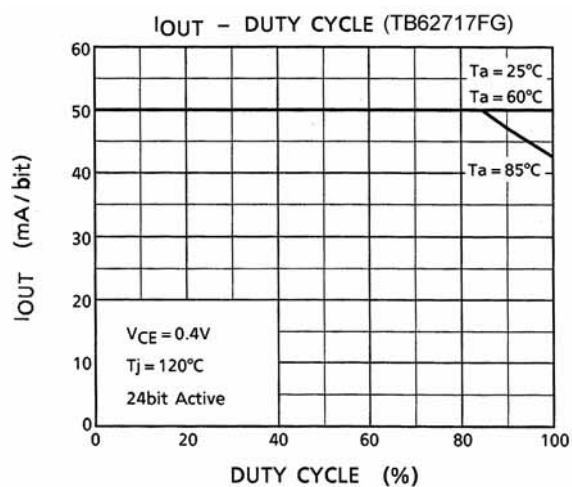
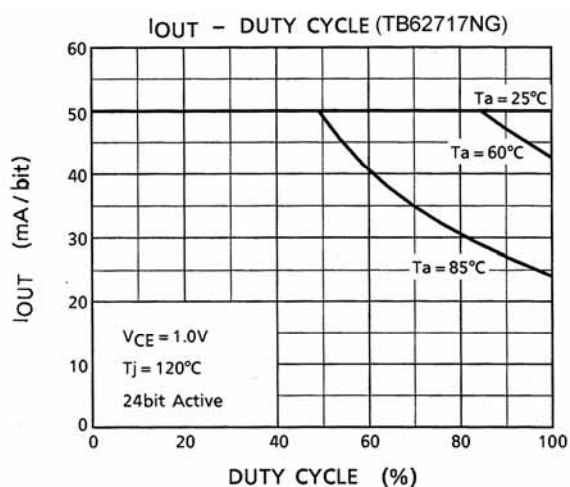
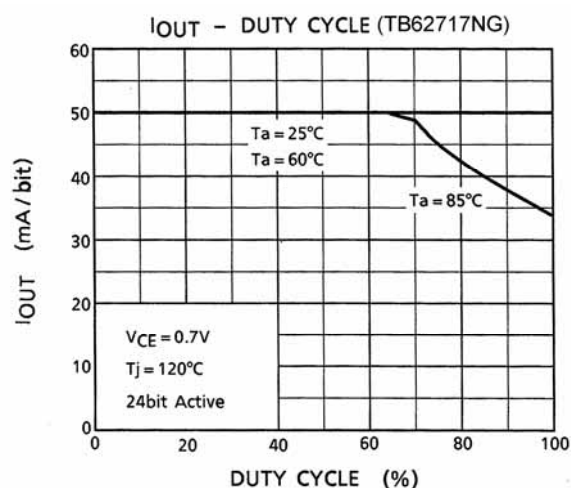
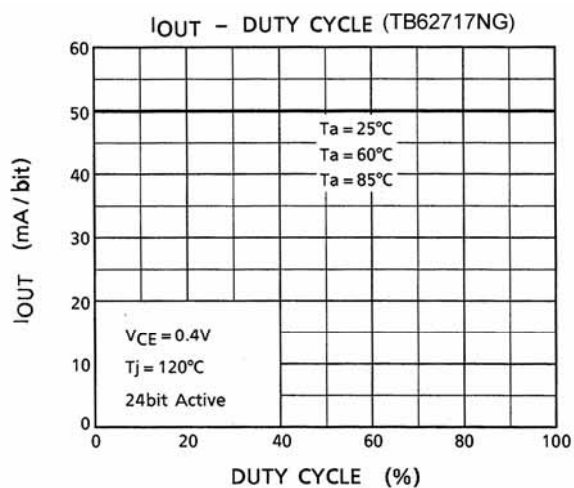


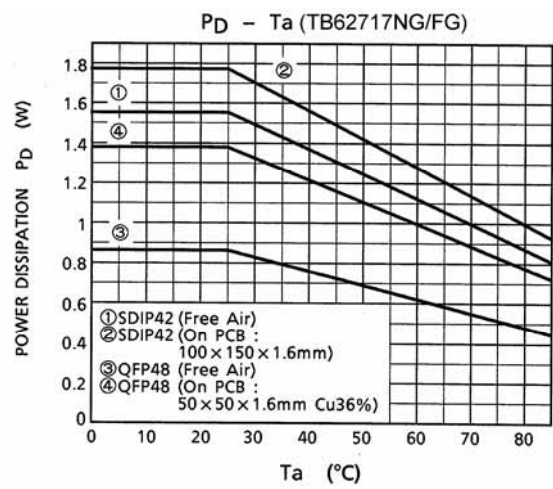
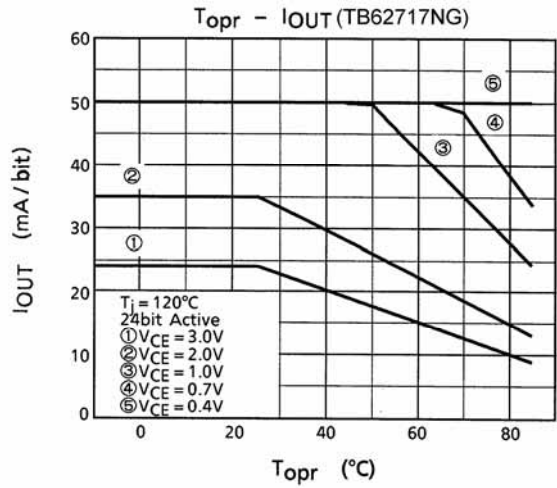
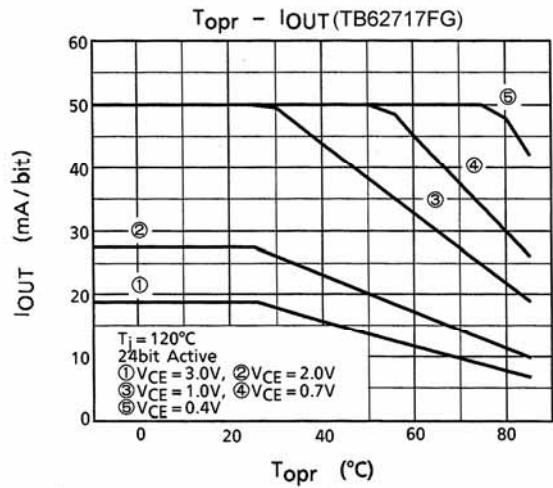
3. CLOCK, $\overline{LATCH}$, $\overline{OUT}$ - R/G/B0 ~ 7



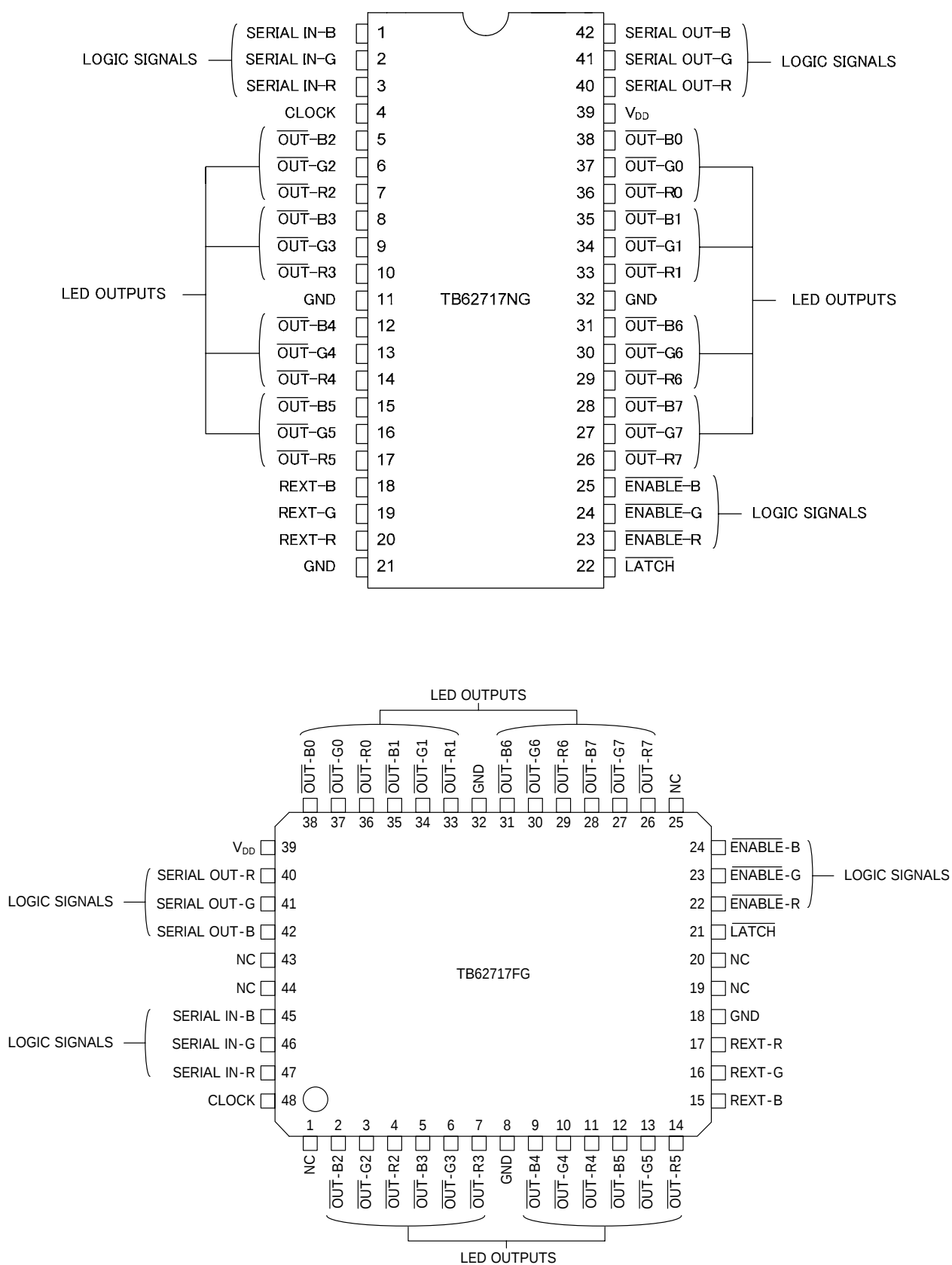
4. $\overline{ENABLE}$ - R/G/B, $\overline{OUT}$ - R/G/B0 ~ 7







I/O Layout Image



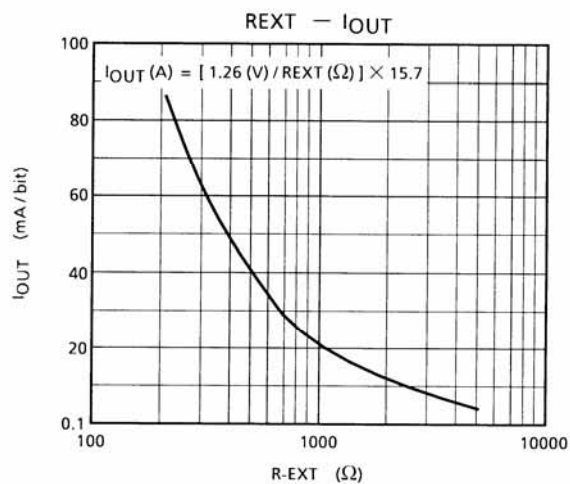


Figure 1

[1] Output Current (I_{OUT})

I_{OUT} is set by the external resistor (R-EXT) as shown in Figure 1.

[2] Total Supply Voltage (V_{LED})

This device can operate 0.4 to 0.7 V (V_O).

When a higher voltage is input to the device, the excess voltage is consumed inside the device, that leads to power dissipation.

In order to minimize power dissipation and loss, we would like to recommend to set the total supply voltage as shown below,

$$V_{LED} = V_{CE} (T_r V_{sat}) + V_f (\text{LED Forward voltage}) + V_O (\text{IC supply voltage})$$

When the total supply is too high considering the power dissipation of this device, an additional R can decrease the supply voltage (V_O).

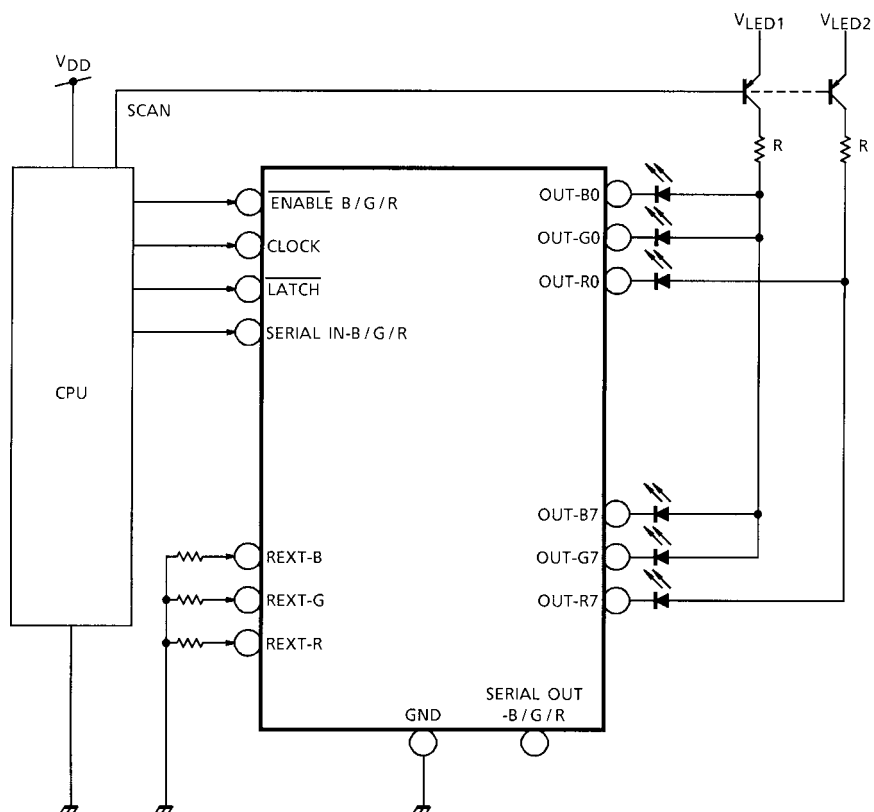
[3] Pattern Layout

This device owns only one ground pin that means signal ground pin and power ground pin are common.

If ground pattern layout contains large inductance and impedance, and the voltage between ground and LATCH, CLOCK terminals exceeds 2.5 V by switching noise in operation, this device may miss-operate.

So we would like you to pay attention to pattern layout to minimize inductance.

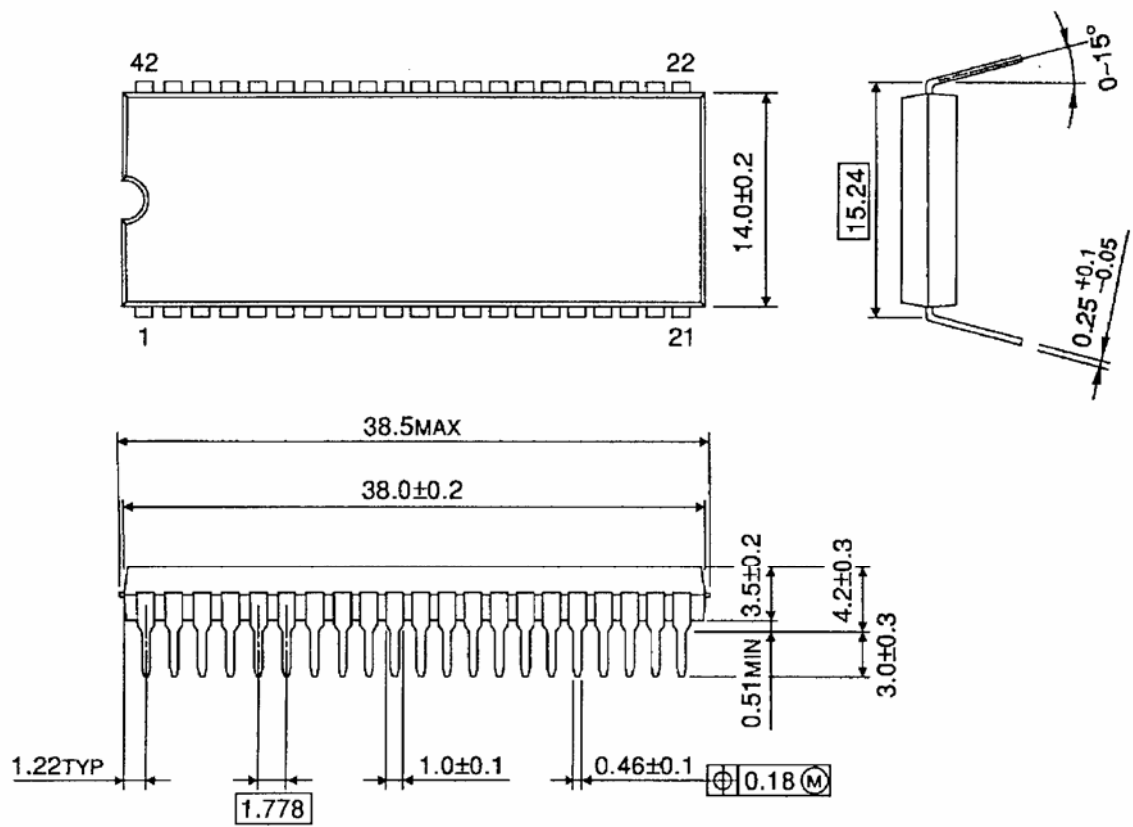
Pattern Layout



Package Dimensions

SDIP42-P-600-1.78

Unit : mm

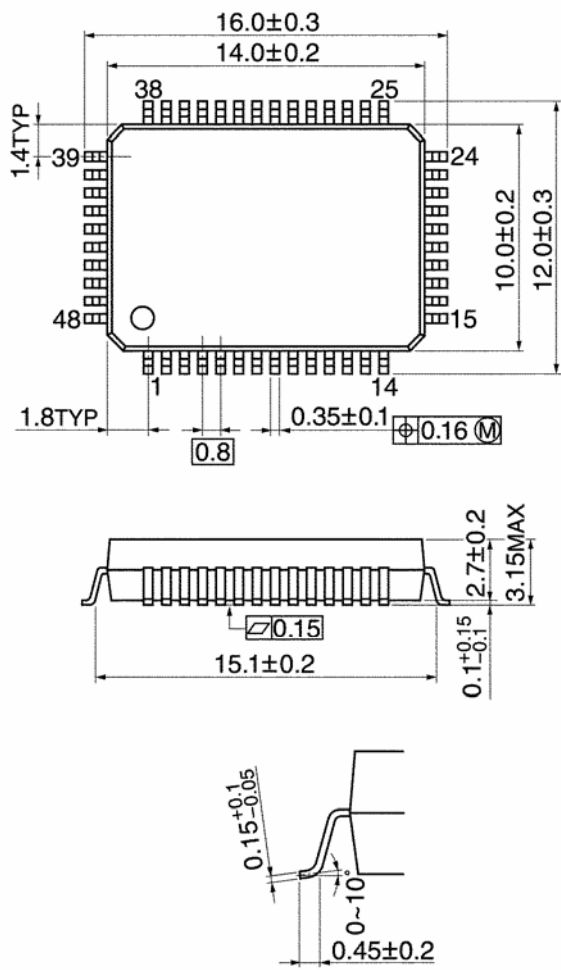


Weight: 4.13 g (typ.)

Package Dimensions

QFP48-P-1014-0.80

Unit: mm



Weight: 0.83 g (typ.)

Notes on Contents**1. Block Diagrams**

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only.

Thorough evaluation is required, especially at the mass production design stage.

Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on Handling of ICs

- (1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
- (2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.
- (3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.
- (4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.
- (5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to Remember on Handling of ICs

- (1) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat radiation with peripheral components.
- (2) Back-EMF
When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

About solderability, following conditions were confirmed

- Solderability

- (1) Use of Sn-37Pb solder Bath

- solder bath temperature = 230°C
 - dipping time = 5 seconds
 - the number of times = once
 - use of R-type flux

- (2) Use of Sn-3.0Ag-0.5Cu solder Bath

- solder bath temperature = 245°C
 - dipping time = 5 seconds
 - the number of times = once
 - use of R-type flux

RESTRICTIONS ON PRODUCT USE

20070701-EN

- The information contained herein is subject to change without notice.
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