National Semiconductor

DM5490A/DM7490A, DM5492A/DM7492A, DM5493A/DM7493A Decade, Divide by 12, and Binary Counters

General Description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 90A, divide-by-six for the 92A and divide-by-eight for the 93A.

All of these counters have a gated zero reset and the 90A also has gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary), the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the 90A counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

Features

- Typical power dissipation
  - 90A 145 mW
  - 92A, 93A 130 mW
- Count frequency 42 MHz

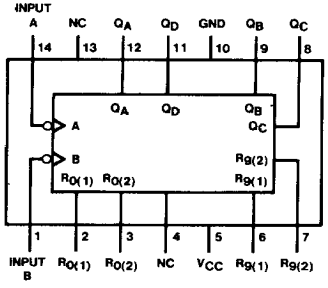
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

Dual-In-Line Package



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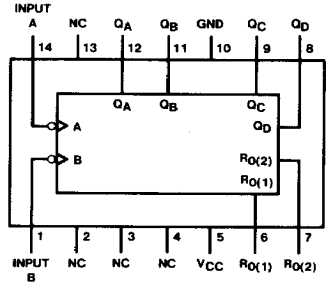
5490A (J) **7490A (N)**

Dual-In-Line Package



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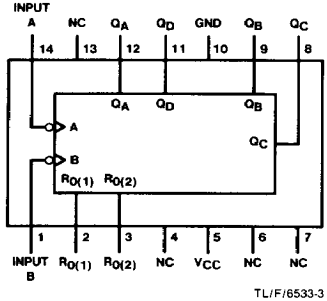
5492A (J) **7492A (N)**

Dual-In-Line Package



TL/F/6533-3

5493A (J) **7493A (N)**

Recommended Operating Conditions

Sym	Parameter		DM5490A			DM7490A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency	A	0		32	0		32	MHz
		Q_B	0		16	0		16	
t_W	Pulse Width	A	15			15			ns
		B	30			30			
		Reset	15			15			
t_{REL}	Reset Release Time		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'90A Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min V_{IL} = Max (Note 4)			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	A			80	μA
			Reset			40	
			B			120	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	A			−3.2	mA
			Reset			−1.6	
			B			−4.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			29	42	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 4: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

'90A Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	A to Q_A	32	42		MHz
	B to Q_B	16			
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_A		10	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_A		12	18	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_D		32	48	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_D		34	50	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_B		10	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_B		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_C		21	32	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_C		23	35	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_D		21	32	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_D		23	35	ns
t_{PLH} Propagation Delay Time Low to High Level Output	SET-9 to Q_A, Q_D		20	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	SET-9 to Q_B, Q_C		26	40	ns
t_{PHL} Propagation Delay Time High to Low Level Output	SET-0 to Any Q		26	40	ns

Recommended Operating Conditions

Sym	Parameter		DM5492A			DM7492A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency	A	0		32	0		32	MHz
		Q_B	0		16	0		16	
t_W	Pulse Width	A	15			15			ns
		B	30			30			
		Reset	15			15			
t_{REL}	Reset Release Time		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'92A Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min V_{IL} = Max (Note 4)			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Reset			40	μA
			A			80	
			B			120	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Reset			−1.6	mA
			A			−3.2	
			B			−4.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			26	39	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, both R0 inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 4: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

'92A Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	A to Q_A	32	42		MHz
	B to Q_B	16			
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_A		10	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_A		12	18	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_D		32	48	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_D		34	50	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_B		10	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_B		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_C		10	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_C		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_D		21	32	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_D		23	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	SET-0 to Any Q		26	40	ns

Recommended Operating Conditions

Sym	Parameter		DM5493A			DM7493A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency	A	0		32	0		32	MHz
		Q_B	0		16	0		16	
t_W	Pulse Width	A	15			15			ns
		B	30			30			
		Reset	15			15			
t_{REL}	Reset Release Time		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'93A Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min V_{IL} = Max (Note 4)			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Reset			40	μA
			A			80	
			B			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Reset			−1.6	mA
			A			−3.2	
			B			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			26	39	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, both R0 inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 4: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

'93A Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	A to Q_A	32	42		MHz
	B to Q_B	16			
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_A		10	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_A		12	18	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_D		46	70	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_D		46	70	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_B		10	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_B		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_C		21	32	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_C		23	35	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_D		34	51	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_D		34	51	ns
t_{PHL} Propagation Delay Time High to Low Level Output	SET-0 to Any Q		26	40	ns

Function Tables (Note D)

90A
BCD COUNT SEQUENCE
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

90A
BI-QUINARY (5-2)
(See Note B)

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

92A
COUNT SEQUENCE
(See Note C)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

93A
COUNT SEQUENCE
(See Note C)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

90A
RESET/COUNT FUNCTION TABLE

Reset Inputs				Output			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

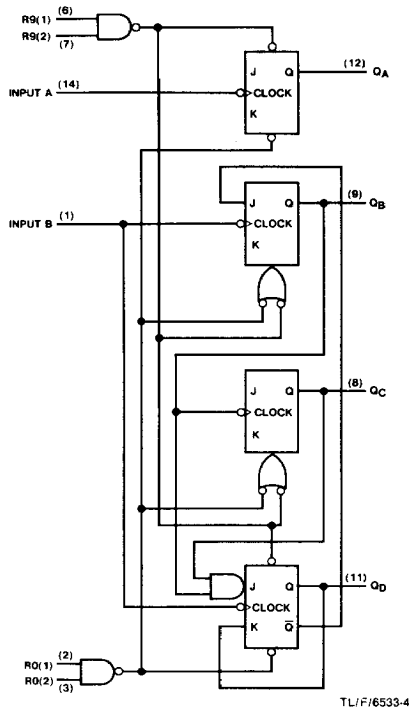
92A, 93A
RESET/COUNT FUNCTION TABLE

Reset Inputs		Output			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

Note A: Output Q_A is connected to input B for BCD count.
Note B: Output Q_D is connected to input A for bi-quinary count.
Note C: Output Q_A is connected to input B.
Note D: H = High Level, L = Low Level, X = Don't Care.

Logic Diagrams

90A



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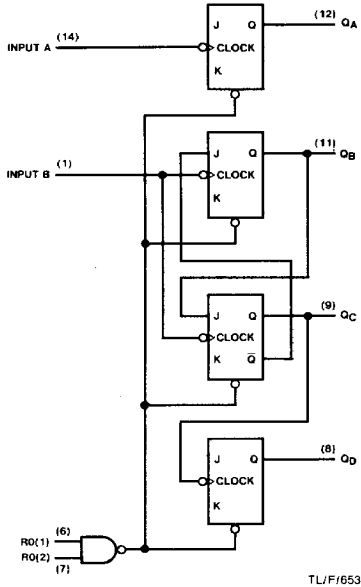
92A



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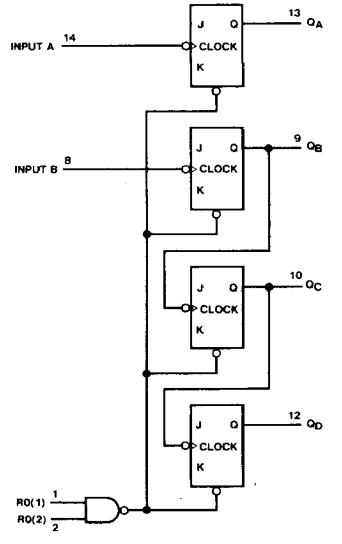
93A



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The J and K inputs shown without connection are for reference only and are functionally at a high level.