4M X 32 Bits DRAM SO-DIMM EDO Memory Module

FEATURES

- Performance range:

t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
60ns	15ns	104ns	25ns

- Extended Data Out (EDO) Mode operation called hyper page mode
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- +3.3V ± 0.3V power supply
- 2048 cycles/32ms refresh
- JEDEC standard pinout
- Gold edge connectors

GENERAL DESCRIPTION

The Simple Technology STI324004D1-60VG is a 4M x 32 bits Dynamic RAM high density memory module. The Simple Technology STI324004D1-60VG consist of eight CMOS 4M x 4 bits DRAMs in 24-pin SOJ packages mounted on a 72-pin glass epoxy substrate. Eight 0.1μF decoupling capacitors are mounted for the DRAMs.

The STI324004D1-60VG is a Small Outline Dual In-line Memory Module intended for mounting into 72-pin SO-DIMM edge connector sockets.

SUMMARY OF OPERATION

Each bit of the DIMM is addressed through a 20-bit address entered 10 bits at a time (A0-A10). $\overline{RAS}$ latches the first 11 bits, and $\overline{CAS}$ latches the last 11 bits.

The state of $\overline{W}$ selects between a read cycle ($\overline{W}$ is high) or write cycle ($\overline{W}$ is low).

In a write cycle, the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is last, latches the data. A early write cycle occurs when $\overline{W}$ becomes low before $\overline{CAS}$. In this case, the output pins are high-z until the next $\overline{CAS}$ cycle.

Traditionally, Fast Page Mode read cycles turn the data-out to high-z when $\overline{CAS}$ goes inactive. However, for EDO Page Mode read cycles (called Hyper Page Mode), data-out is valid after $\overline{CAS}$ becomes high, as long as $\overline{RAS}$ is low and $\overline{W}$ is high. By removing $\overline{CAS}$ output control, pipeline reads are allowed.

To keep the outputs disabled during the $\overline{CAS}$ high time, transition $\overline{W}$ and the EDO outputs are disabled after t_{WEZ}.

During cycles other than Hyper Page Mode read, the outputs are disabled at t_{REZ} after $\overline{RAS}$ is high or t_{CEZ} after $\overline{CAS}$ is high (whichever occurs last), or t_{WEZ} after $\overline{W}$ transitions low.

PIN CONFIGURATION

Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	25	DQ_{12}	49	DQ_{18}
2	DQ_0	26	DQ_{13}	50	DQ_{19}
3	DQ_1	27	DQ_{14}	51	DQ_{20}
4	DQ_2	28	A_7	52	DQ_{21}
5	DQ_3	29	NC	53	DQ_{22}
6	DQ_4	30	V_{CC}	54	DQ_{23}
7	DQ_5	31	A_8	55	NC
8	DQ_6	32	A_9	56	DQ_{24}
9	DQ_7	33	NC	57	DQ_{25}
10	V_{CC}	34	$\overline{RAS}_2$	58	DQ_{26}
11	PD_1	35	DQ_{15}	59	DQ_{28}
12	A_0	36	NC	60	DQ_{27}
13	A_1	37	DQ_{16}	61	V_{CC}
14	A_2	38	DQ_{17}	62	DQ_{29}
15	A_3	39	V_{SS}	63	DQ_{30}
16	A_4	40	$\overline{CAS}_0$	64	DQ_{31}
17	A_5	41	$\overline{CAS}_2$	65	NC
18	A_6	42	$\overline{CAS}_3$	66	PD_2
19	A_{10}	43	$\overline{CAS}_1$	67	PD_3
20	NC	44	$\overline{RAS}_0$	68	PD_4
21	DQ_8	45	NC	69	PD_5
22	DQ_9	46	NC	70	PD_6
23	DQ_{10}	47	$\overline{W}$	71	PD_7
24	DQ_{11}	48	NC	72	V_{SS}

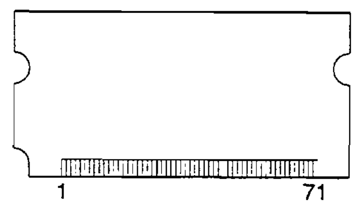
Pin Names

Pin Name	Pin Function
A_0-A_{10}	Address Inputs
DQ_0-DQ_{31}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}_0$, $\overline{RAS}_2$	Row Adress Strobe
$\overline{CAS}_0$-$\overline{CAS}_3$	Column Address Strobe
PD_1-PD_7	Presence Detect
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

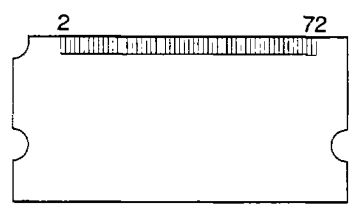
Presence Detect Pins

For 4Mx32 Configuration with 4Mx4, 2K DRAM Components: PD_1=NC, PD_2=NC, PD_3=V_{SS}, PD_4=NC
Speed 60ns: PD_5=NC, PD_6=NC
Normal Refresh: PD_7=NC

Odd numbered pins from pin 1 to pin 71 on front



Even numbered pins from pin 2 to pin 72 on back



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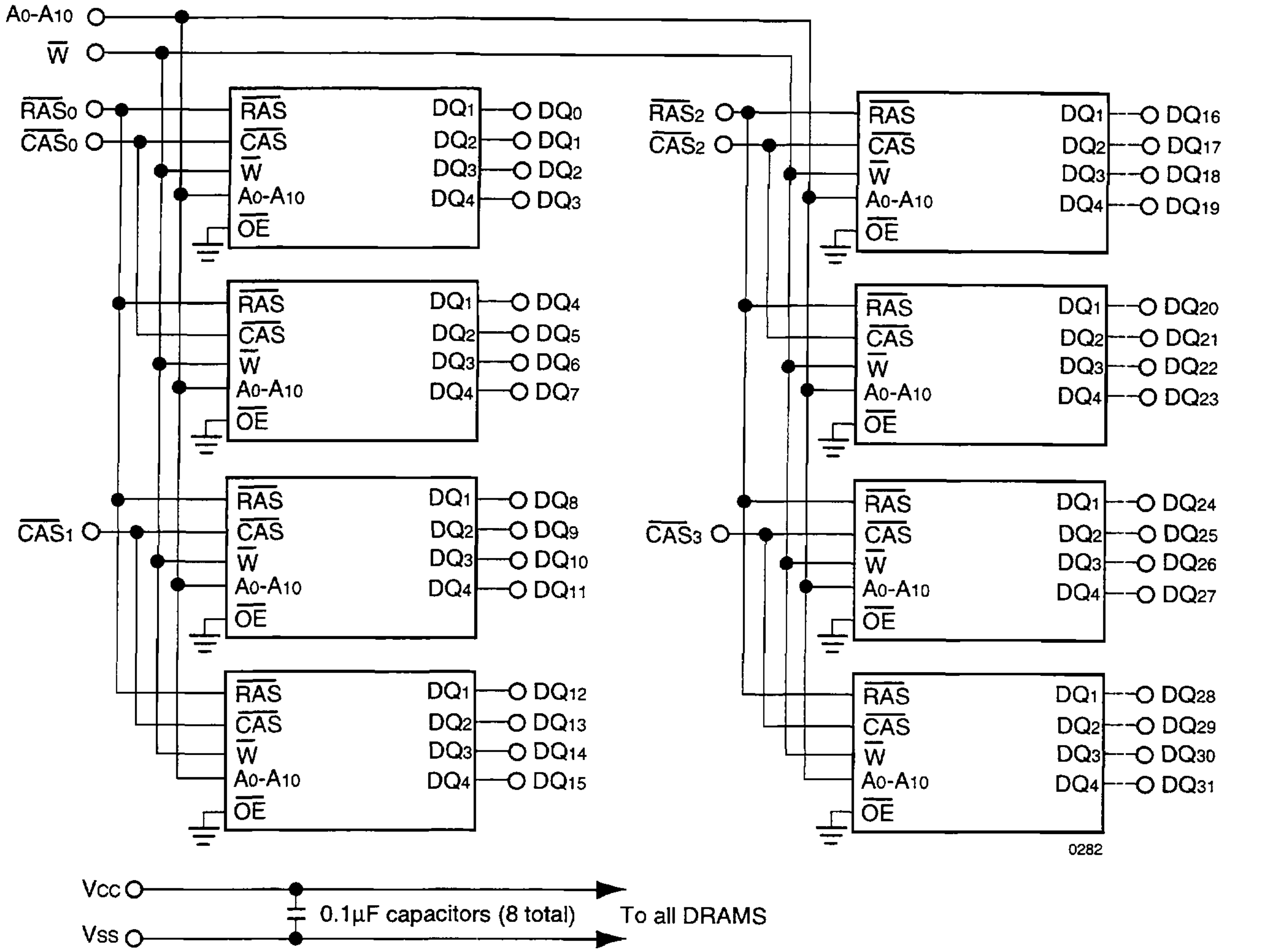
TRUTH TABLE

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	Addresses t_R	Addresses t_C	Data-In/Out DQ_0-DQ_{31}
STANDBY		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	H→L	L	ROW	COL	Data-In
HYPER (EDO)	1st Cycle	L	H→L	H	ROW	COL	Data-Out
PAGE MODE READ	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
HYPER (EDO)	1st Cycle	L	H→L	L	ROW	COL	Data-In
PAGE MODE WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data-In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the oprerational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}+0.3*	V
Input Low Voltage	V_{IL}	-0.3**	—	0.8	V

* V_{CC}+1.3V/15ns. Pulse width is measured at V_{CC}.

** -1.3V/15ns. Pulse width is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC}=min.)	I_{CC1}	—	800	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	I_{CC2}	—	8	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	I_{CC3}	—	800	mA
Hyper (EDO) Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{HPC}=min.)	I_{CC4}	—	800	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	I_{CC5}	—	4	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	I_{CC6}	—	800	mA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.3V, all other pins not under test=0V)	I_{IL}	-40	40	µA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤V_{CC})	I_{OL}	-5	5	µA
Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	—	0.4	V

* I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} are dependent on output loading and cycling rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page mode cycle time, t_{HPC}.

CAPACITANCE (T_A=25 °C, V_{CC}=3.3, f=1MHz)

Item	Symbol	Min	Max	Units
Input Capacitance (A_0-A_{10})	C_{IN1}	—	40	pF
Input Capacitance ($\overline{W}$)	C_{IN2}	—	56	pF
Input Capacitance ($\overline{RAS}_0$, $\overline{RAS}_2$)	C_{IN3}	—	28	pF
Input Capacitance ($\overline{CAS}_0$-$\overline{CAS}_3$)	C_{IN4}	—	14	pF
Input/Output Capacitance (DQ_{0--31})	C_{DQ1}	—	7	pF

AC CHARACTERISTICS (0 °C≤T_A≤70 °C, V_{CC}=3.3V±0.3V, See notes 1, 2)

Parameter	Symbol	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	104		ns	
Read-modify-write cycle time	t_{RWC}	140		ns	
Access time from $\overline{RAS}$	t_{RAC}		60	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15	ns	3,4,5
Access time from column address	t_{AA}		30	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	15	ns	7,12,13
Transition time (rise and fall)	t_T	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		ns	
$\overline{CAS}$ hold time	t_{CSH}	45		ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10,000	ns	14
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	ns	11
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{CRP}	5		ns	
Row address set-up time	t_{ASR}	0		ns	
Row address hold time	t_{RAH}	10		ns	
Column address set-up time	t_{ASC}	0		ns	
Column address hold time	t_{CAH}	10		ns	
Column address hold time ref. to $\overline{RAS}$	t_{AR}	45		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		ns	
Read command set-up time	t_{RCS}	0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		ns	9
Write command set-up time	t_{WCS}	0		ns	8
Write command hold time	t_{WCH}	10		ns	6
Write command hold time ref. to $\overline{RAS}$	t_{WCR}	45		ns	
Write command pulse width	t_{WP}	10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		ns	

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AC CHARACTERISTICS (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Write command to $\overline{CAS}$ lead time	t_{CWL}	10		ns	
Data-in set-up time	t_{DS}	0		ns	10
Data-in hold time	t_{DH}	10		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	45		ns	6
Refresh period	t_{REF}		32	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	34		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	79		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	49		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	54		ns	
$\overline{CAS}$ set-up time (C-B-R refresh)	t_{CSR}	5		ns	
$\overline{CAS}$ hold time (C-B-R refresh)	t_{CHR}	10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge	t_{RPC}	5		ns	
$\overline{CAS}$ precharge (C-B-R counter test)	t_{CPT}	20		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35	ns	3
Hyper page mode cycle time	t_{HPC}	25		ns	14
$\overline{CAS}$ precharge time (hyper page)	t_{CP}	10		ns	
$\overline{RAS}$ pulse width (hyper page)	t_{RASP}	60	200,000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		ns	
$\overline{W}$ to $\overline{RAS}$ precharge (C-B-R refresh)	t_{WRP}	10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time (C-B-R refresh)	t_{WRH}	10		ns	
Output data hold time	t_{DOH}	5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	15	ns	7,12,13
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	15	ns	7,12
$\overline{W}$ to data delay	t_{WED}	15		ns	
$\overline{W}$ pulse width (hyper page)	t_{WPE}	5		ns	

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AC CHARACTERISTICS (continued)

Notes

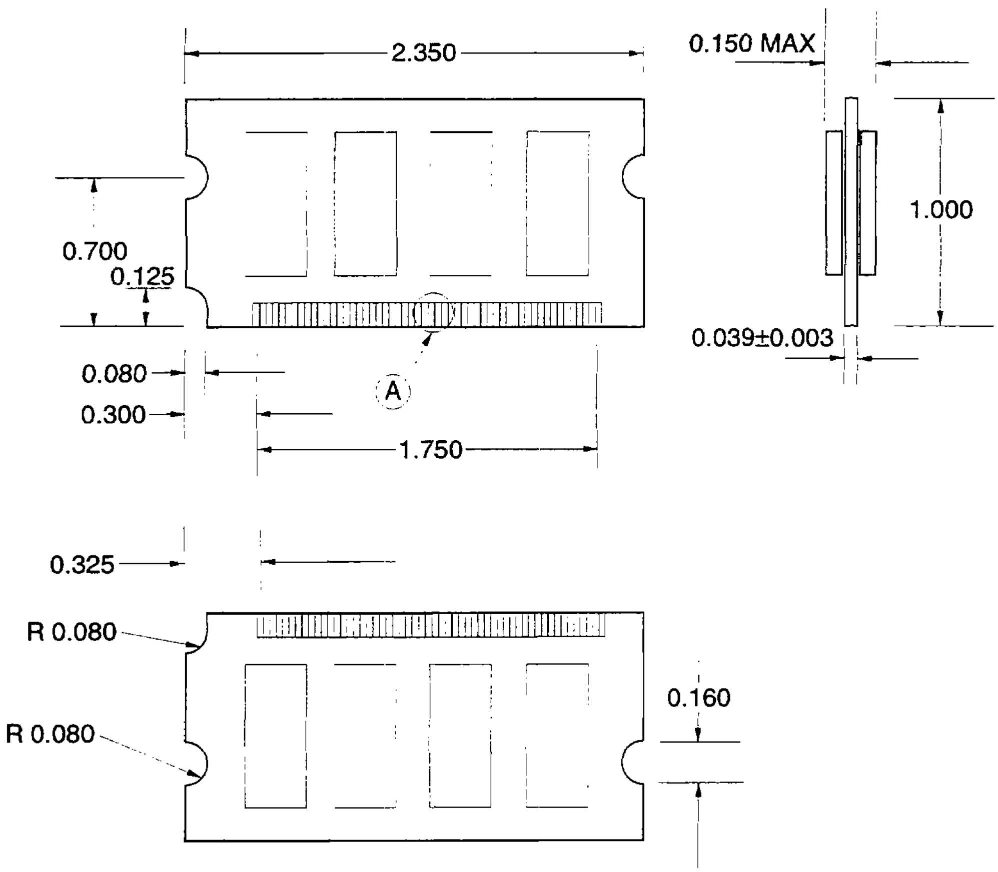
1. An initial pause of 200 µs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 2ns for all inputs.
3. Measure with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes the $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, and t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are non-restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AED(min)}$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ falling edge in early write cycles and to the $\overline{W}$ falling edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. $t_{CEZ(max)}$, $t_{REZ(max)}$, and $t_{WEZ(max)}$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
13. If $\overline{RAS}$ goes high before $\overline{CAS}$ goes high, the open circuit condition of the output is achieved by $\overline{CAS}$ going high. If $\overline{CAS}$ goes high before $\overline{RAS}$ goes high, the open circuit condition of the output is achieved by $\overline{RAS}$ going high.
14. $t_{ASC} \geq t_{CP(min)}$.

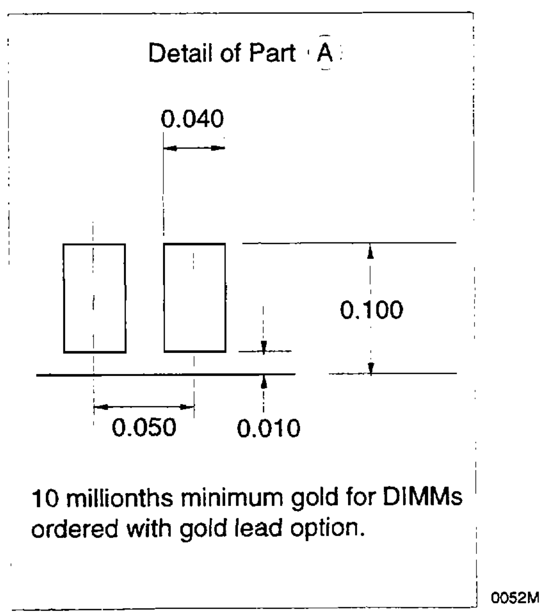
Timing Diagrams

Please refer to attached Timing Chart IV.

PACKAGE DIMENSIONS

Units: Inches





TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED