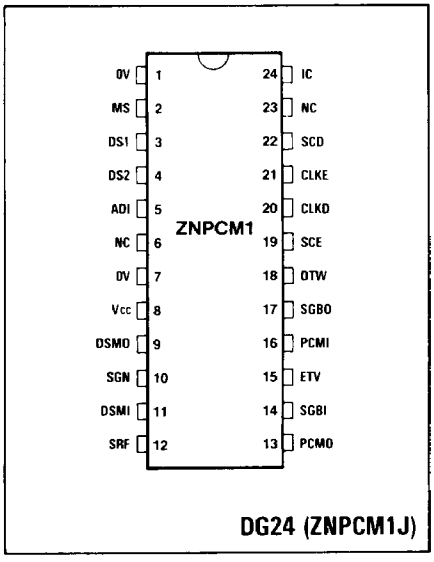
ZNPCM1

SINGLE CHANNEL CODEC

FEATURES

- Converts a Delta-Sigma Modulated Digital Pulse Stream into Compressed 'A'-Law PCM and Vice-Versa.
- Enables Realisation of a Single Channel Codec Circuit with Minimum Component Usage.
- Pin Selectable Input/Output Interface Providing either Single Channel Operation at 64Kbit/s or up to 2048kbit/s for Multi-Channel Operation (2048kHz External Clock).
- Encoder and Decoder can be Clocked Asynchronously (Useful for PCM Multiplex Applications).
- Optional Alternate Digit Inversion.
- Pin and Function Compatible with AY-3-9900.
- Fully TTL Compatible.
- Single 5V Supply.



Pin connections - top view

DESCRIPTION

The ZNPCM1 integrated circuit is the result of a joint development programme with British Telecom. Designed for use in single channel Codec systems, the device accepts a delta-sigma modulated pulse stream at 2048kbit/s (2048kHz external clock) and converts it into 8K sample compressed 'A'-law PCM. In the decode direction, the device performs the reverse function.

A flexible serial PCM input/ouput interface is provided, allowing operation in a single channel mode at 64Kbit/s or at up to 2048kbit/s (2048kHz external clock). for a multi-channel burst format. Digit delay control is provided to compensate for transmission delays.

Optional alternate digit inversion is provided and the encoder and decoder can be clocked asynchronously if required for use in PCM multiplex applications. Designed for use with a 2048kHz system clock, when operated with the required delta-sigma modulator and demodulator, the device performance complies with BT specification RC5549B and CCITT recommendations G711/G712 (1972).

The ZNPCM1 is guaranteed to operate up to 2048kHz and will typically operate up to 4MHz. Operation is from a single 5V power supply, with a typical power dissipation of 400mW.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .. .. +7 Volts
Input Voltage, V_{IN} .. .. +5.5 Volts
Operating Temperature Range .. 0°C to +70°C
Storage Temperature Range .. .. -65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Min.	Nom.	Max.	Unit
Supply Voltage, V_{CC}	4.75	5.0	5.25	V
High-level Output Current, I_{OH}	—	—	-400	μA
Low-level Output Current, I_{OL}	—	—	4	mA
Operating Temperature Range, T_{amb}	0	—	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating temperature range).

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage		2.5	—	—	V
V_{IL}	Low level input voltage		—	—	0.8	V
V_{OH}	High level output voltage	V_{CC} = Min., I_{OH} = Max.	2.4	3.5	—	V
V_{OL}	Low level output voltage	V_{CC} = Min., I_{OL} = Max.	—	—	0.4	V
I_{IH}	High level input current	V_{CC} = Max., V_{IH} = Min.	—	0.2	0.4	mA
I_{IL}	Low level input current	V_{CC} = Max., V_{IL} = Max.	—	-1	-10	μA
I_{CC}	Supply current	V_{CC} = Max.	—	80	110	mA
t_{vw}	Encoder timing vector pulse width		—	488	—	ns
t_{vv}	Encoding timing vector pulse width with edge variation		—	—	100	ns
t_{ww}	Decoder timing waveform pulse width		10	15.6	—	μs
f_{max}	Operating frequency		2.048	4	—	MHz
t_r & t_f	Rise and fall times	0.4V to 3V Transition	5	—	40	ns
t_{pw}	Pulse width	Between 1.5V levels	200	—	—	ns
C_I	Input capacitance		—	—	10	pF

PIN CONFIGURATIONS

Pin	Notation	Comments
1	0V	
2	MS	MODE SELECT (Note 1) Logic 0 = External pcm I/O interface timing Logic 1 = Internal pcm I/O interface timing
3	DS1	DECODER SELECT 1 and 2 (Note 2)
4	DS2	A two bit binary word selects required digit delay between encoder and decoder. DS1 DS2 Digit Delay 0 0 0 0 1 1 1 0 2 1 1 3
5	ADI	ALTERNATE DIGIT INVERSION Logic 0 = No. ADI Logic 1 = ADI
6	N.C.	NO CONNECTION
7	0V	
8	V_{CC}	
9	DSMO	DELTA-SIGMA MODULATED OUTPUT SIGNAL
10	SGN	SIGN BIT OUTPUT Sign bit from the encoder, used to operate on the delta-sigma modulator to reduce d.c. offset effects.
11	DSMI	DELTA-SIGMA MODULATED INPUT
12	SRF	SPECTRAL REDISTRIBUTION FUNCTION Output signal used to operate on the delta-sigma modulator to reduce low frequency quantisation noise.
13	PCMO	PCM OUTPUT
14	SGBI	SIGNALLING BIT INPUT Facility for adding signalling bit(s) to the output pcm stream.
15	ETV	ENCODER TIMING VECTOR A pulse defining the beginning of each frame used to maintain encoder timing.
16	PCMI	PCM INPUT
17	SGBO	SIGNALLING BIT OUTPUT Serial output for extracting signalling bit(s) from the incoming pcm stream.

PIN CONFIGURATIONS *(continued)*

Pin	Notation	Comments
18	DTW	DECODER TIMING WAVEFORM A pulse used to indicate to the decoder when the input pcm stream is in the input register (required only when external shift clocks are used).
19	SCE	ENCODER SHIFT CLOCK Used to control the output of serial pcm data from the encoder (when MS is low).
20	CLKD	DECODER MAIN CLOCK
21	CLKE	ENCODER MAIN CLOCK
22	SCD	DECODER SHIFT CLOCK Used to control the input of the serial pcm data to the decoder (when MS is low).
23	N.C.	NO CONNECTION
24	I.C.	INTERNAL CONNECTION Make no external connection to this pin.

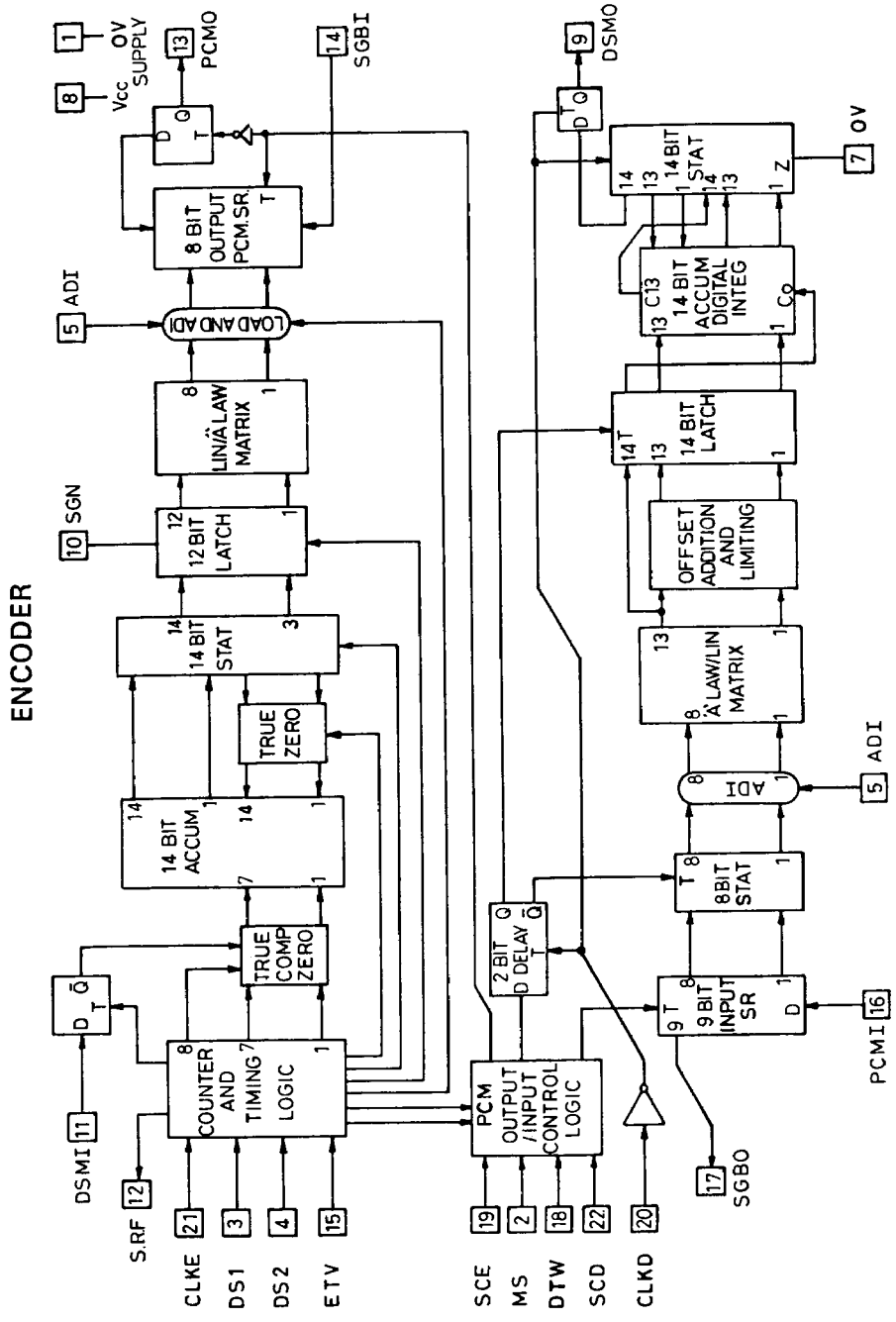
Notes:

1. With MS low (logic 0) serial PCM transmission is under the control of an externally generated shift clock SCE which can vary from 64 kHz to 2,048 kHz. The timing of this input function allows the insertion of a number of signalling bits into the PCM stream via the SGB1 input. In the high (logic 1) state the 8 bit PCM codeword will be transmitted at a rate of 64K bit/sec and each codeword will occupy the full 125 μs frame period with the leading edge of the first bit occurring at a time defined by the ETV pulse.

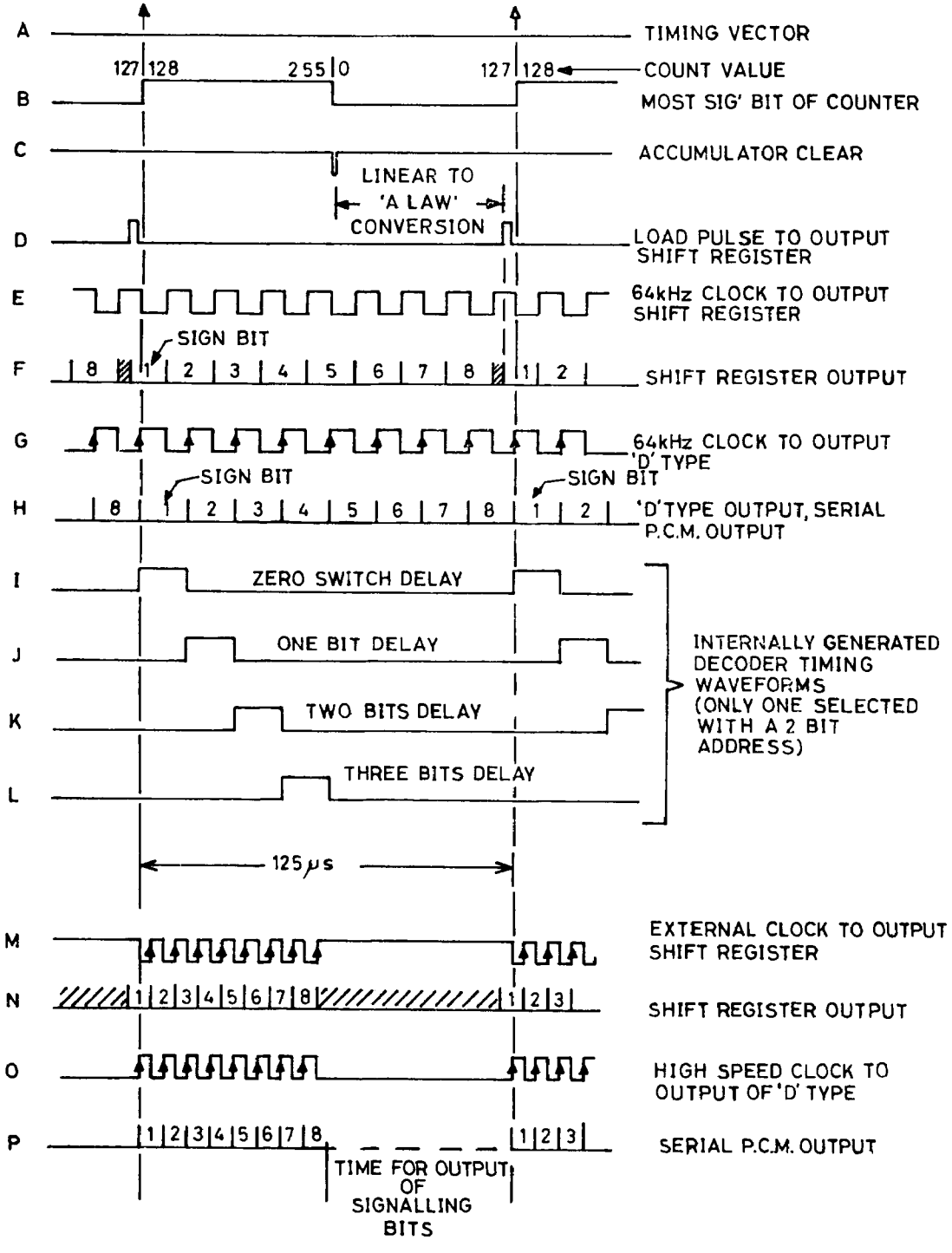
2. Delays through the transmission network, normally under the control of transmission switches, may cause the decoder input pulse stream to be delayed in time by a number of digits from the original transmitted pulse. To compensate for this delay two control inputs, DS1 and DS2, are provided. Consequently when MS is in the high state discrete digit delays of 0 to 3 periods may be selected resulting in a controlled shift of decoder timing in order to re-align Bit 1 in its correct position in the input register.

   When using an externally generated clock (i.e. MS in low state) an input shift clock (SCD) and timing waveform (DTW) are required to ensure that Bit 1 of the input codeword occupies its correct position in the input shift register.

FUNCTIONAL DIAGRAM

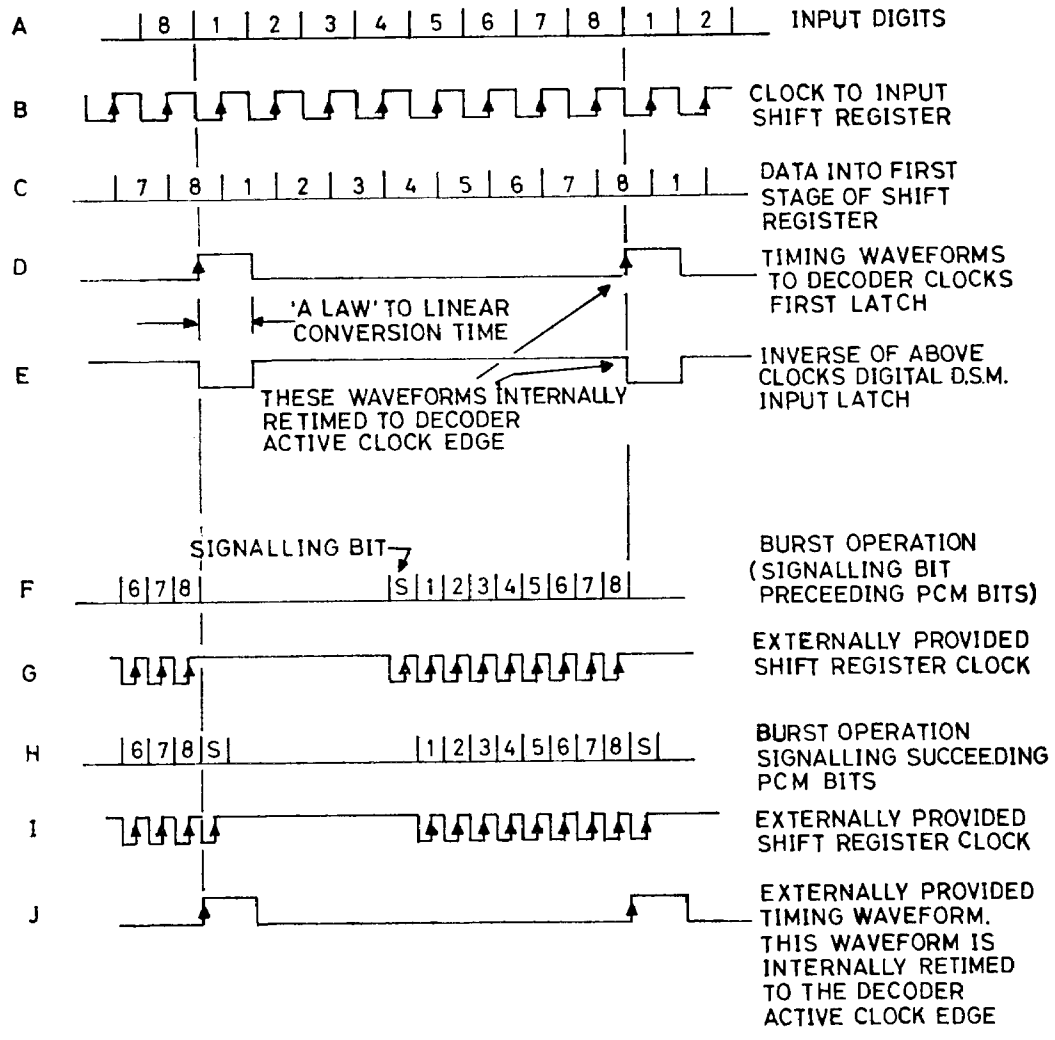


TIMING DIAGRAM
ENCODER



TIMING DIAGRAM

DECODER



APPLICATIONS INFORMATION

(a) A Single Channel Codec

Fig. 1 shows a block diagram of a single channel Codec using the ZNPCM1. The circuit accepts a band limited analogue input signal (300 – 3,400 kHz) and converts it to one bit/sample delta sigma code format at a high sampling rate. The dsm bit stream is then converted by the ZNPCM1 into 8-bit compressed pulse code modulation (pcm) code words at the standard rate of 8K samples/sec, which is then converted into serial format for transmission serially at 64K bit/sec. External timing signals can be used to increase the transmission bit rate to 2,048K bit/sec. to allow for multiplexing in a burst format (see application b).

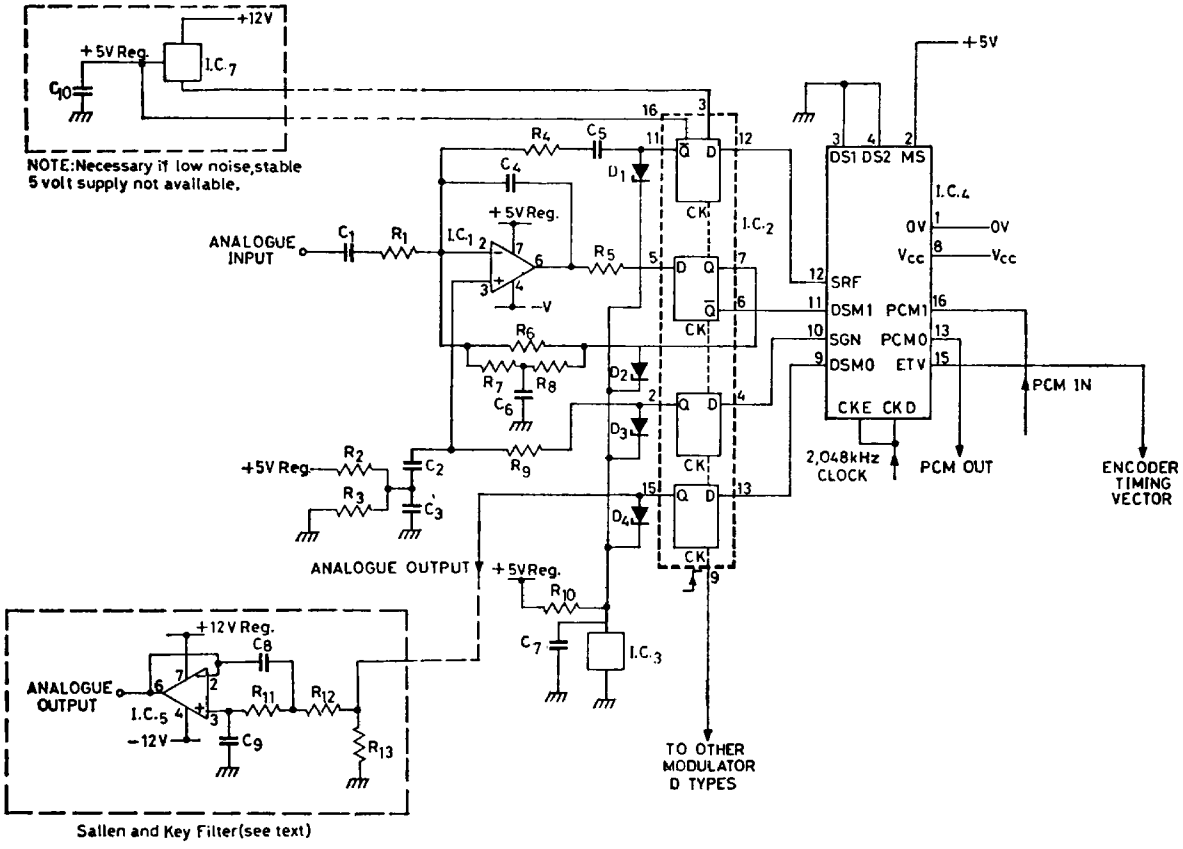


Fig. 1.

The pcm input interface will accept either a 64K bit/sec. bit stream or, by the application of external timing signals, a bit rate of 2,048K bit/sec. in burst format. This is then converted by the ZNPCM1 into a dsm bit stream at 2,048K bit/sec. The dsm demodulator accepts this bit stream and produces one of two precisely defined analogue levels per single bit sample. The analogue waveform can then be recovered via a low pass filter, cutting off just above the highest signal frequency to be recovered (3.4 kHz).

Output voltages of the dsm circuit are stabilised by supplying the quad D-type from a 5 volt regulator, which is always associated with the Codec, and clamping the high state output voltages to a 2.45V reference by the use of Schottky diodes. These also help to match the voltages influencing the d.c. alignment conditions and minimise the effects of power supply variations and noise. Resistor ratio stability is obtained, along with a small modulator/demodualtor physical size by implementing the resistors and small capacitors as an in-line hybrid. More details of the operation of the dsm circuit are outlined in the Plessey brochure 'A Single Channel Codec'.

An interesting development, again in co-operation with British Telecom, is the integrated circuit dsm solution, the ZNPCM2. This will reduce the circuitry surrounding the ZNPCM1 to a single I.C. and seven capacitors.

The Codec performance related to CCITT criteria is outlined in Fig.2.

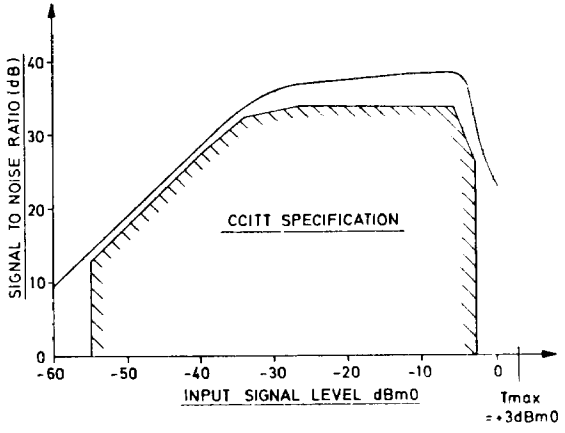


Fig. 2.

(b) A 30 Channel PCM Codec Solution

Traditionally the code conversion process on branch-to-main telephone exchange systems has been performed using multiplexed codecs. Historically the reason for this has been the codec specification where the signal-to-noise and gain-linearity constraints imposed on the systems have resulted in the use of expensive hybrid codecs. It might seem immediately obvious that the use of single channel codecs offers a more attractive solution, however a comparison of one of the major performance criteria is first of all necessary, that of power dissipation. Indeed, an initial comparison using the conventional 30 Channel PCM system shows the single channel codec approach to disadvantage. However, a more detailed analysis, using the single channel codecs in a power switching mode, shows this technique to be compatible with time shared codecs. This is described in section (d).

Let us first of all consider the system approach for using the single channel codecs in a 30 channel PCM system by looking at Fig.3.

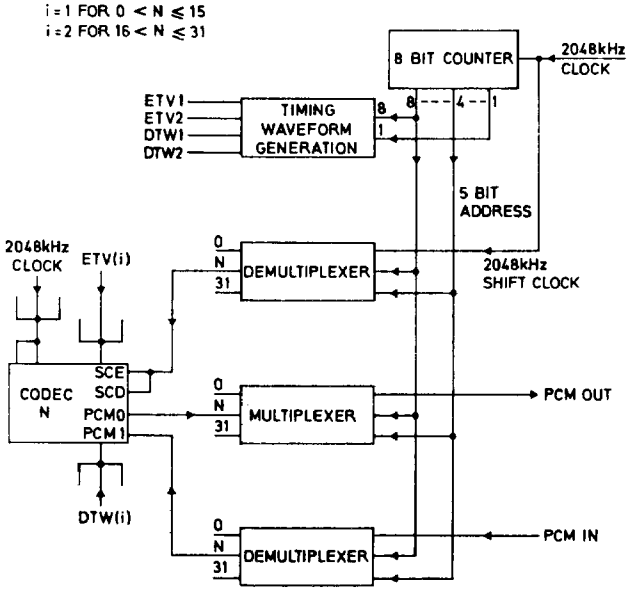


Fig. 3.

Fig. 3 shows how a 32 time slot (Note: A 30 Channel system has in fact, 32 time slots, the two additional ones being for signalling notation and synchronisation), 2,048K bit/sec. multiplex can be formed and decoded using 30 single channel codecs, when the two directions of transmission operate synchronously. Only the Nth codec is shown, connected to the 'Nth' port of the 32 port multiplexer and demultiplexers. When the 5-bit address equals N the 2,048 kHz shift clock is routed through the 'Nth' codec for eight clock pulses as shown in Fig. 4(a). The shift-in and shift-out clock terminals of the codec are commoned together. Since the shift-out terminal uses a negative active clock edge and the shift-in terminal uses a positive active clock edge the pcm digits for the two directions may be in exact time alignment. This is compatible with using the same 5-bit address for the multiplexer and the other demultiplexer.

The Encoder Timing Vector (ETV) and the Decoder Timing Waveform (DTW) may be derived from a counter driven by the 2,048 kHz clock and commoned across a number of codecs. For a 32 time slot multiplex, two sets of ETV's and DTW's should be generated with a half frame displacement as shown in Figs. 4(b) and 4(c). The first pair will supply ports 0 to 15 and the second pair ports 16 to 31, and consequently allowing the shift activity to be kept well clear of the timing waveforms for a given codec.

For a conventional 32 time slot codec ports 0 and 16 correspond to the synchronisation and signalling channels respectively.

Fig. 5 shows a similar arrangement for generating and decoding a 32 time slot multiplex when the two directions of transmission operate asynchronously. The two directions are operated quite independently but using similar principals to those previously discussed. It should again be noted that two sets of ETV's and DTW's should be used.

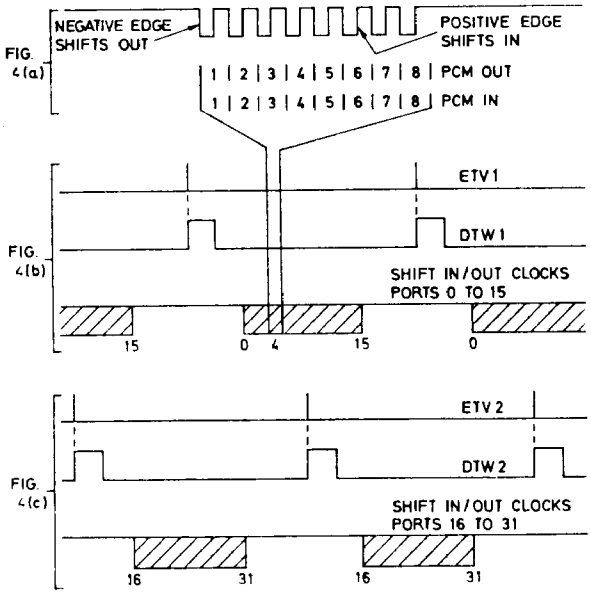


FIG. 4(a)
NEGATIVE EDGE SHIFTS OUT
POSITIVE EDGE SHIFTS IN
1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | PCM OUT
1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | PCM IN
FIG. 4(b)
ETV1
DTW1
SHIFT IN/OUT CLOCKS PORTS 0 TO 15
15
0 4
15
0
FIG. 4(c)
ETV2
DTW2
SHIFT IN/OUT CLOCKS PORTS 16 TO 31
16
31
16
31

Fig. 4.

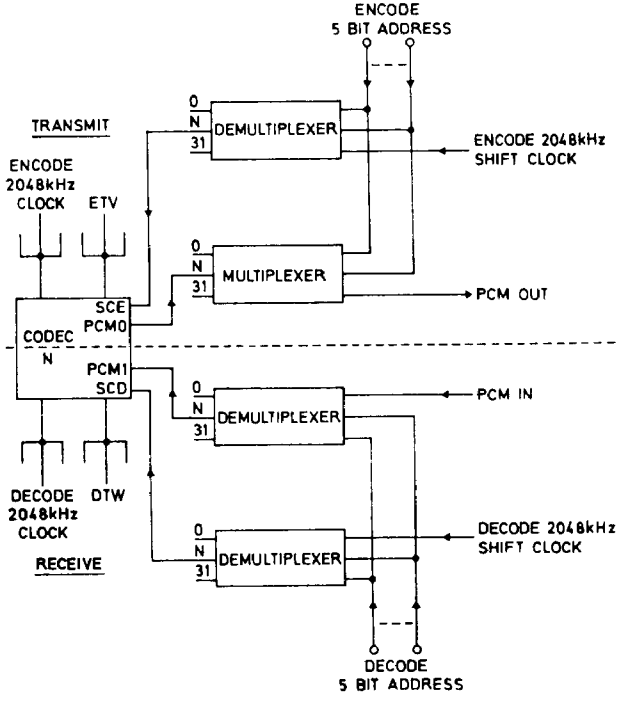

ENCODE 5 BIT ADDRESS
TRANSMIT
ENCODE 2048kHz CLOCK
ETV
0
N
31
DEMULTIPLEXER
ENCODE 2048kHz SHIFT CLOCK
MULTIPLEXER
PCM OUT
SCE
PCM0
CODEC
N
PCM1
SCD
PCM IN
DECODE 2048kHz CLOCK
DTW
RECEIVE
DECODE 2048kHz SHIFT CLOCK
DECODE 5 BIT ADDRESS

Fig. 5.

(c) Switching Applications

The ZNPCM1 can be used in a variety of ways to satisfy switching applications. One technique is to operate directly on the 2,048K bit/s digit stream produced by the circuit arrangement shown in Fig. 3, where each codec has a defined time slot in the bit stream. An alternative technique would be to derive the address applied to the multiplexer and demultiplexer from the contents of a random access memory (RAM) which defines the codec to be used in a given time slot, in an exchange of PCM codewords between the codec and an intermediate store. In this mode of use the codec interface is effectively used as a time switch store.

The circuit shown in Fig 5 can be used without an intermediate store where again the codec addresses are derived from RAM's. The encode address defines the 'source' and the decode address the 'sink' in a given time slot. The decode address may be delayed with respect to the encode address by an integer number of 2,048 kHz clock periods to take account of any small fixed switching delay.

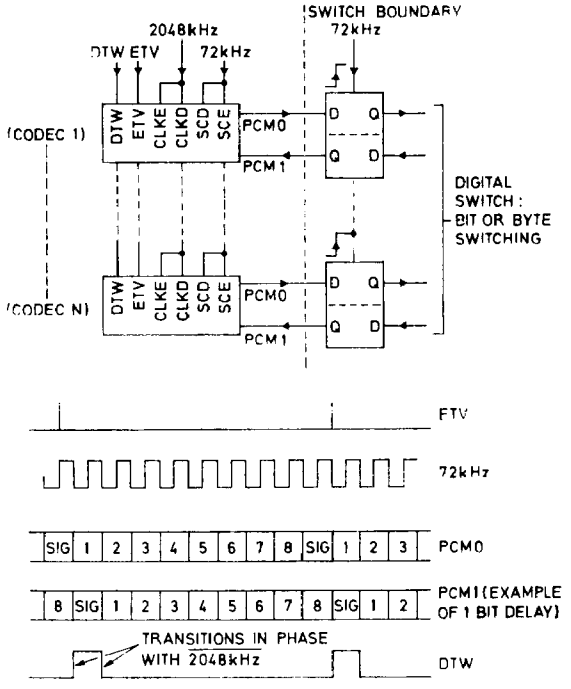


Fig. 6.

Fig. 6 shows an arrangement where the codecs input and output continuously, allowing 9-bits (8 PCM plus 1 signalling) to be exchanged in each 125 μs sample period. All the codecs may be supplied with common ETV, DTW, 2,048 kHz and 72 kHz waveforms. Each bit is retimed in the digital switch using a latch.

The digital switch may be operated using a bit switching arrangement, combined with the extraction and insertion of the signalling bits. Alternatively the bits may be reformatted into bytes and then byte switching performed. If the signalling is handled separately to the pcm codewords then a 64K bit/s rate can be used to and from the codec. This is compatible with using the codecs internal clock mode (MS = 1) in which case the only common timing waveforms required at the codec are the 2,048 kHz clock and the ETV.

(d) Power Switching

Comparisons have previously been made between shared and single channel codecs where these comparisions were reduced to one of power dissipation. Considerable power savings can be made by using the codecs in such a mode that they are only powered-up when required for use.

It is interesting to compare the power dissipation of an eight channel system using in one case eight ZNPCM1s in a power switching mode and, in the other case, one of the more popular time shared codecs which caters for eight channels. One single channel codec dissipates 600 mW and the time shared codec dissipates 1500 mW.

If the channel occupancy is p, then the average power dissipation per channel for the time shared codec is given by

$$W_{TS} = 1 - (1-p)^8 \frac{1500}{8} \text{ mW}$$

This assumes the time shared codec is only powered-up when any of the eight channels are required for use.

The average power dissipation per channel using the single channel codecs is simply given by

$$W_{SC} = p.600 \text{ mW}$$

Fig. 7 shows a plot of power dissipation versus channel occupancy ; p for both approaches. The busy period average channel occupancies are likely to be in the range 0.2 to 0.15, clearly the lower end of the curves. Taking a figure of p = 0.06, for example, then the single channel codec dissipates only 36 mW per channel, approximately 50% less than the time shared codec. As the graph shows even for very busy exchanges given values for p of up to 0.3 shows the ZNPCM1 system to dissipate less power.

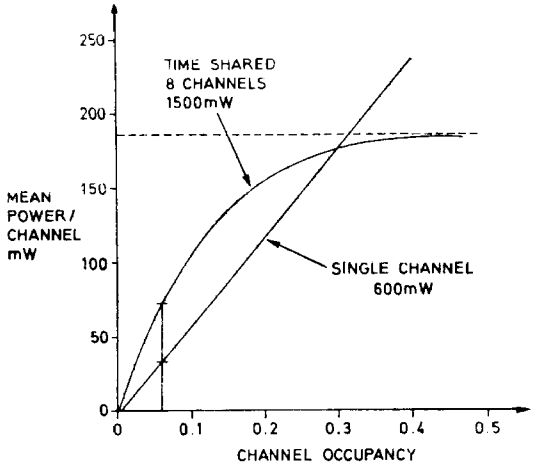


Fig. 7.