



PRODUCT OVERVIEW

DATEL's ADSD-1402S is a functionally complete, dual 14-bit, 2MSPS, sampling A/D converter. Its standard, 40-pin, triple-wide SMT DIP contains two fast-settling sample/hold amplifiers, two 14-bit A/D converters, multiplexed output buffers, a precision reference, and all the timing and control logic necessary to operate from either two or a single start convert pulse.

The ADSD-1402S is optimized for wideband frequencydomain applications and is fully FFT tested. The ADSD-1402S requires only $\pm 5V$ supplies and typically consumes 0.6 Watts. Models are available in either commercial 0 to $+70^{\circ}C$ or military -55 to $+125^{\circ}C$ (-EX suffix model) operating temperature ranges.

FEATURES

- 14-bit resolution; 2MSPS sampling rate
- Functionally complete; $\pm 5V$ input range
- No missing codes over full temperature range
- Edge-triggered; No pipeline delays
- $\pm 5V$ supplies, 0.6 Watts
- Small, 40-pin, low-cost surface-mount TDIP
- 79dB SNR, $-80dB$ THD
- Ideal for both time and frequency domain applications
- Out-of-range indicator

INPUT/OUTPUT CONNECTIONS			
PIN	FUNCTION	PIN	FUNCTION
1	INPUT A	40	INPUT B
2	+5VA	39	+5VA
3	ANALOG GROUND	38	ANALOG GROUND
4	GAIN A	37	GAIN B
5	OFFSET A	36	OFFSET B
6	RANGE	35	N/C
7	2.5V REF	34	N/C
8	ANALOG GROUND	33	ANALOG GROUND
9	-5V	32	-5V
10	ENABLE A	31	ENABLE B
11	START A	30	START B
12	+5VD	29	EOC
13	BIT 14 (LSB)	28	BIT 1 (MSB)
14	BIT 13	27	BIT 2
15	BIT 12	26	BIT 3
16	BIT 11	25	BIT 4
17	BIT 10	24	BIT 5
18	BIT 9	23	BIT 6
19	BIT 8	22	BIT 7
20	DGND	21	DGND

BLOCK DIAGRAM

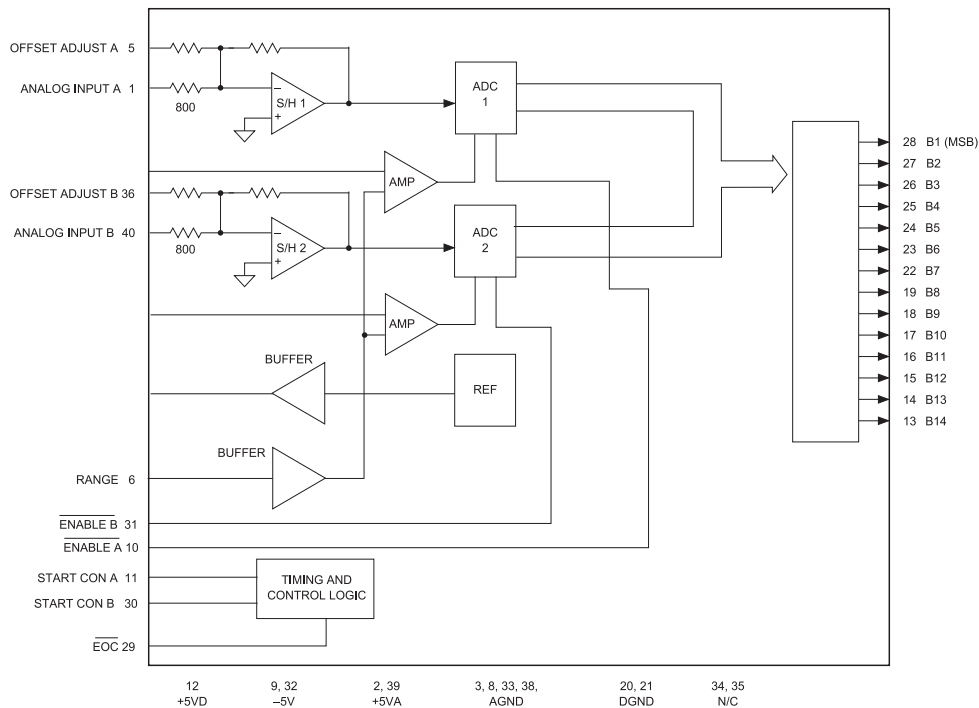


Figure 1. ADSD-1402S Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS		
PARAMETERS	LIMITS	UNITS
+5V Supply (Pins 2, 12, 39)	0 to +6	Volts
-5V Supply (Pins 9, 32)	0 to -6	Volts
Digital Inputs (Pins 3, 10, 11, 31)	-0.3 to +VDD +0.3	Volts
Analog Input (Pins 1, 40)	±5	Volts
Lead Temp. (10 seconds)	+300	°C

FUNCTIONAL SPECIFICATIONS

(TA = +25°C, +VDD = +5V, Vee = -5V, 2MSPS sampling rate, Vin = ±5V and a minimum 7 minute warmup unless otherwise specified.)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range	—	±5V	—	Volts
Input Impedance	—	400	—	Ω
Input Capacitance	—	7	15	pF
DIGITAL INPUTS				
Logic Levels				
Logic "1"	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	μA
Logic Loading "0"	—	—	-20	μA
PERFORMANCE				
Integral Non-Linearity (fin = 10KHz)				
+25°C	—	±1	—	LSB
0 to +70°C	—	±1	—	LSB
-55 to +125°C	—	±2	—	LSB
Differential Non-Linearity (fin = 10KHz)				
+25°C	-0.99	±0.5	+1.75	LSB
0 to +70°C	-0.99	±0.5	+2.5	LSB
-55 to +125°C	-0.99	±0.75	+2.5	LSB
Offset Error				
+25°C (see Figure 3)	—	±0.25	±0.5	%FSR
0 to +70°C	—	±0.25	±0.5	%FSR
-55 to +125°C	—	±0.5	±0.8	%FSR
Gain Error				
+25°C (see Figure 3)	—	±0.3	±0.6	%FSR
0 to +70°C	—	±0.3	±0.6	%FSR
-55 to +125°C	—	±0.6	±0.8	%FSR
No Missing Codes (fin = 975kHz)				
14 Bits	-55 to +125°C			
Resolution	14 Bits			
OUTPUTS				
Output Coding	Offset Bin.			
Logic Level				
Logic "1"	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	Volts
Logic Loading "1"	—	—	4	μA
Logic Loading "0"	—	—	4	mA
Internal Reference				
Voltage, +25°C	+2.45	+2.5	+2.55	Volts
0 to +70°C	+2.45	+2.5	+2.55	Volts
External Current	—	—	5	mA

DYNAMIC PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Total Harm. Distort. (-0.5dB)				
dc to 500kHz	—	-79	-72	dB
500kHz to 1MHz	—	-73	-70	dB
Signal-to-Noise Ratio (w/o distortion, -0.5dB)				
dc to 500kHz	76	80	—	dB
500kHz to 1MHz	76	80	—	dB
Signal-to-Noise Ratio (and distortion, -0.5dB)				
dc to 500kHz	70	74	—	dB
500kHz to 1MHz	69	73	—	dB
Spurious Free Dyn. Range ①				
dc to 500kHz	—	-85	-74	dB
500kHz to 1MHz	—	-74	-70	dB
Two-tone IMD Distortion (fin = 975kHz, fs = 2.0MHz, -0.5dB)				
Input Bandwidth (-3dB)	—	-76	—	dB
Small Signal (-20dB input)				
Large Signal (-0.5dB input)	—	16	—	MHz
Slew Rate	—	±250	—	V/μs
Aperture Delay Time	—	—	±10	ns
Aperature Uncertainty	—	—	5	ps
S/HAquisition Time(to±0.003%FSR), stepinput	—	100	150	ns
Conversion Rate	2	—	—	MHz
Feedthrough Rejection (fin = 1MHz)	—	85	—	dB
Noise	—	250	—	μVrms
POWER REQUIREMENTS				
Power Supply Ranges				
-5V Supply	-5.25	-5	-4.75	Volts
+5V Supply	+4.75	+5.0	+5.25	Volts
Power Supply Currents				
-5V Supply	-80	-70	—	mA
+5V Supply	—	+50	+70	mA
Power Dissipation	—	0.6	0.75	Watts
Power Supply Rejection	—	—	±0.01	%FSR%
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range, Case				
ADSD-1402SMC	0	—	+70	°C
ADSD-1402SMM	-55	—	+125	°C
Storage Temperature Range	-65	—	+150	°C
Weight	16.1/0.6			grams/oz
Package Type	0-pin, SMT TDIP			

Footnote:

① Same specification as In-Band Harmonics and Peak Harmonics.

TECHNICAL NOTES

1. Rated performance requires using good high-frequency circuit board layout techniques. Connect the digital and analog grounds to one point, the analog ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

INPUT RANGE	OFFSET ADJUST +1/2 LSB	GAIN ADJUST FS - 1/2 LSB
±5V	+0.000305V	+4.999085V

Table 2. Offset and Gain Adjustments

Adjust the gain trimpot R1 until the output code flickers equally between 11 1111 1111 1110 and 11 1111 1111 1111.

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3. Apply a pulse of 100 nanoseconds minimum to START CONVERT (pin 11) at a rate of 200kHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero (Offset) Adjustments

Apply a precision voltage reference source between ANALOG INPUT A (pin 1) and SIGNAL GROUND (pin 3), then adjust the reference source output per Table 2. Adjust trimpot R2 until the code flickers equally between 10 0000 0000 0000 and 10 0000 0000 0001.

3. Full-Scale (Gain) Adjustments

Set the output of the voltage reference used in step 2 to the value shown in Table 2.

4. Repeat above steps for Analog Input B (Pin 40). Use trimpot R3 for the zero (Offset) adjustment and trimpot R4 for the Full-Scale (Gain) adjustment.
5. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 3.

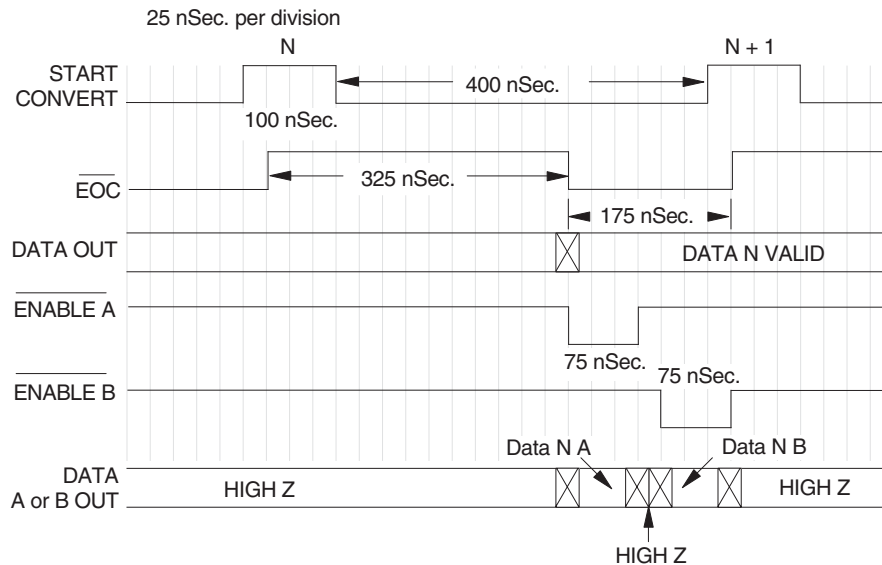
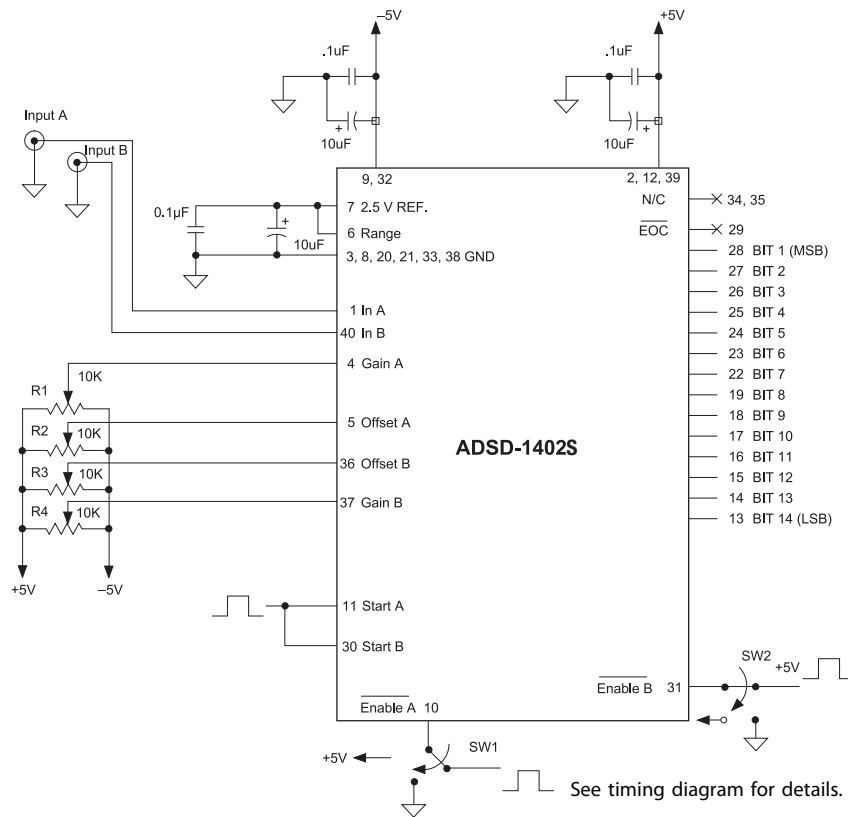


Figure 2. ADSD-1402S Timing Diagram

OUTPUT CODING		INPUT RANGE	BIPOLAR SCALE
MSB	LSB	±5V	
11	1111 1111	+4.999390	+FS - 1LSB
11	1000 0000	+4.250000	+3/4FS
11	0000 0000	+2.500000	+1/2FS
10	0000 0000	±0.000000	0
01	0000 0000	-2.500000	-1/2FS
00	1000 0000	-4.250000	-3/4FS
00	0000 0001	-4.999390	-FS+1LSB
00	0000 0000	-5.000000	-FS

Table 3. Output Coding



Notes:

- ① Recommended to use same supply source for +5 Analog and +5 Digital. Try using as clean of a supply as possible (Bypass caps., 10uF and .1uF).
- ② Outputs are enabled by either turning $\overline{\text{ENABLE A}}$ (Pin 10) or $\overline{\text{ENABLE B}}$ (Pin 31) low for prespective analog inputs A or B. A high on $\overline{\text{ENABLE A}}$ or $\overline{\text{ENABLE B}}$ results in disabling the output bus (High Z).

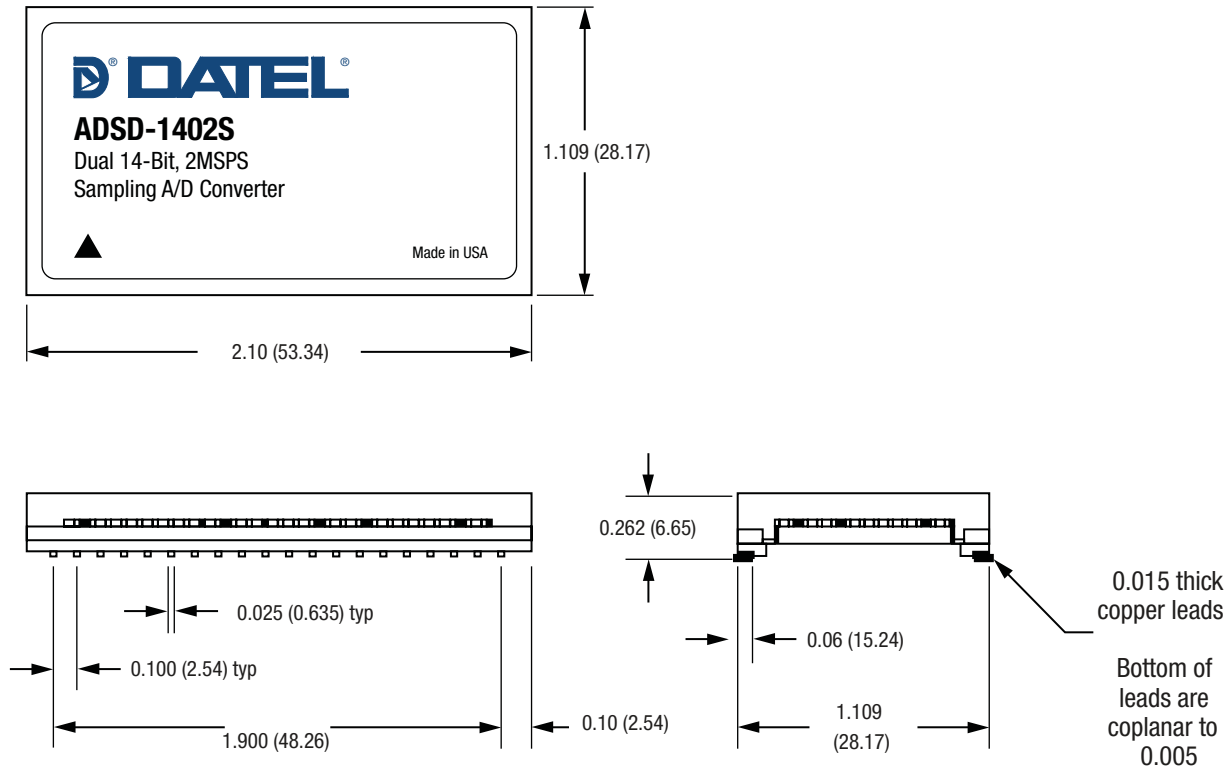
Figure 3. ADSD-1402S Connection Diagram

THERMAL REQUIREMENTS

The ADSD-1402S sampling A/D converter is fully characterized and specified over the commercial operating temperature (ambient) range of 0 to +70°C and military temperature range of -55 to +125°C (EX suffix). All room-temperature (TA = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables. These devices do not normally require heat sinks, however, standard precautionary design and layout procedures

should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package. Devices should be soldered to boards rather than "socketed", and of course, minimal air flow over the surface can greatly help reduce the package temperature.

MECHANICAL DIMENSIONS - INCHES (mm)



ORDERING INFORMATION					
MODEL NUMBER	OPERATING TEMP. RANGE	PACKAGE	ROHS	ACCESSORIES	
ADSD-1402S	0 to +70°C	SMT-TDIP	No	HS-40	Heat Sink for all ADSD-1402S models
ADSD-1402S-EX	-55to +125°C	SMT-TDIP	No		
ADSD-1402S-C	0 to +70°C	SMT-TDIP	Yes		
ADSD-1402S-EX-C	-55to +125°C	SMT-TDIP	Yes		

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