NMB Semiconductor

AAA1M200 Fast Page Mode CMOS 1M × 1 Dynamic RAM

PRELIMINARY

FEATURES

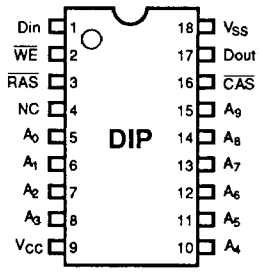
- 1,048,576 × 1 bit Organization
- Single 5V ±10% Power Supply
- Performance Ranges:

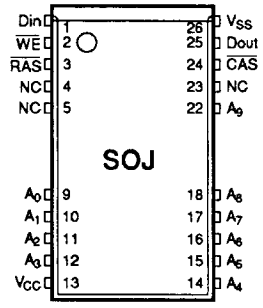
Parameter	-06	-07	-08	-10
Max. $\overline{RAS}$ Access Time	60ns	70ns	80ns	100ns
Max. $\overline{CAS}$ Access Time	15ns	20ns	20ns	25ns
Max. Column Address Access Time	30ns	35ns	40ns	50ns
Min. Read/Write Cycle Time	110ns	130ns	150ns	190ns

- Fast page mode operation
- Low Power Operation
  - Standby current (CMOS) 2mA
  - Operating current 75mA
- 512 Refresh cycles distributed across 8ms
- All input and output clocks are fully TTL and CMOS compatible
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$ and hidden refresh
- High reliability plastic 18 pin 300 mil wide DIP, plastic 26pin SOJ, and plastic 20pin ZIP.

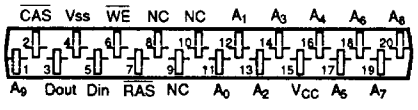
PIN CONFIGURATIONS

(TOP VIEWS)





ZIP



DESCRIPTION

The AAA1M200 is a high speed, 1,048,576 × 1 bit CMOS Dynamic Random Access Memory. Fabricated with leading edge CMOS technology, the AAA1M200 offers a combination of features unattainable with NMOS technolgy, namely, speed, power and inherently high CMOS reliability.

The AAA1M200, with its fast page mode operation can allow random or sequential access of up to 1,024 bits within a row with cycle times as fast as 40ns. Because of static circuitry, the $\overline{CAS}$ clock is no longer in the critical timing path.

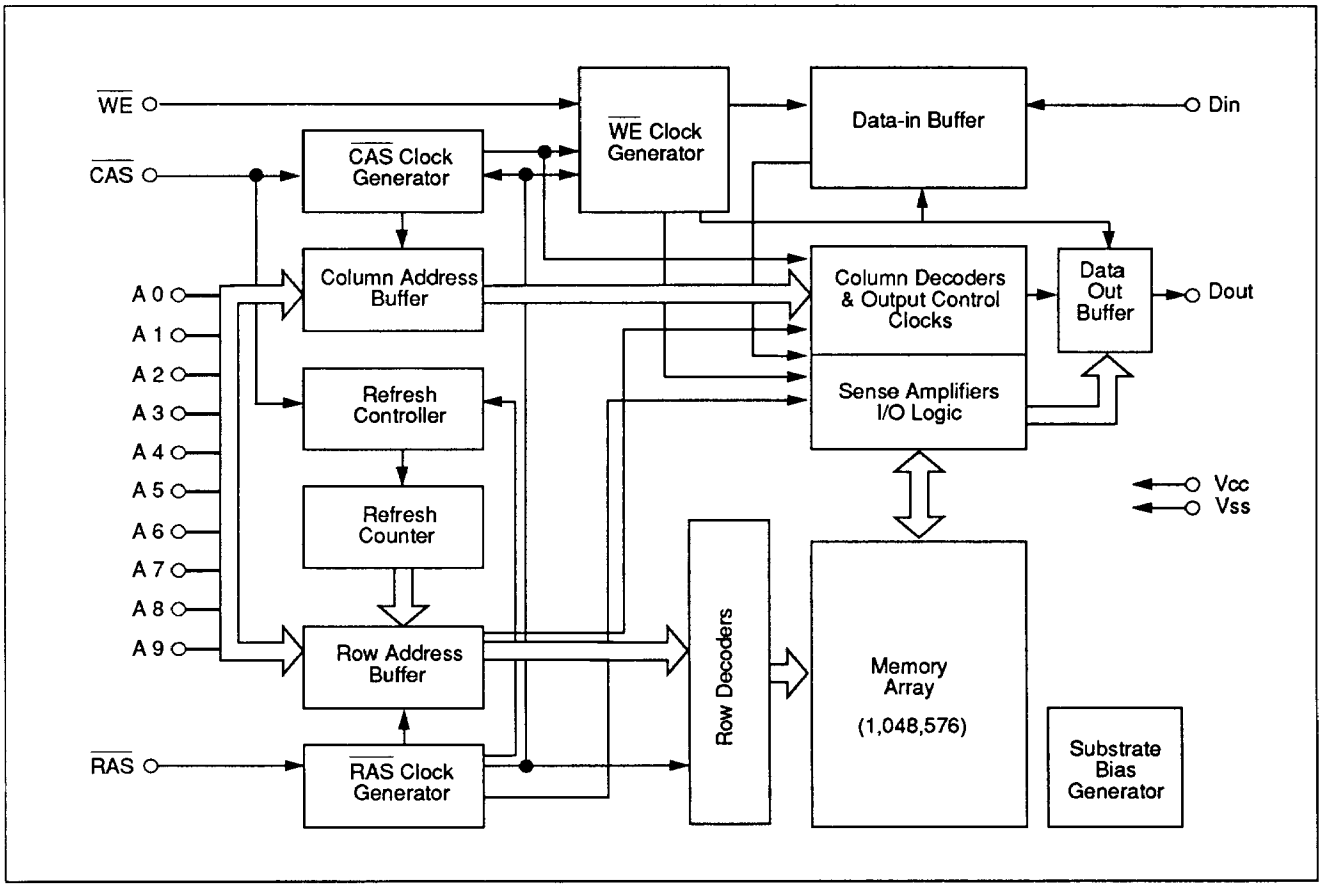
The flow-through column address latch allows address pipelining while relaxing many critical system timing requirements for fast speed.

Multiplexed address inputs permit AAA1M200 to be packaged in a standard 18-pin plastic DIP, 26-pin plastic SOJ and 20-pin plastic ZIP. The package sizes provide high system densities and are compatible with widely available automated testing and insertion equipment. System level features include single power supply of 5V ±10% tolerance and direct interface with high performance TTL logic families.

PIN NAMES

A0~A9	Address Inputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
Din	Data Input
Dout	Data Output
$\overline{WE}$	Write Enable
Vcc	+5V Supply
Vss	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
Voltage on Any Pin Relative to V_{SS}	Vin,Vout	–1 to 7	V
Voltage on Vcc Relative to V_{SS}	V_{CC}	–1 to 7	V
Storage Temperature (Plastic)	Tstg	–55 to 125	°C
Power Dissipation	Pd	600	mW
Ambient Operating Temperature	Ta	0 to +70	°C

* Permanent device damage can occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

DC OPERATING CONDITION

SYMBOL	PARAMETER	MIN.	NOM	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage		0		V
V_{IH}	Input High Voltage, All Inputs	2.4		6.5	V
V_{IL}	Input Low Voltage, All Inputs	–1.0		0.8	V

Note: All voltage values in this data sheet are with respect to V_{SS}.

DC ELECTRICAL CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	SPEED	MIN.	MAX.	UNIT	TEST CONDITIONS	NOTE
I_{CC1}	Average V_{CC} Power Supply Current (Operating)	-06 -07 -08 -10		90 90 90 75	mA mA mA mA	t_{RC} = t_{RC} (min.) $\overline{RAS}$, $\overline{CAS}$, Address Cycling	1, 2
I_{CC2}	V_{CC} Supply Current (TTL standby)			3	mA	$\overline{RAS}$ and $\overline{CAS}$ at V_{IH}. All Other Inputs ≥ V_{SS}	
I_{CC3}	V_{CC} Supply Current ($\overline{RAS}$ only refresh)	-06 -07 -08 -10		90 90 90 75	mA mA mA mA	t_{RC} = t_{RC} (min.) $\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}	1
I_{CC4}	V_{CC} Supply Current (Fast page mode)	-06 -07 -08 -10		70 70 70 55	mA mA mA mA	t_{PC} = t_{PC} (min.) $\overline{RAS}$ = V_{IL} $\overline{CAS}$, Address Cycling	1, 2
I_{CC5}	V_{CC} Supply Current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	-06 -07 -08 -10		90 90 90 75	mA mA mA mA	t_{RC} = t_{RC} (min.) $\overline{RAS}$, $\overline{CAS}$ Cycling	1
I_{CC6}	V_{CC} Supply Current (CMOS standby)			2	mA	$\overline{RAS}$ ≥ V_{CC}-0.2V and $\overline{CAS}$ at V_{IH} All Other Inputs ≥ V_{SS}	
$I_{I(L)}$	Input Leakage Current (Any input pin)		-10	10	µA	0V ≤ V_{IN} ≤ V_{CC}, Others = 0V	
$I_{O(L)}$	Output Leakage Current (For high impedance state)		-10	10	µA	$\overline{RAS}$ at V_{IH}, $\overline{CAS}$ at V_{IH} 0V ≤ V_{OUT} ≤ V_{CC}	
V_{OH}	Output High Voltage		2.4		V	I_{OH} = –5.0 mA	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.2 mA	

Notes: 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.

CAPACITANCE (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{IN}	Address, D_{IN}	—	5	pF
C_{IN}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	—	7	pF
C_{OUT}	Output Capacitance	—	7	pF

A.C. OPERATING CONDITIONS ($0°C \leq Ta \leq 70°C$, $V_{CC} = 5\ V \pm 10\%$, $V_{SS} = 0\ V$) (NOTES 3, 4, 5)

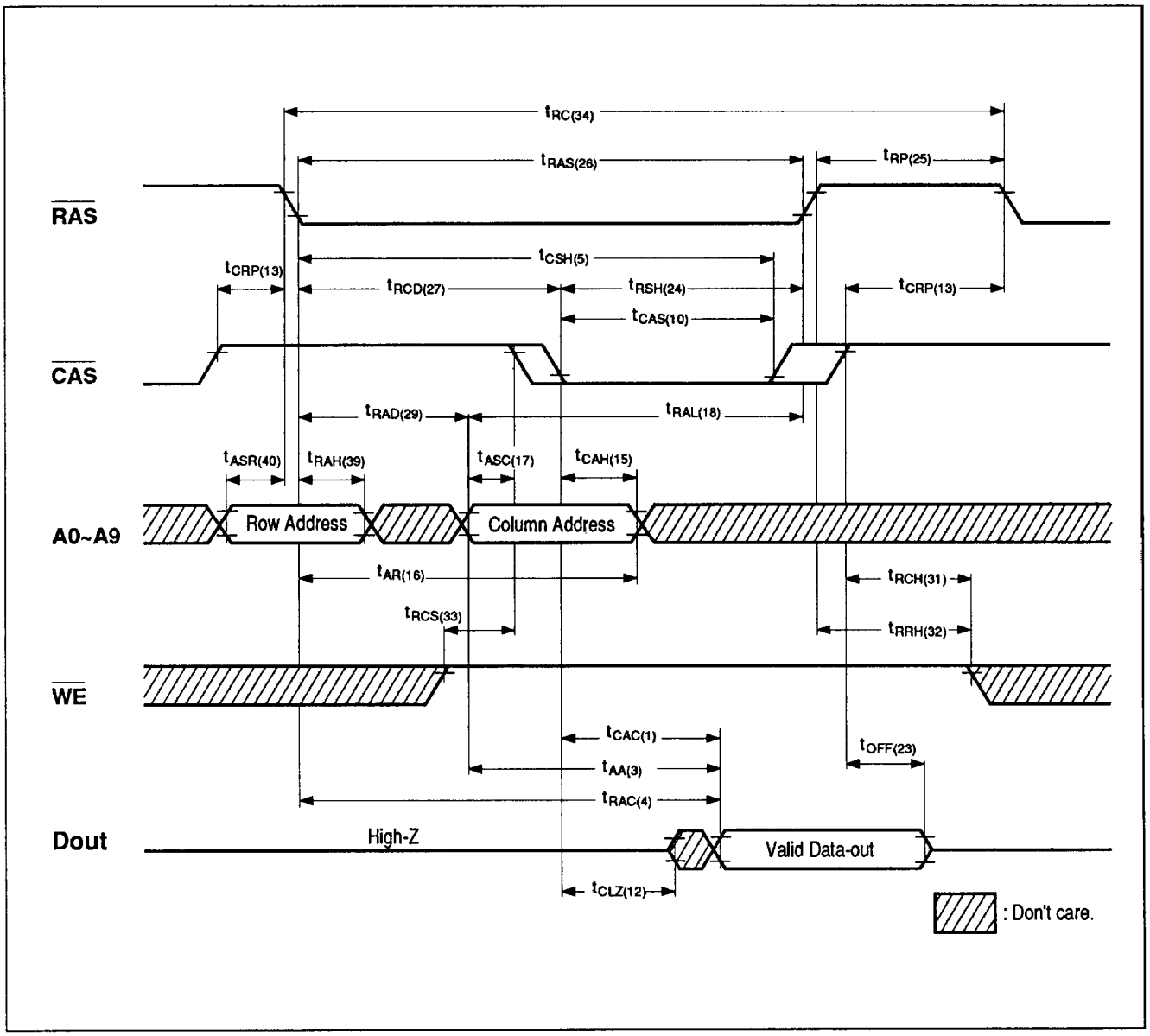
NO.	SYMBOL		PARAMETER	1M200-06		1M200-07		1M200-08		1M200-10		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	—	20	—	25	ns	6
2	t_{CH2QV}	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	40	—	45	—	50	—	55	ns	13
3	t_{AVQV}	t_{AA}	Access Time from Column Address	—	30	—	35	—	40	—	50	ns	7
4	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	—	80	—	100	ns	6
5	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	80	—	100	—	ns	
6	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	30	—	30	—	30	—	30	—	ns	
7	t_{CH2CL2}	t_{CPN}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	10	—	10	—	10	—	15	—	ns	
8	t_{CH2CL2}	t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test)	30	—	40	—	40	—	50	—	ns	
9	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	—	10	—	10	—	10	—	ns	
10	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	15	10K	20	10K	20	10K	25	10K	ns	
11	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	10	—	10	—	10	—	10	—	ns	
12	t_{CL1QV}	t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	0	—	0	—	ns	8
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	5	—	5	—	ns	
14	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	—	20	—	20	—	25	—	ns	11
15	t_{CL1AX}	t_{CAH}	Column Address Hold Time	10	—	15	—	15	—	20	—	ns	
16	t_{RL1AX}	t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	50	—	55	—	60	—	75	—	ns	
17	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0	—	0	—	0	—	0	—	ns	
18	t_{AVRH1}	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	40	—	50	—	ns	
19	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	30	—	35	—	40	—	45	—	ns	11
20	t_{CL1DX} t_{WL1DX}	t_{DH}	Data Hold Time	10	—	15	—	15	—	20	—	ns	12
21	t_{RL1DX}	t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	50	—	55	—	60	—	75	—	ns	
22	t_{DVCL2} t_{DVWL2}	t_{DS}	Data Setup Time	0	—	0	—	0	—	0	—	ns	12
23	t_{CH2QX}	t_{OFF}	Output Buffer Turn-off Delay Time	0	15	0	20	0	20	0	30	ns	10
24	t_{CL1RH1}	t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	20	—	25	—	ns	
25	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	60	—	70	—	ns	
26	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	60	100K	70	100K	80	100K	100	100K	ns	
27	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	15	45	20	50	20	60	25	75	ns	6
28	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	—	0	—	0	—	0	—	ns	
29	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	20	50	ns	7
30	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	60	—	70	—	80	—	100	—	ns	11
31	t_{CH2WL2}	t_{RCH}	Read Command Hold Time	0	—	0	—	0	—	0	—	ns	9
32	t_{RH2WL2}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	—	0	—	0	—	0	—	ns	9
33	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0	—	0	—	0	—	0	—	ns	
34	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	110	—	130	—	150	—	190	—	ns	
35	t_{CL2CL2}	t_{PC}	Read or Write Cycle Time (Fast Page Mode)	40	—	45	—	50	—	55	—	ns	13,14
36	t_{RL2RL2}	t_{RWC}	Read-Modify-Write Cycle Time	135	—	155	—	175	—	225	—	ns	
37	t_{CL2CL2}	t_{PRWC}	Read-Modify-Write Cycle Time (Fast Page Mode)	65	—	70	—	75	—	90	—	ns	13,14

NO.	SYMBOL		PARAMETER	1M200-06		1M200-07		1M200-08		1M200-10		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
38	t_{REF}	t_{REF}	Refresh Period	—	8	—	8	—	8	—	8	ms	
39	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10	—	12	—	12	—	15	—	ns	
40	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0	—	0	—	0	—	0	—	ns	
41	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	4, 5
42	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	10	—	15	—	15	—	20	—	ns	
43	t_{RL1WH1}	t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	50	—	55	—	60	—	75	—	ns	
44	t_{WL1WH1}	t_{WP}	Write Command Pulse Width	10	—	15	—	15	—	20	—	ns	
45	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0	—	0	—	0	—	0	—	ns	11
46	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	20	—	25	—	ns	
47	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	20	—	25	—	ns	

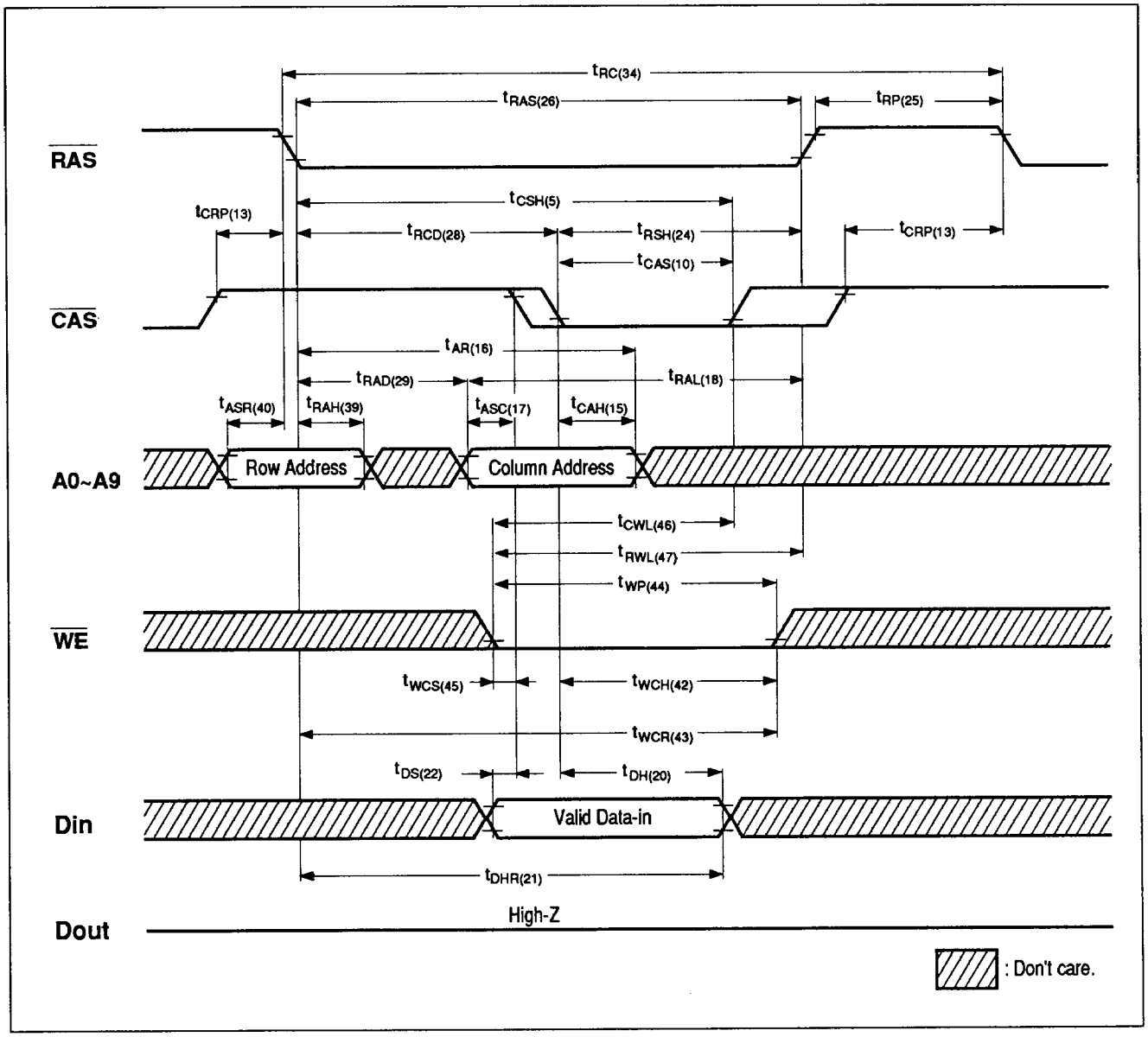
Notes:

3. Following power up, an initial pause of 200µs is required followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required. Eight initialization cycles are required after extended periods of bias without clocks (greater than 8ms).
4. AC measurements assume t_T=5ns. All AC parameters are measured with V_{IL}(min.)≥V_{SS} and V_{IH}(max.)≤V_{CC} and with a load equivalent to two TTL loads and 100pF.
5. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
6. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
7. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
8. Assumes three state test load (5pF and a 380 Ohm Thevenin equivalent).
9. Either t_{RCH} or t_{RRH} must be satisfied for a Read cycle.
10. t_{OFF}(max.) defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS}≥t_{WCS}(min.), the cycle is an Early Write cycle and the data-out pin will remain open circuit (high impedance) throughout the entire cycle. If t_{RWD}≥t_{RWD}(min.), t_{CWD}≥t_{CWD}(min.) and t_{AWD}≥t_{AWD}(min.), the cycle is a Read-Modify-Write cycle and Data-out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of Data-out (at access time) is indeterminate.
12. These parameters are referenced to $\overline{CAS}$ leading edge in Early Write cycles and to $\overline{WE}$ leading edge in Read-Modify-Write cycles.
13. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{CPA}.
14. t_{ASC}≥t_{CP} to achieve t_{PC}(min.) and t_{CPA}(max.) values.

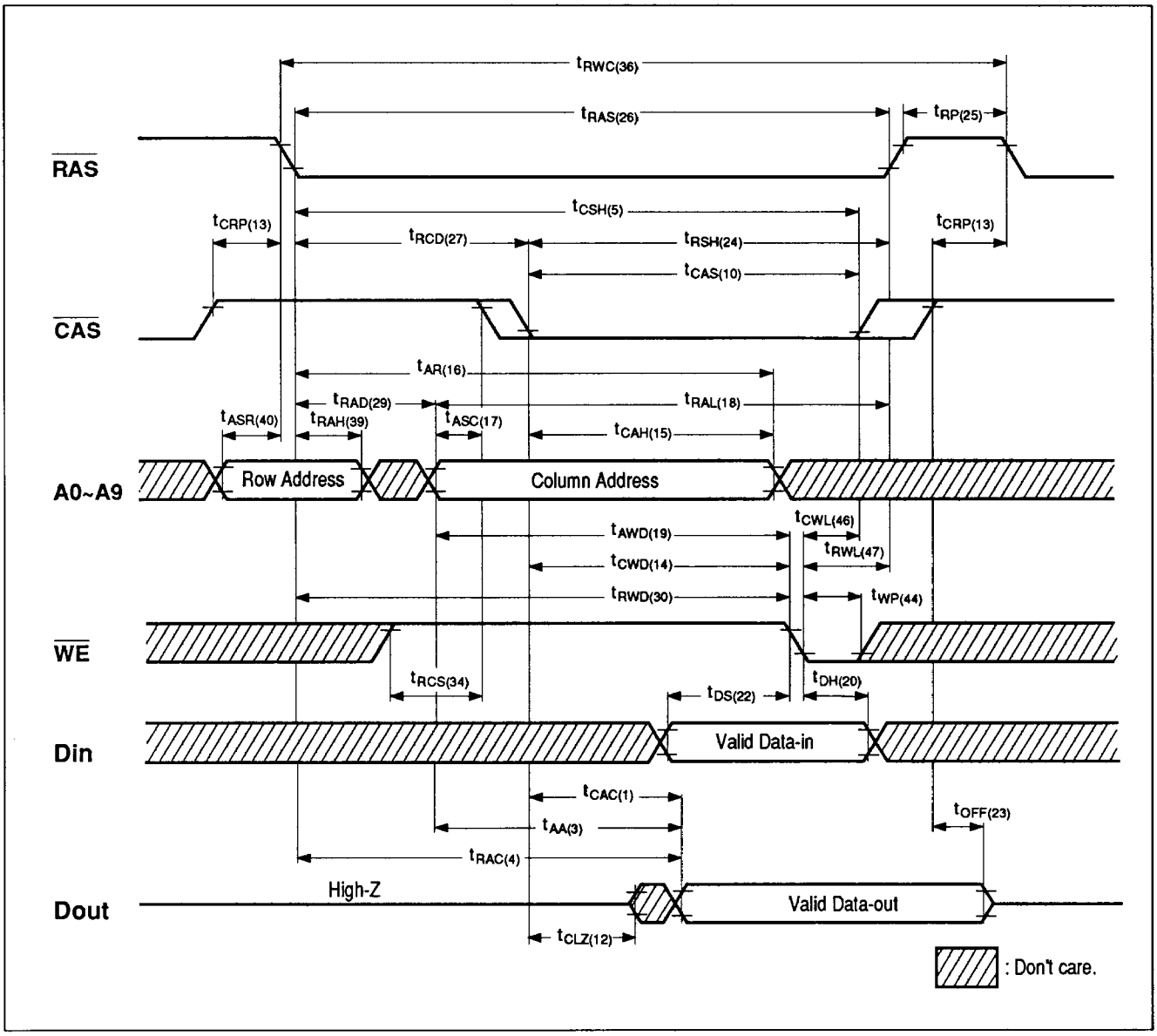
READ CYCLE


tRC(34)
tRAS(26)
tRP(25)
RAS
tCSH(5)
tCRP(13)
tRCD(27)
tRSH(24)
tCRP(13)
tCAS(10)
CAS
tRAD(29)
tRAL(18)
tASR(40)
tRAH(39)
tASC(17)
tCAH(15)
A0~A9
Row Address
Column Address
tAR(16)
tRCH(31)
tRCS(33)
tRRH(32)
WE
tCAC(1)
tOFF(23)
tAA(3)
tRAC(4)
Dout
High-Z
Valid Data-out
tCLZ(12)
: Don't care.

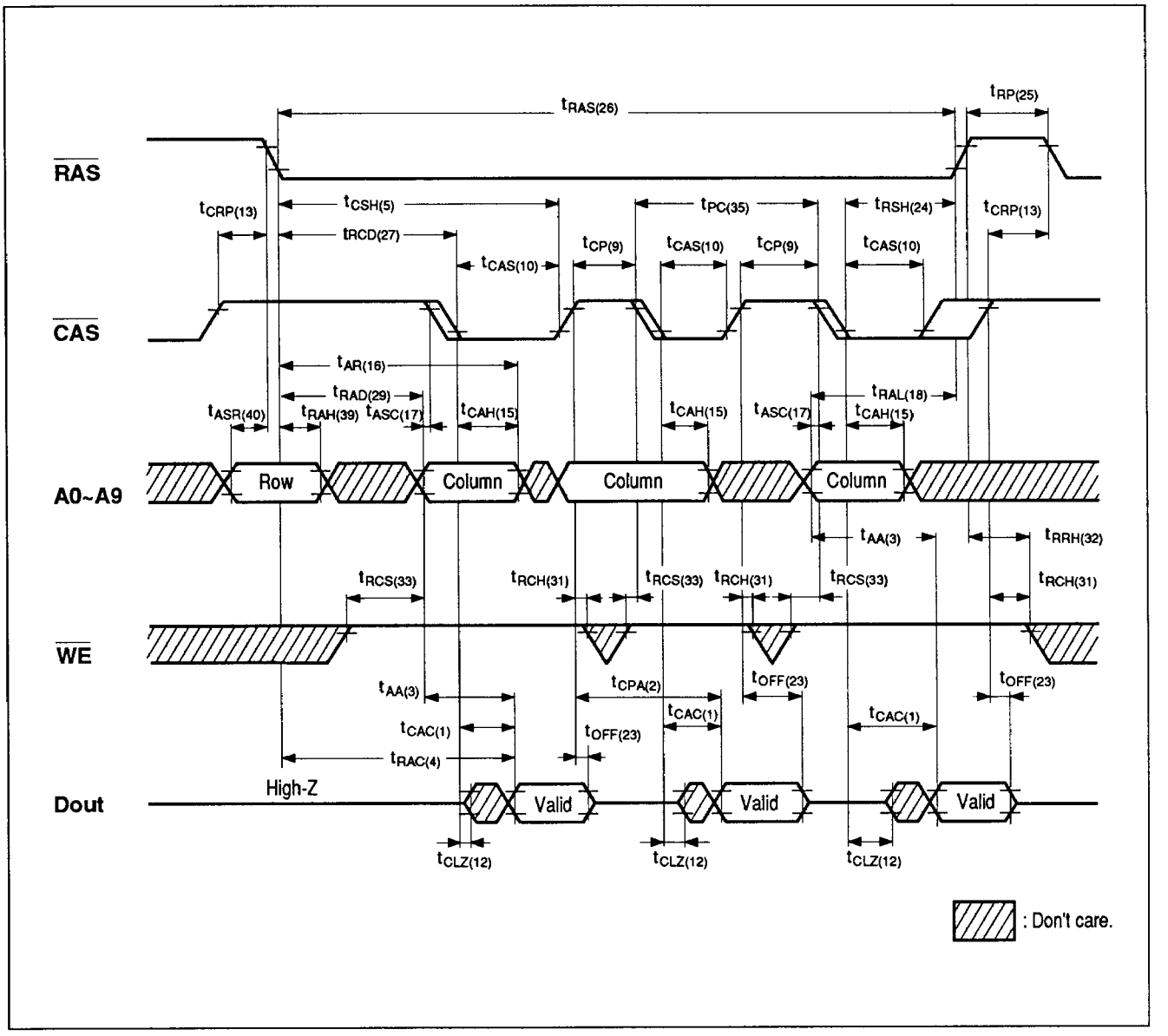
EARLY WRITE CYCLE



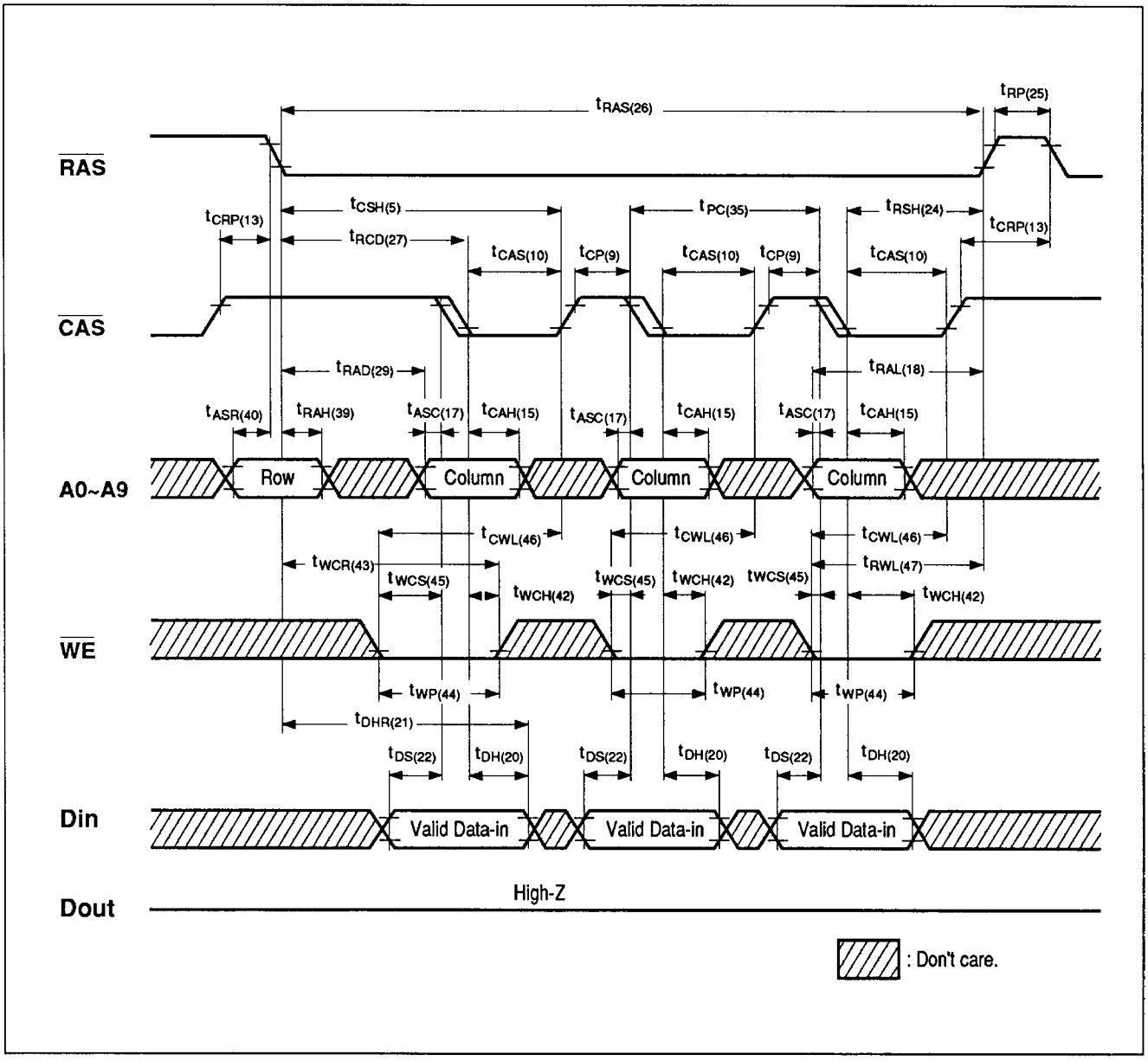
READ-MODIFY-WRITE CYCLE



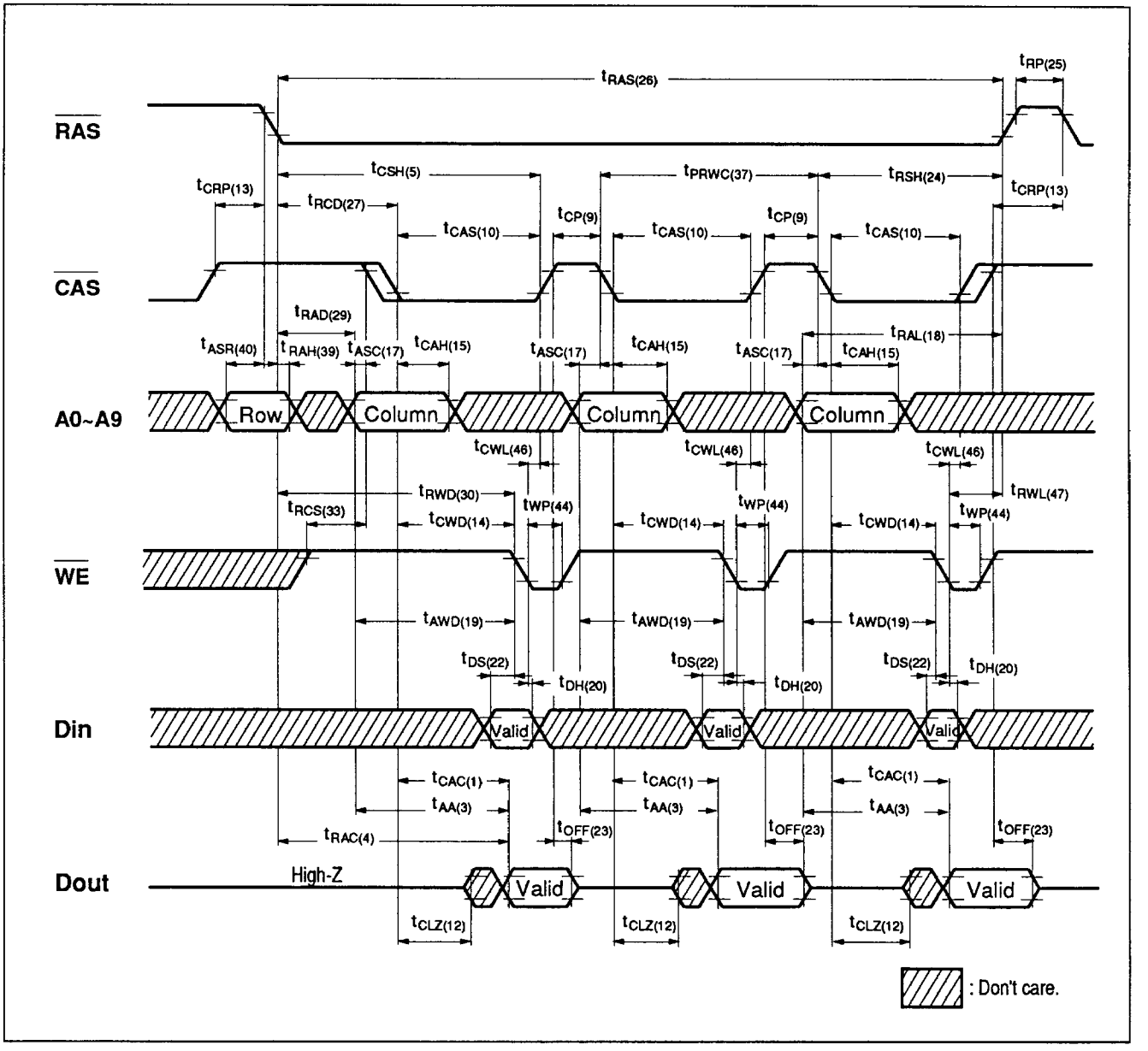
FAST PAGE MODE READ CYCLE



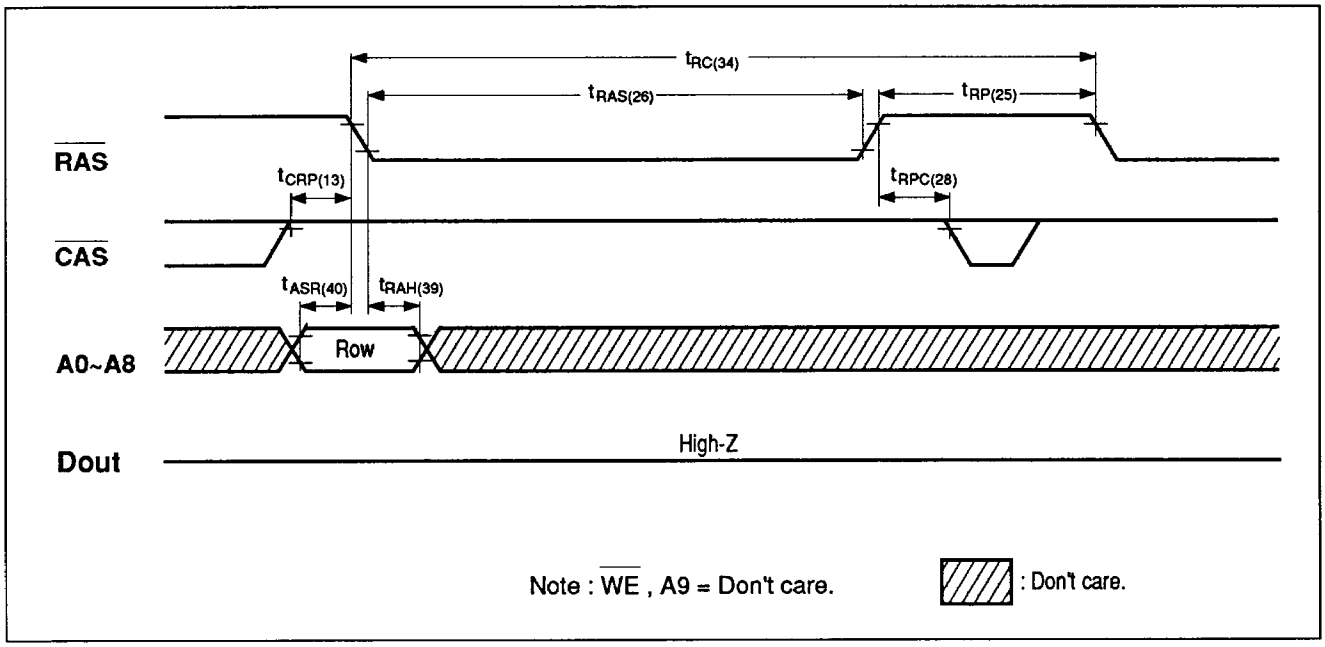
FAST PAGE MODE EARLY WRITE CYCLE



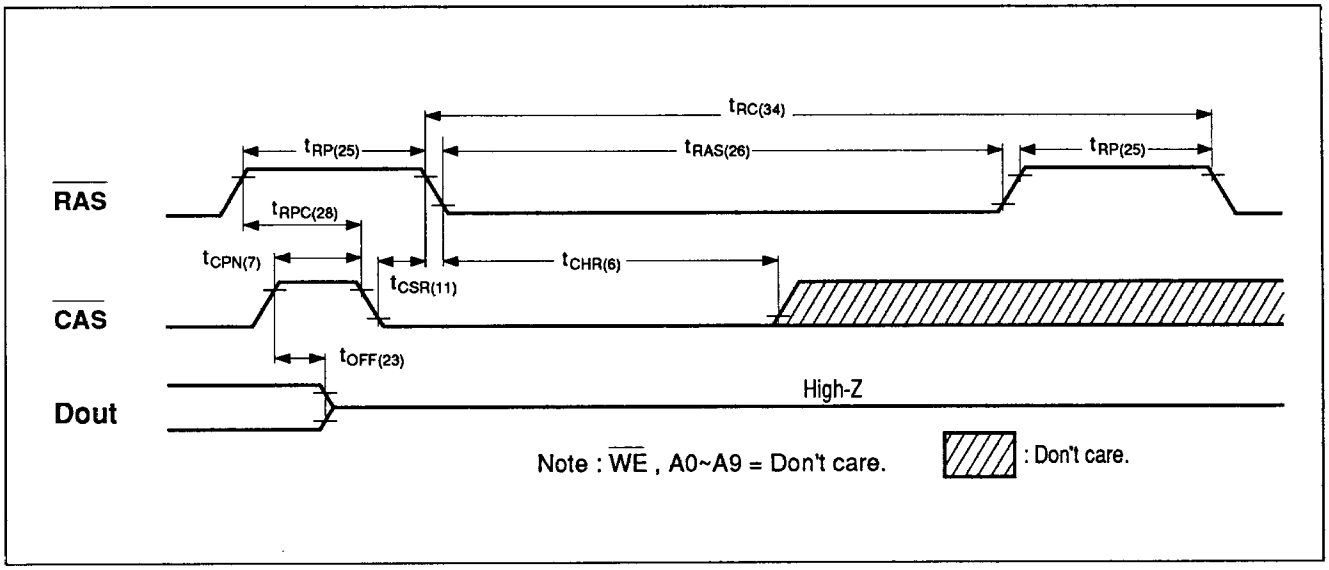
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



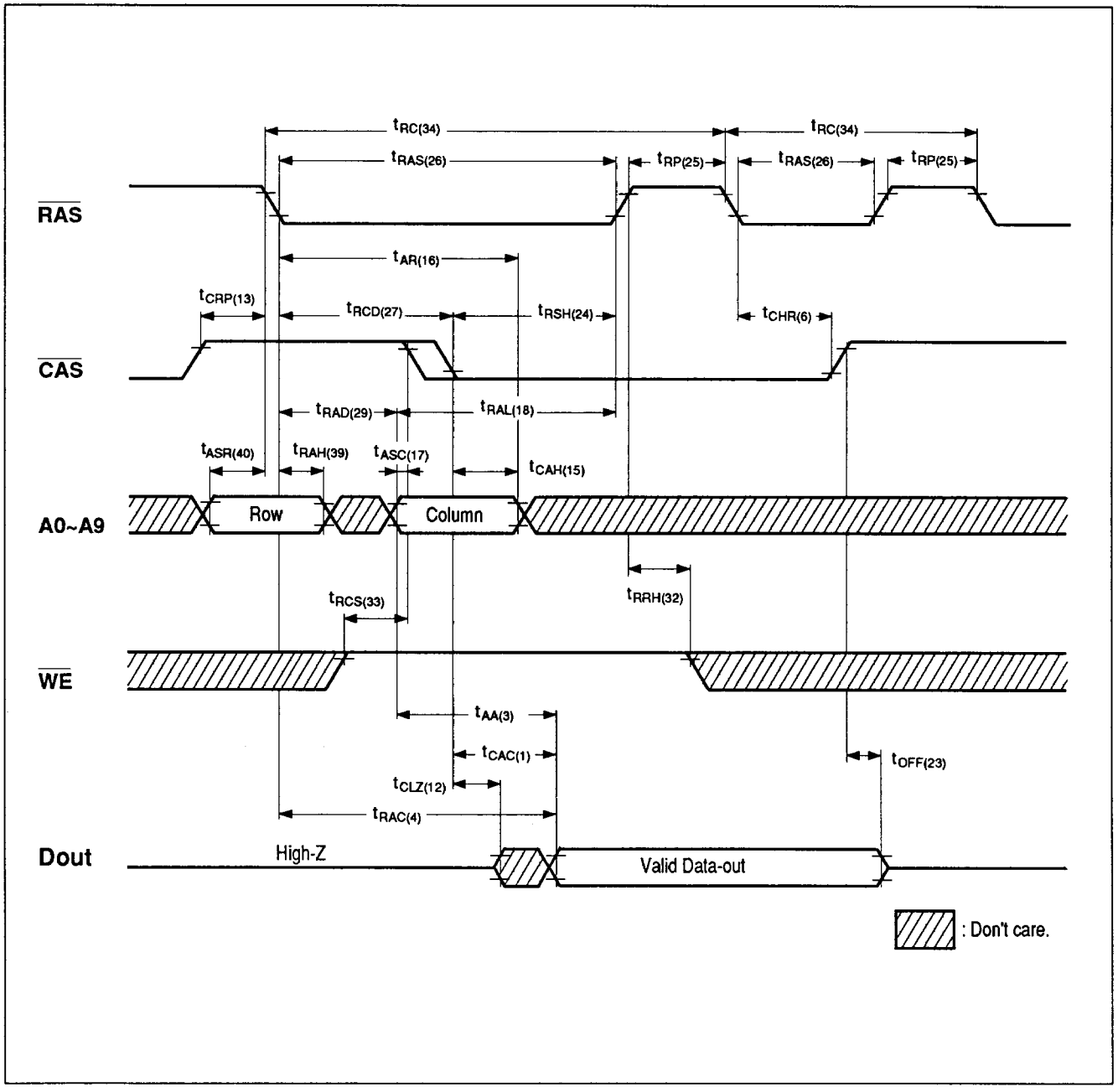
$\overline{RAS}$ ONLY REFRESH



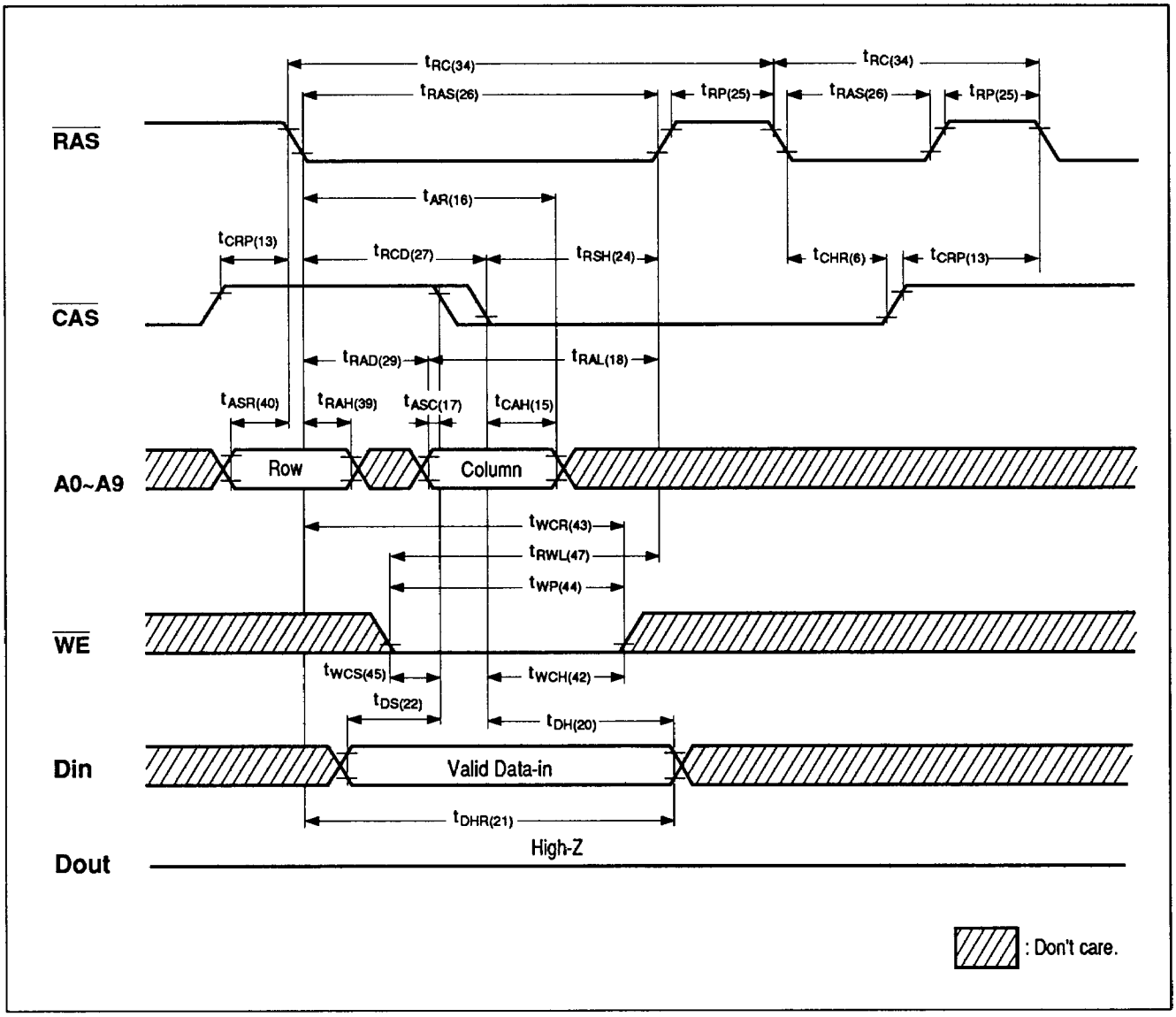
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH



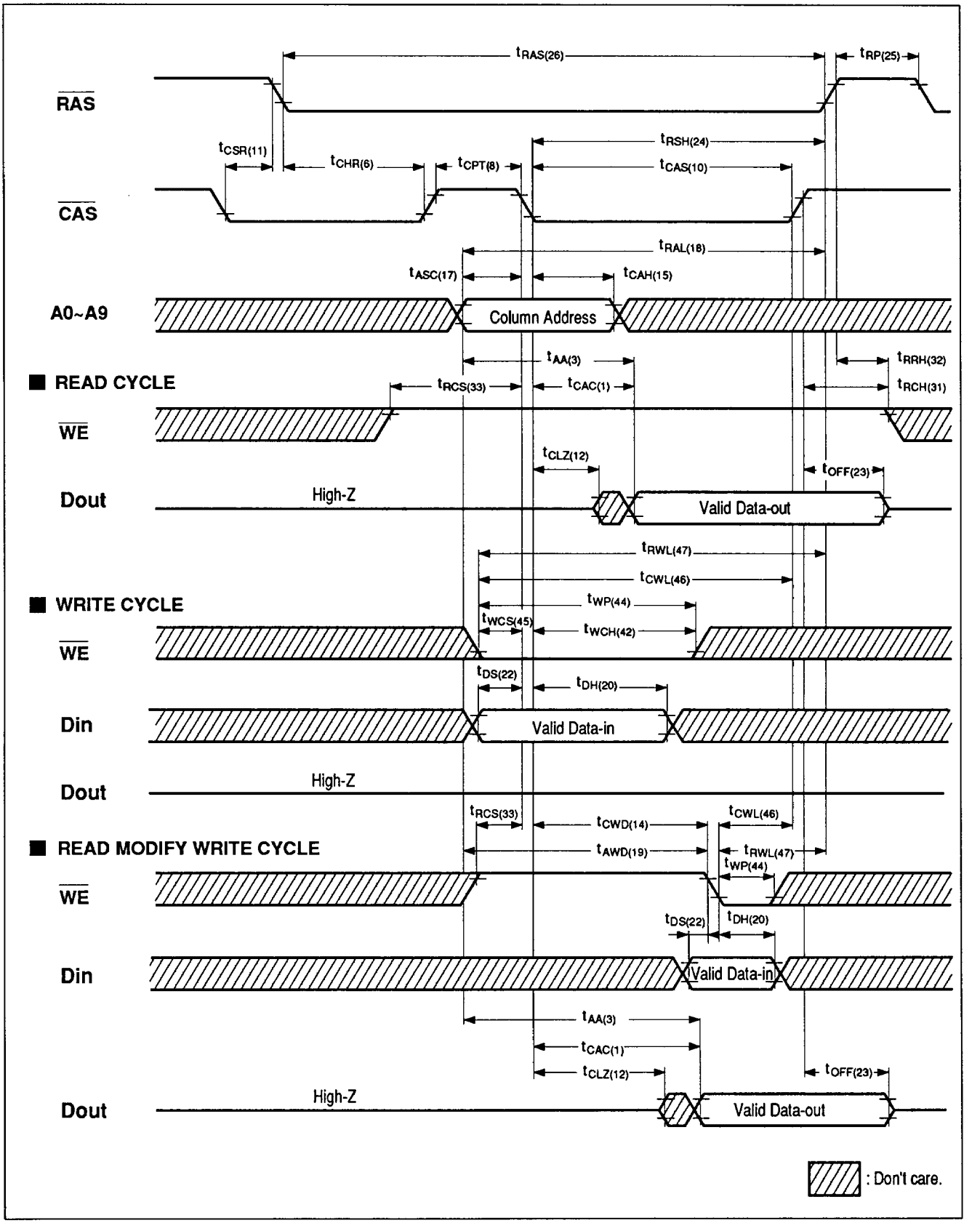
HIDDEN REFRESH (READ)



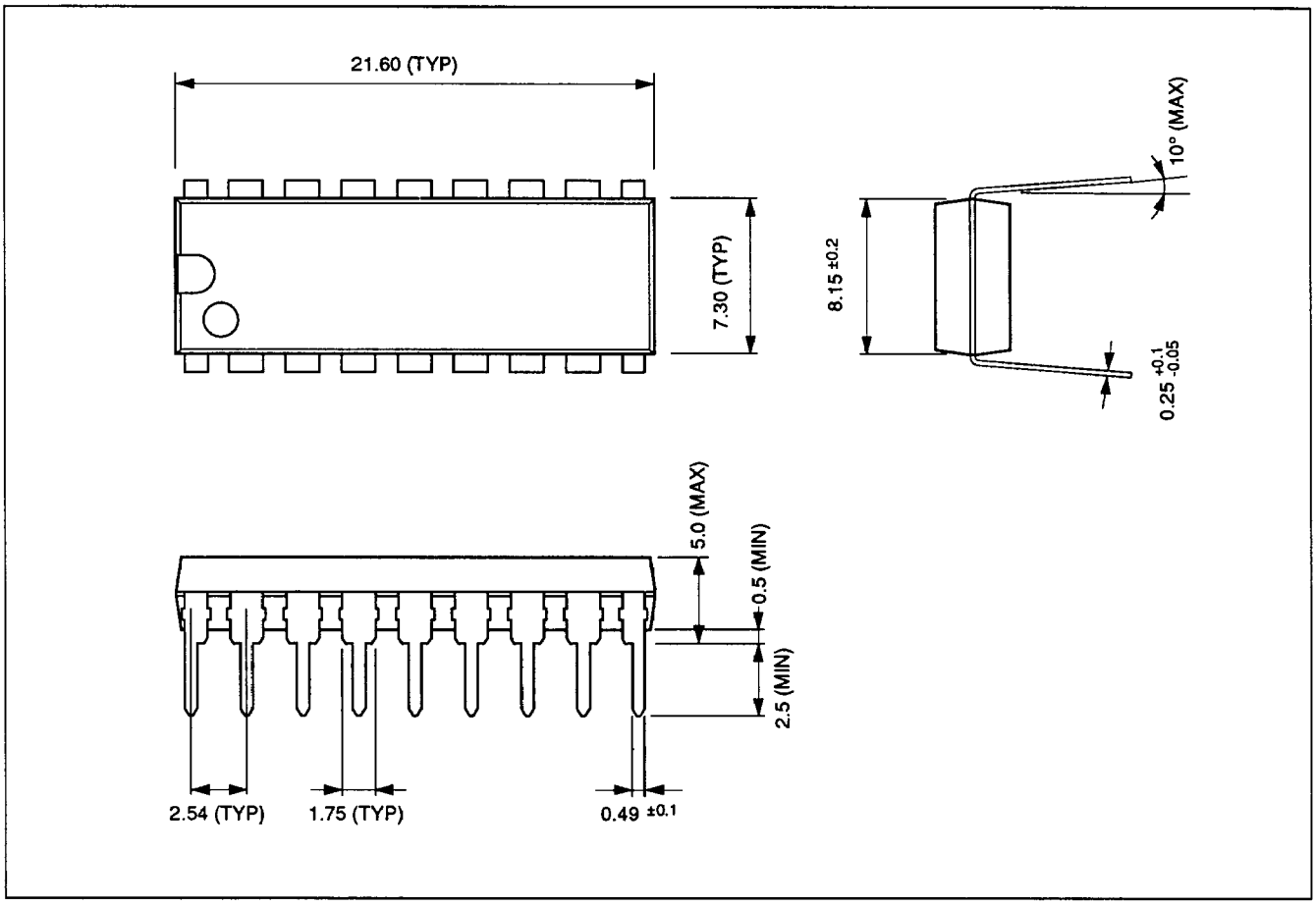
HIDDEN REFRESH (WRITE)



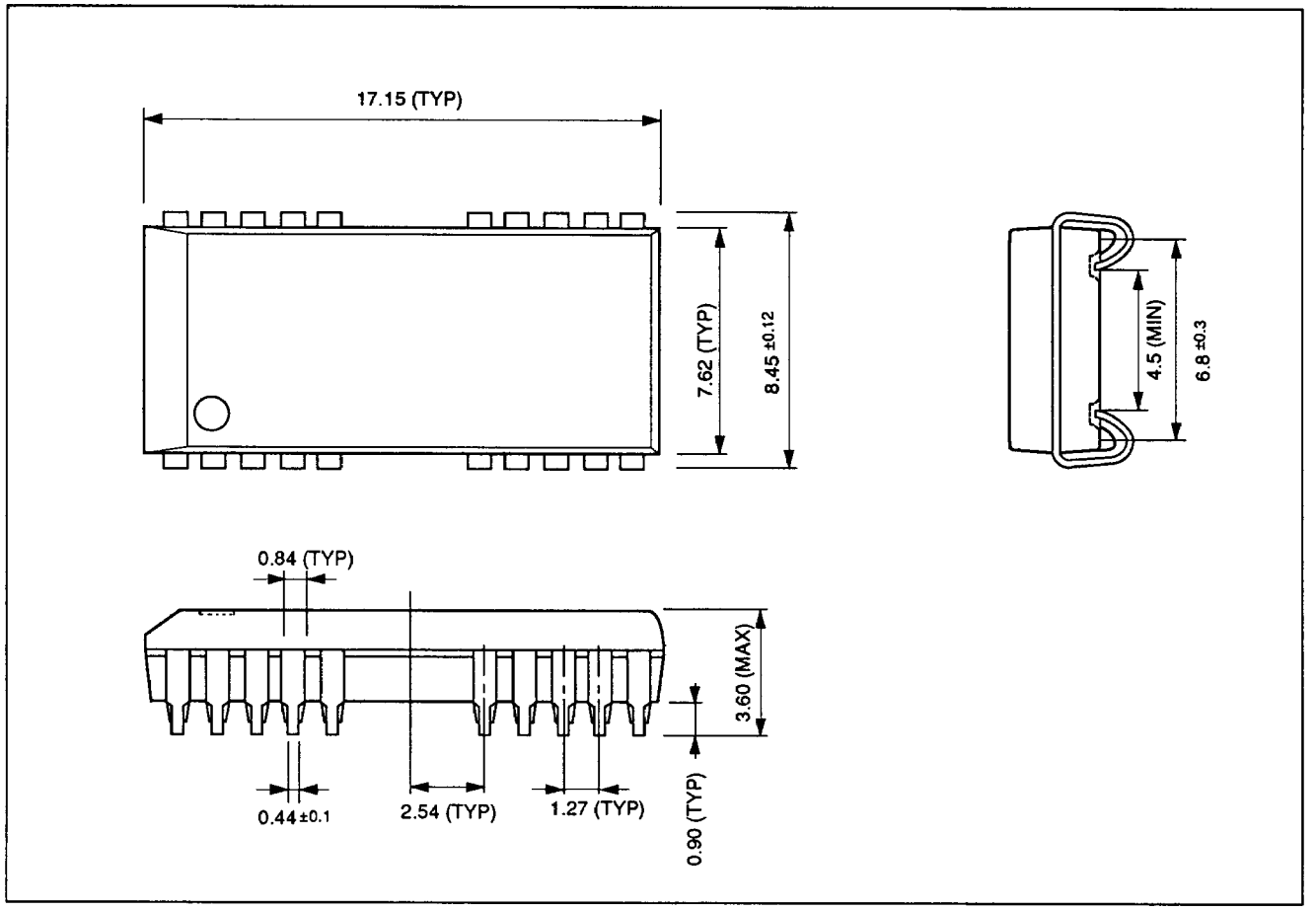
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



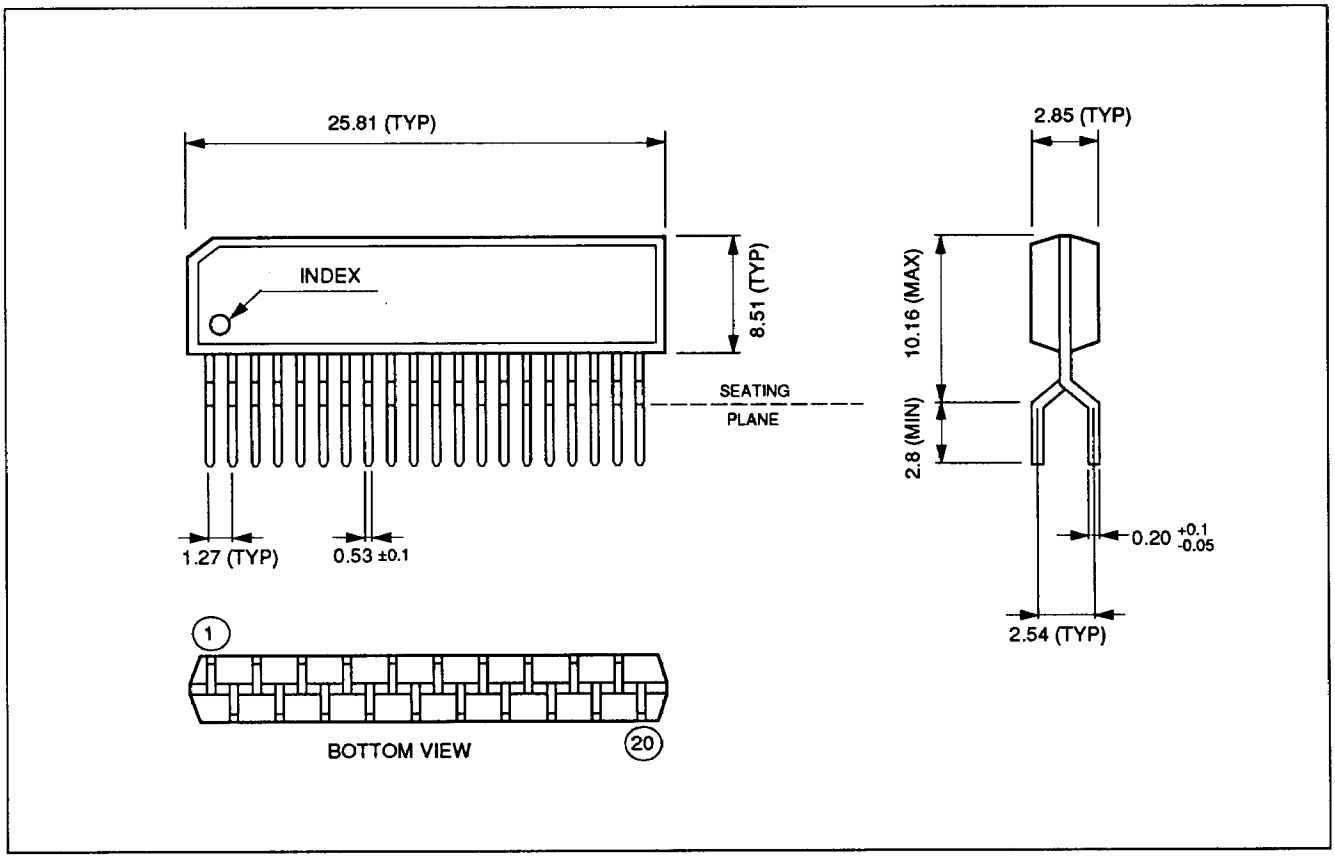
18 PIN PLASTIC DIP (300 mil) (Unit: mm)



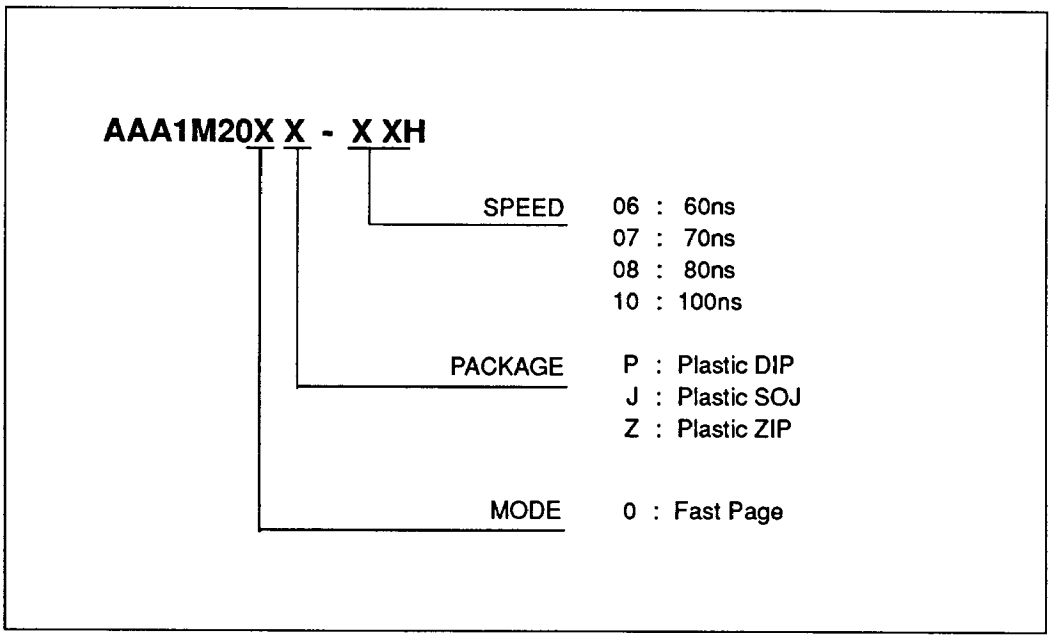
26 PIN PLASTIC SOJ (Unit: mm)



20 PIN PLASTIC ZIP (Unit: mm)



ORDERING INFORMATION



NMB SEMICONDUCTOR CO., LTD. reserves the right to make changes to the product described herein, and does not assume any liability which may occur due to the use or application of the product described.

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