



8-INPUT PRIORITY ENCODER

The HEF4532B is an 8-input priority encoder with eight active HIGH priority inputs (I_0 to I_7), three active HIGH outputs (O_0 to O_2), an active HIGH enable input (E_{in}), an active HIGH enable output (E_{out}) and an active HIGH group select output (GS).

Data is accepted on inputs I_0 to I_7 . The binary code corresponding to the highest priority input (I_0 to I_7) which is HIGH, is generated on O_0 to O_2 if E_{in} is HIGH. Input I_7 is assigned the highest priority. GS is HIGH when one or more priority inputs and E_{in} are HIGH. E_{out} is HIGH when I_0 to I_7 are LOW and E_{in} is HIGH. E_{in} , when LOW, forces all outputs (O_0 to O_2 , GS, E_{out}) LOW.

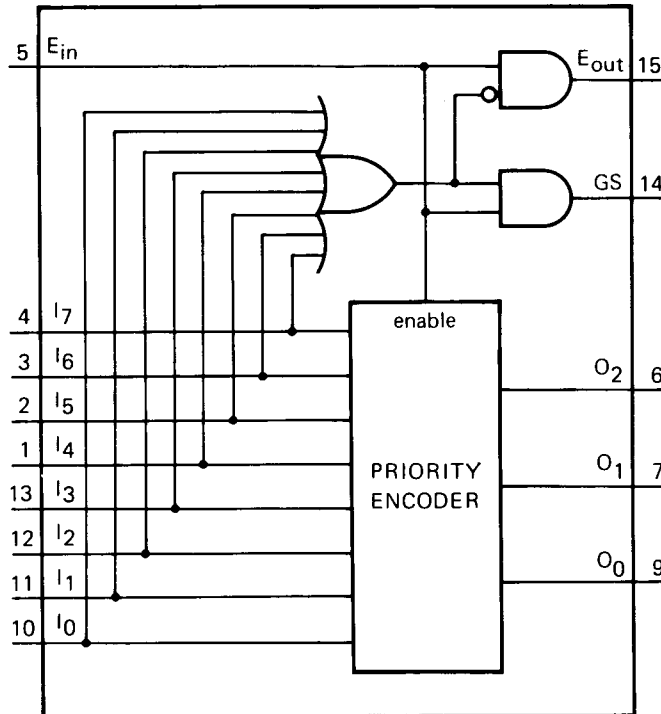
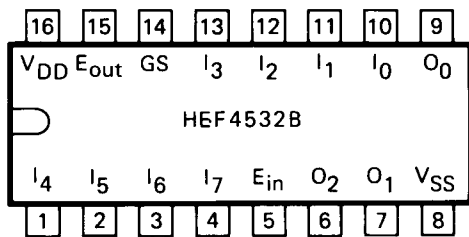


Fig. 1 Functional diagram.

7Z75371.1



7Z75365.1

Fig. 2 Pinning diagram.

HEF4532BP : 16-lead DIL; plastic (SOT-38Z).
 HEF4532BD : 16-lead DIL; ceramic (cerdip) (SOT-74).
 HEF4532BT : 16-lead mini-pack; plastic
 (SO-16; SOT-109A).

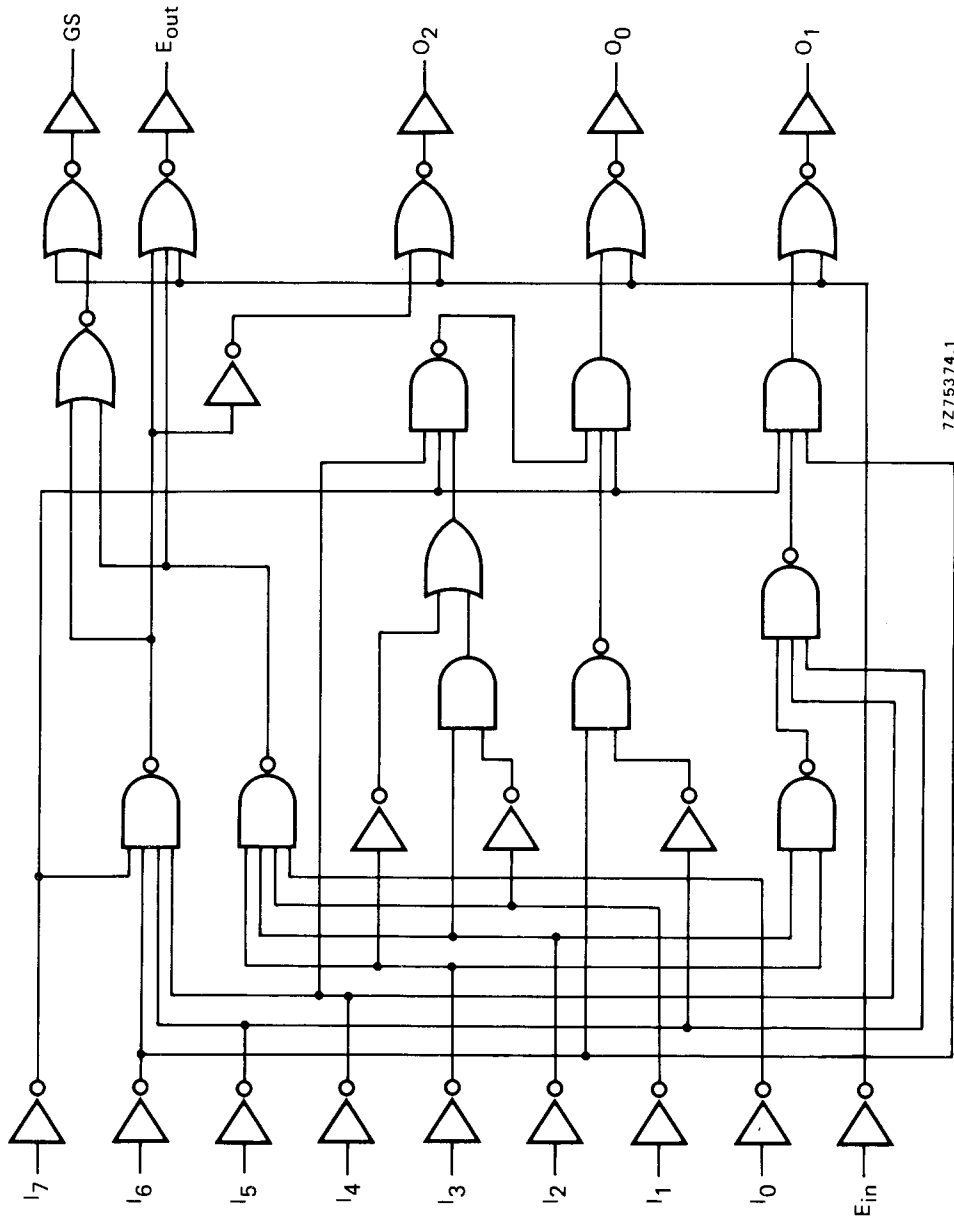
PINNING

I_0 to I_7 priority inputs
 E_{in} enable input
 E_{out} enable output
 GS group select output
 O_0 to O_2 outputs

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications



7275374.1

Fig. 3 Logic diagram.

TRUTH TABLE

inputs									outputs				
E _{in}	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	GS	O ₂	O ₁	O ₀	E _{out}
L	X	X	X	X	X	X	X	X	L	L	L	L	L
H	L	L	L	L	L	L	L	L	L	L	L	L	H
H	H	X	X	X	X	X	X	X	H	H	H	H	L
H	L	H	X	X	X	X	X	X	H	H	H	L	L
H	L	L	H	X	X	X	X	X	H	H	L	H	L
H	L	L	L	H	X	X	X	X	H	H	L	L	L
H	L	L	L	L	H	X	X	X	H	L	H	H	L
H	L	L	L	L	L	H	X	X	H	L	H	L	L
H	L	L	L	L	L	L	H	X	H	L	L	H	L
H	L	L	L	L	L	L	L	H	H	L	L	L	L

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

LOGIC EQUATIONS

$$O_2 = E_{in} \cdot (I_4 + I_5 + I_6 + I_7)$$

$$O_1 = E_{in} \cdot (I_2 \cdot \bar{I}_4 \cdot \bar{I}_5 + I_3 \cdot \bar{I}_4 \cdot \bar{I}_5 + I_6 + I_7)$$

$$O_0 = E_{in} \cdot (I_1 \cdot \bar{I}_2 \cdot \bar{I}_4 \cdot \bar{I}_6 + I_3 \cdot \bar{I}_4 \cdot \bar{I}_6 + I_5 \cdot \bar{I}_6 + I_7)$$

$$E_{out} = E_{in} \cdot \bar{I}_0 \cdot \bar{I}_1 \cdot \bar{I}_2 \cdot \bar{I}_3 \cdot \bar{I}_4 \cdot \bar{I}_5 \cdot \bar{I}_6 \cdot \bar{I}_7$$

$$GS = E_{in} \cdot (I_0 + I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + I_7)$$

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	typical formula for P (μW)	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) Σ(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5 10 15	1 620 f _i + Σ(f _o C _L) × V _{DD} ² 6 600 f _i + Σ(f _o C _L) × V _{DD} ² 15 970 f _i + Σ(f _o C _L) × V _{DD} ²	

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$; see also waveforms Fig. 4

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays $E_{in} \rightarrow E_{out}$ HIGH to LOW	5	tPHL		95	190	ns	$68\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		45	90	ns	$34\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		35	70	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	tPLH		80	160	ns	$53\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		35	70	ns	$24\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$	
$E_{in} \rightarrow GS$ HIGH to LOW	5	tPHL		85	170	ns	$58\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		45	90	ns	$34\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		35	70	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	tPLH		80	160	ns	$53\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$	
$E_{in} \rightarrow O_n$ HIGH to LOW	5	tPHL		80	160	ns	$53\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	tPLH		85	170	ns	$58\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$	
$I_n \rightarrow O_n$ HIGH to LOW	5	tPHL		115	230	ns	$88\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		35	70	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	tPLH		115	230	ns	$88\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		35	70	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$	
$I_n \rightarrow GS$ HIGH to LOW	5	tPHL		115	230	ns	$88\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		40	80	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	tPLH		115	230	ns	$88\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		40	80	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$	
Output transition times HIGH to LOW	5	tTHL		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
LOW to HIGH	5	tTLH		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	

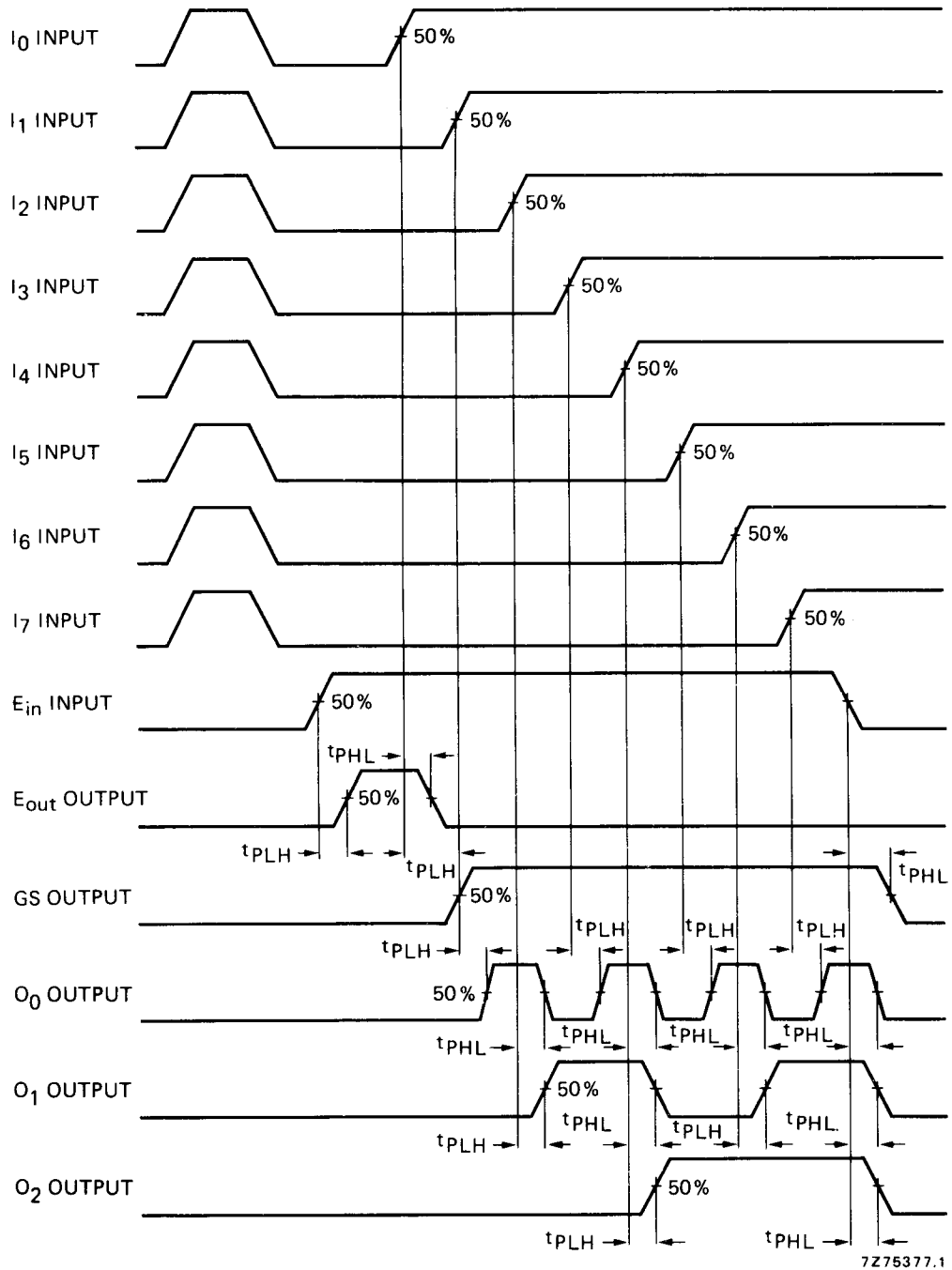


Fig. 4 Waveforms showing propagation delays from inputs to outputs.

APPLICATION INFORMATION

Some examples of applications for the HEF4532B are:

- Priority encoder
- Keyboard encoder

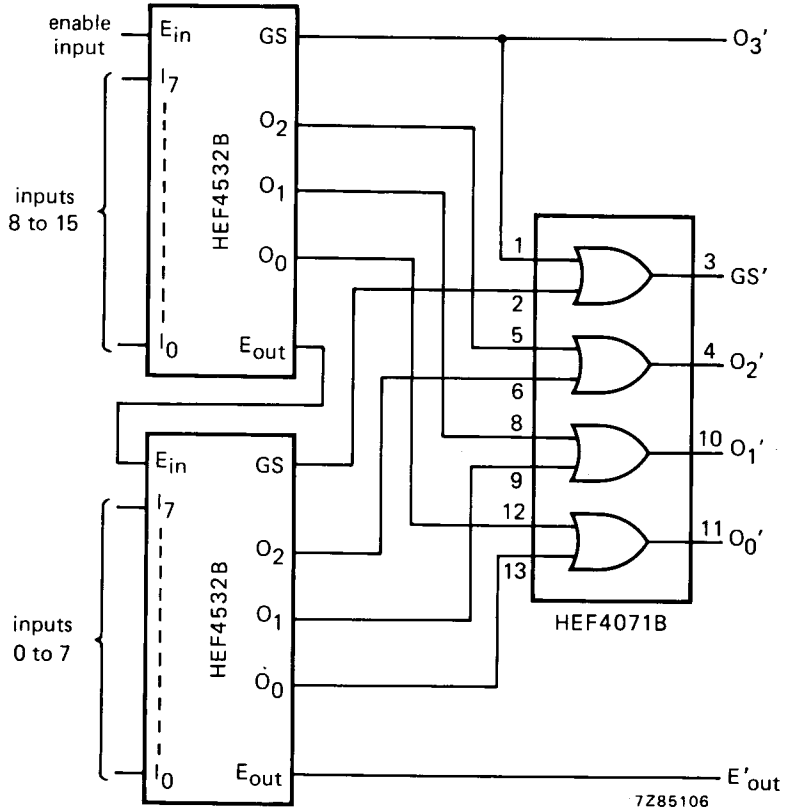


Fig. 5 16-level priority encoder.

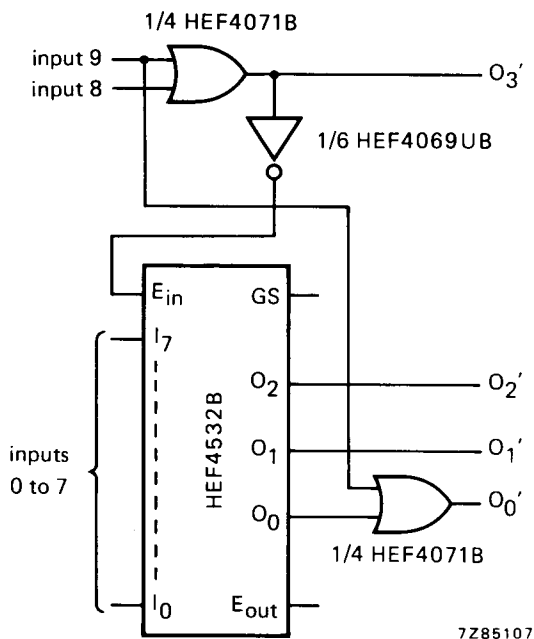


Fig. 6 0-to-9 keyboard encoder.

TRUTH TABLE (for Fig. 6)

inputs										outputs				
9	8	7	6	5	4	3	2	1	0	GS	O ₃ '	O ₂ '	O ₁ '	O ₀ '
H	X	X	X	X	X	X	X	X	X	L	H	L	L	H
L	H	X	X	X	X	X	X	X	X	L	H	L	L	L
L	L	H	X	X	X	X	X	X	X	H	L	H	H	H
L	L	L	H	X	X	X	X	X	X	H	L	H	H	L
L	L	L	L	H	X	X	X	X	X	H	L	H	L	H
L	L	L	L	L	H	X	X	X	X	H	L	L	H	H
L	L	L	L	L	L	H	X	X	X	H	L	L	H	L
L	L	L	L	L	L	L	H	X	X	H	L	L	L	H
L	L	L	L	L	L	L	L	H	H	H	L	L	L	L

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial