PRELIMINARY

Am79Q06/061/062/063

Quad Subscriber Line Audio-Processing Circuit (QSLAC™) Devices

TABLE OF CONTENTS

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LIST OF FIGURES

LIST OF TABLES

DISTINCTIVE CHARACTERISTICS

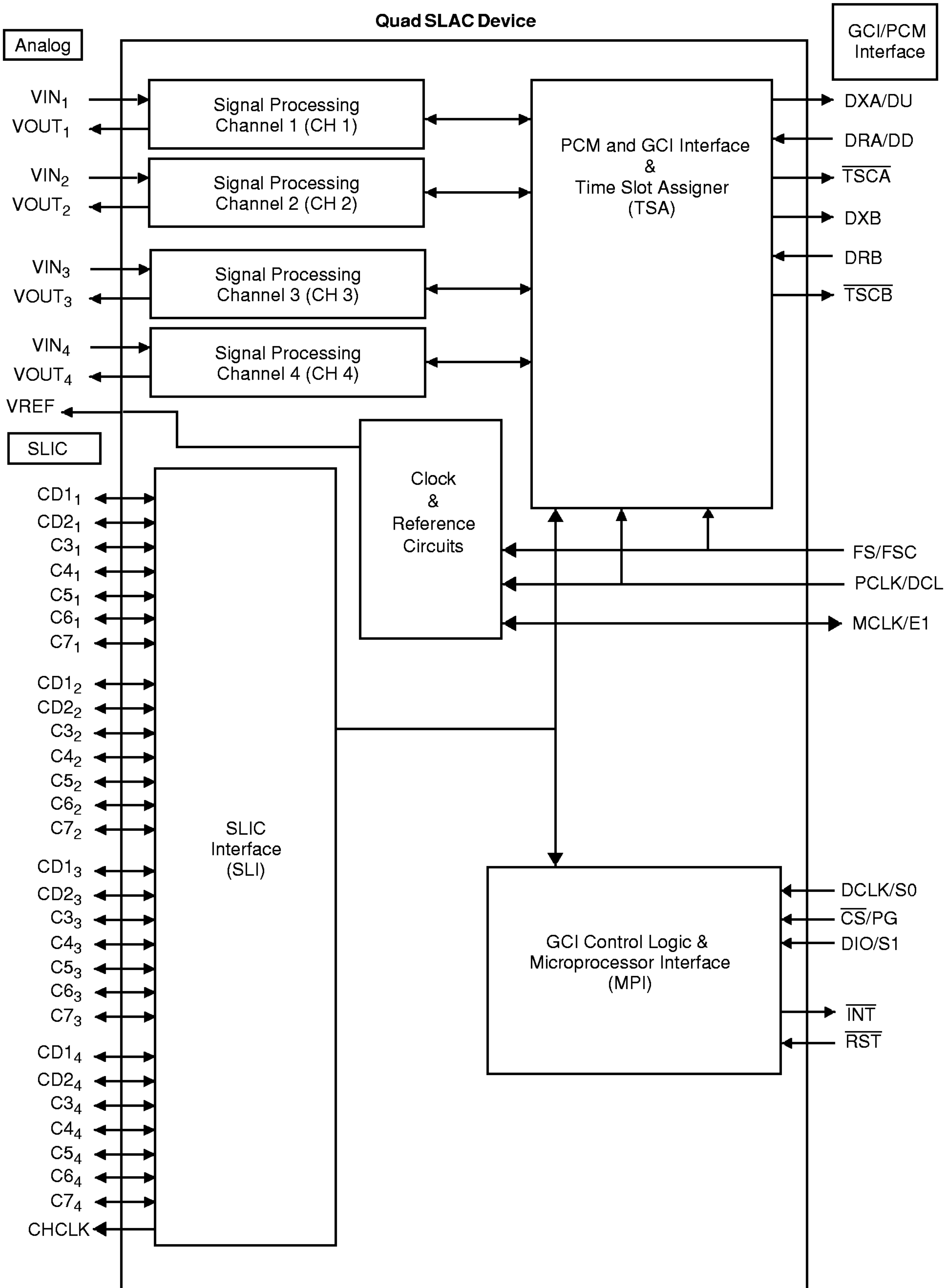
- **Pin Programmable PCM/MPI or GCI Interface**
- **Standard PCM/microprocessor interface (PCM/MPI)**
  - — Single or Dual PCM ports available
  - — Time slot assigner
  - — Clock slot and transmit clock edge options
  - — Up to 128 channels (PCLK at 8.192 MHz) per PCM port
  - — Optional supervision on the PCM highway
  - — 1.536, 1.544, 2.048, 3.072, 3.088, 4.096, 6.144, 6.176, or 8.192 MHz master clock derived from MCLK or PCLK (PCM/MPI mode)
  - — µP access to PCM data
  - — Linear Data mode
  - — Real Time Data register with interrupt (open drain or TTL output)
  - — Broadcast mode
- **General Circuit Interface (GCI)**
  - — Control and PCM data on a single port
  - — 2.048 Mbits/s data rate
  - — 2.048 MHz or 4.096 MHz clock option
- **Performs the functions of four codec/filters**
- **A-law, µ-law, or linear coding**
- **Software programmable:**
  - — SLIC input impedance and Transhybrid balance
  - — Transmit and receive gains and Equalization
  - — Programmable Digital I/O pins with debouncing
- **Built-in test modes with loopback and tone generation**
- **Low-power, 5.0 V only CMOS Technology**
- **Mixed mode (analog and digital) impedance scaling**
- **Performance characteristics guaranteed over a 12 dB gain range**
- **Supports multiplexed SLIC inputs**
- **256 kHz or 293 kHz chopper clock for AMD SLICs with switching regulator**
- **Maximum channel bandwidth for V.34 modems**

GENERAL DESCRIPTION

The Am79Q06/061/062/063 Quad Subscriber Line Audio-Processing Circuit (QSLAC™) devices integrate the key functions of analog linecards into high-performance, very-programmable, four-channel codec-filter devices. The QSLAC devices are based on the proven design of AMD's reliable SLAC™ device families. The advanced architecture of the QSLAC devices implements four independent channels and employs digital filters to allow software control of transmission, thus providing a cost-effective solution for the audio-processing function of programmable linecards. Submicron CMOS technology makes the Am79Q06/061/062/063 QSLAC device economical, with the functionality and low power consumption needed in linecard design, maximizing density at minimum cost. When used with four AMD SLICs, a QSLAC device provides a complete software-configurable solution to the BORSCHT function.

The Am79Q06/061/062/063 device supports the feature set of the Am79Q02/021/031 device and provides a General Circuit Interface as a programmable option.

BLOCK DIAGRAM



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ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

Am79Q06/061/062/063 J C

TEMPERATURE RANGE
*C = Commercial (0°C to 70°C;
Relative Humidity = 15% to 95%)

PACKAGE TYPE
J = 44-Pin Plastic Leaded Chip Carrier (PL 044)
—Am79Q06/061 Only
32-Pin Plastic Leaded Chip Carrier (PL 032)
—Am79Q062
V = 44-Pin Thin Quad Flat Pack (PQT 044)
—Am79Q06/061 Only
64-Pin Thin Quad Flat Pack (PQL 064)
—Am79Q063 Only

DEVICE NUMBER/DESCRIPTION
Am79Q06/061/062/063
Quad Subscriber Line Audio-Processing Circuit (QSLAC) Device

Valid Combinations	
Am79Q06	JC, VC
Am79Q061	JC, VC
Am79Q062	JC
Am79Q063	VC

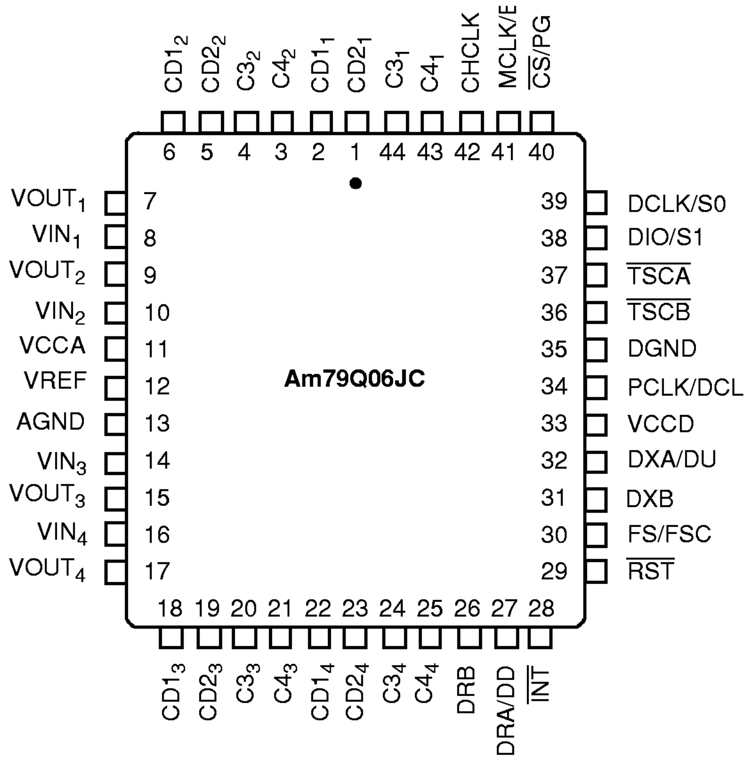
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note:
** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

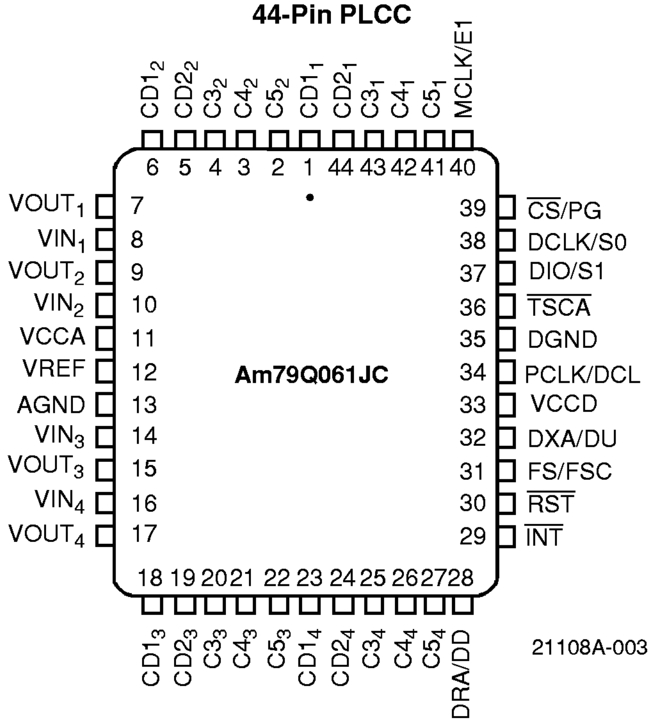
CONNECTION DIAGRAMS

Top View



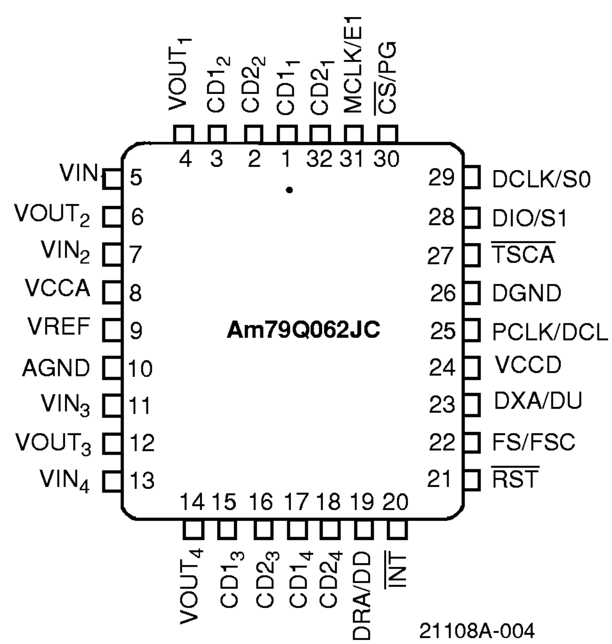
21108A-002

44-Pin PLCC



21108A-003

32-Pin PLCC



21108A-004

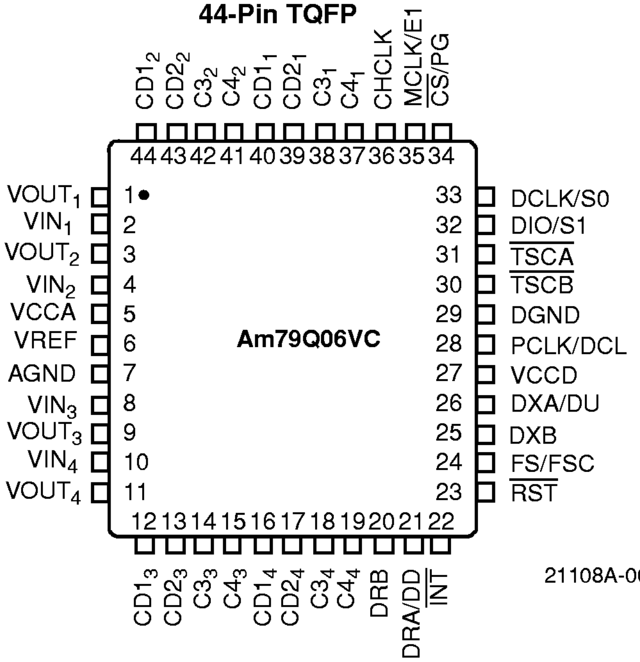
Notes:

1. *Pin 1 is marked for orientation.*
2. *RSVD = Reserved pin; do not connect externally to any signal or supply.*

CONNECTION DIAGRAMS (continued)

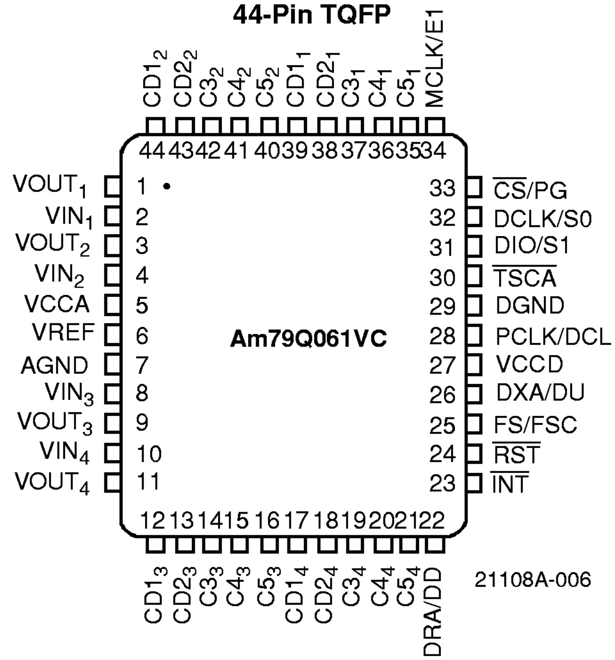
Top View

44-Pin TQFP



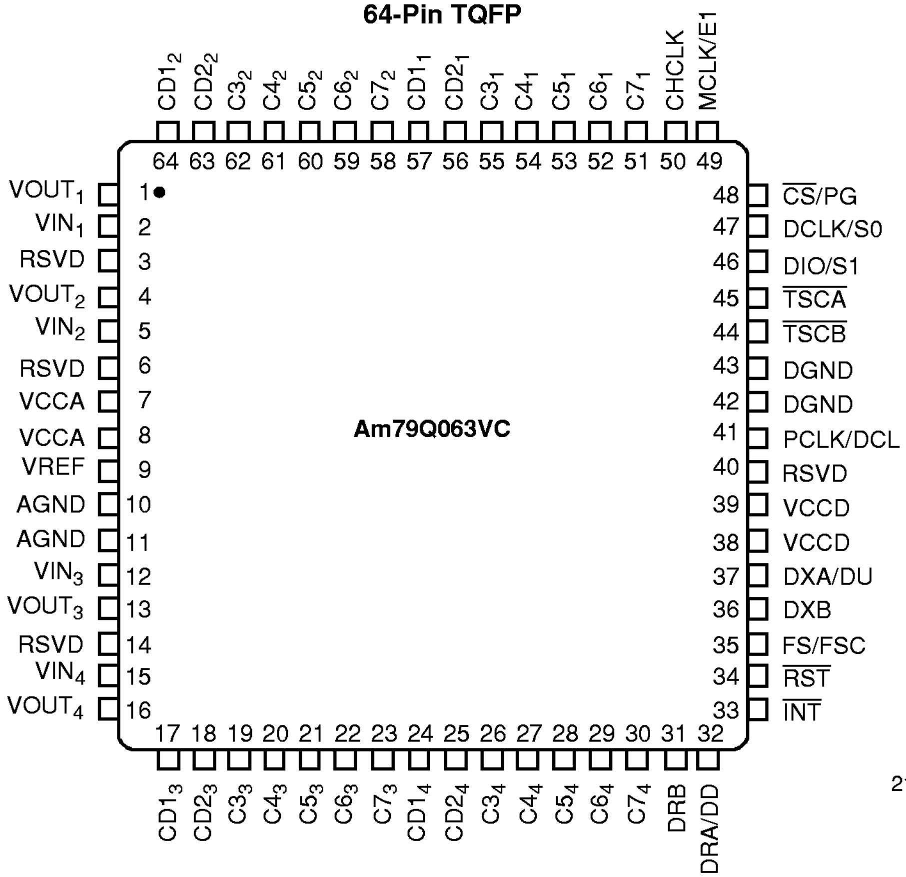
21108A-005

44-Pin TQFP



21108A-006

64-Pin TQFP



21108A-007

Notes:

1. *Pin 1 is marked for orientation.*
2. *RSVD = Reserved pin; should not be connected externally to any signal or supply.*
3. *Pins of same name on Am79Q063VC internally connected (AGND, pins 10, 11; VCCA, pins 7, 8; VCCD, pins 38, 39; DGND, pins 42, 43).*

PIN DESCRIPTIONS

$CD1_1$–$CD1_4$, $CD2_1$–$CD2_4$

Control and Data (Inputs/Outputs)

CD1 and CD2 are TTL compatible programmable Input or Output (I/O) ports. They can be used to monitor or control the state of SLIC or any other device associated with subscriber line interface. The direction, input or output, is programmed using MPI Command 22 or GCI Monitor channel Command 8. As outputs, CD1 and CD2 can be used to control relays, illuminate LEDs, or perform any other function requiring a latched TTL compatible signal for control. In PCM/MPI mode, the output state of CD1 and CD2 is written using MPI Command 20. In GCI mode, the output state of CD1 and CD2 is determined by the C1 and C2 bits contained in the down stream C/I channel for the respective channel. As inputs, CD1 and CD2 can be processed by the QSLAC device (if programmed to do so). CD1 can be debounced before it is made available to the system. The debounce time is programmable from 0 to 15 ms in 1 ms increments using MPI Command 45 and GCI monitor channel Command 11. CD2 can be filtered using the up/down counter facility and programming the sampling interval using MPI Command 52 or GCI SOP Command 12.

Additionally, CD1 can be demultiplexed into two separate inputs using the E1 demultiplexing function. The E1 demultiplexing function of the QSLAC device was designed to interface directly to AMD SLICS supporting the ground key function. With the proper AMD SLIC and the E1 function of the QSLAC enabled, the CD1 bit can be demultiplexed into an Off-Hook/Ring Trip signal and Ground Key signal. In the demultiplex mode, the second bit, Ground Key, takes the place of the CD2 as an input. The demultiplexed bits can be debounced (CD1) or filtered (CD2) as explained previously. A more complete description of CD1, CD2, debouncing, and filtering functions is contained in the *Operating the QSLAC Device* section on page 31.

Once the CD1 and CD2 inputs are processed (Debounced, Filtered and/or Demultiplexed) by the QSLAC device, the information can be accessed by the system in two ways in the PCM/MPI mode: 1) on a per channel basis along with C3, C4, and C5 of the specific channel using MPI Command 21, or 2) by using MPI Commands 16 and 17, which obtain the CD1 and CD2 bits from all four channels simultaneously. This feature reduces the processor overhead and the time required to retrieve time-critical signals from the line circuits, such as off-hook and ring trip. With this feature, hookswitch status and ring trip information, for example, can be obtained from all four channels of a QSLAC device with one read command. In the GCI mode, the processed CD1 and CD2 inputs are transmitted upstream on the CD1 and CD2 bits for the respective analog channel, 1 or 2, using the C/I channel.

$C3_1$–$C3_4$, $C4_1$–$C4_4$, $C5_1$–$C5_4$

Control (Inputs/Outputs)

C3, C4, and C5 are TTL-compatible programmable Input or Output (I/O) ports. They can be used to monitor or control the state of SLIC or any other device associated with subscriber line interface. The direction, input or output, is programmed using MPI Command 22 or GCI Monitor channel Command 8. As outputs, C3, C4, and C5 can be used to control relays, illuminate LEDs, or perform any other function requiring a latched TTL compatible signal for control. In PCM/MPI mode, the output state of C3, C4, and C5 is written using MPI Command 20. In GCI mode, the output state of C3, C4, and C5 is determined by the C3, C4, and C5 bits contained in the down stream C/I channel for the respective analog channel. As inputs, C3, C4, and C5 can be accessed by the system in PCM/MPI mode by using MPI Command 21. In GCI mode, C3 is transmitted upstream, along with CD1 and CD2, for the respective analog channel using C3 of the C/I channel. Also, in GCI mode, C3, C4, and C5 can be read along with CD1 and CD2 using Monitor channel Command 10.

The Am79Q061 QSLAC device contains a single PCM highway or GCI Interface and five programmable I/Os per channel (CD1, CD2, C3, C4, and C5) in a 44-pin PLCC or TQFP package. In the Am79Q06 QSLAC device, the $C5_1$, $C5_2$, $C5_3$, and $C5_4$ I/Os are eliminated, enabling dual PCM highways or a GCI interface and a chopper clock output in a 44-pin PLCC or TQFP package. In the Am79Q062 QSLAC device, the $C3_1$–$C5_1$, $C3_2$–$C5_2$, $C3_3$–$C5_3$, and $C3_4$–$C5_4$ I/Os are eliminated, enabling a single PCM highway or GCI Interface and two control and data I/Os (CD1, CD2) per channel in a 32-pin PLCC package.

$C6_1$–$C6_4$, $C7_1$–$C7_4$

Control (Outputs)

Two additional outputs per channel are available on the Am79Q063VC device.

CHCLK

Chopper Clock (Output)

This output provides a 256 kHz or a 292.57 kHz, 50% duty cycle, TTL-compatible clock for use by up to four SLICs with built-in switching regulators. The CHCLK frequency is synchronous to MCLK/DCL (MCLK in PCM mode, DCL in GCI mode), but the phase relationship to MCLK/DCL is random. The chopper clock is not available in all package types.

$\overline{\text{CS}}$/PG

Chip Select/PCM-GCI (Input)

The $\overline{\text{CS}}$/PG input along with the DCLK/S0 input are used to determine the operating state of the programmable PCM/GCI interface. On power up, the QSLAC device will initialize to GCI mode if $\overline{\text{CS}}$/PG is low *and* there is no toggling (no high to low or low to high transitions) of the DCLK/S0 input. The device will initialize to the PCM/MPI mode if either $\overline{\text{CS}}$ is high *or* DCLK is toggling.

Once the device is in PCM/MPI mode, it is ready to receive commands through its serial interface pins, DIO and DCLK. Once a valid command has been sent through the MPI serial interface, GCI mode cannot be entered unless a hardware reset is asserted or power is removed from the part. If a valid command has not been sent since the last hardware reset or power up, then GCI mode can be re-entered (after a delay of one PCM frame) by holding $\overline{\text{CS}}$/PG low and keeping DCLK static. While the part is in GCI mode, then $\overline{\text{CS}}$/PG going high or DCLK toggling will immediately place the device in PCM/MPI mode.

In the PCM/MPI mode, the Chip Select input (active Low) enables the device so that control data can be written to or read from the part. The channels selected for the write or read operation are enabled by writing 1s to the appropriate bits in the Channel Enable Register of the QSLAC device prior to the command. See EC1, EC2, EC3, and EC4 of the Channel Enable Register and Command 14 for more information. If Chip Select is held Low for 16 rising edges of DCLK, a hardware reset is executed when Chip Select returns High.

DCLK/S0

Data Clock (Input)

In addition to providing both a data clock input and an S0 GCI address input, DCLK/S0 acts in conjunction with $\overline{\text{CS}}$/PG to determine the operational mode of the system interface, PCM/MPI or GCI. See $\overline{\text{CS}}$/PG for details.

In the PCM/MPI mode, the Data Clock input shifts data into and out of the microprocessor interface of the QSLAC device. The maximum clock rate is 4.096 MHz and the minimum clock rate is 10 kHz.

Select Bit 0 (Input)

In GCI mode, S0 is one of two inputs (S0, S1) that is decoded to determine which GCI channels the QSLAC transmit and receives data on.

DIO/S1

Data Input Output (Input)

In the PCM/MPI mode, control data is serially written into and read out of the QSLAC device via the DIO pin, most significant bit first. The Data Clock determines the data rate. DIO is high impedance except when data is being transmitted from the QSLAC device.

Select Bit 1 (Input)

In GCI mode, S1 is the second of two inputs (S0, S1) that is decoded to determine which GCI channels the QSLAC transmits and receives data on.

DRA, DRB/DD

PCM Data Receive (A/B) (Inputs)

In the PCM/MPI mode, the PCM data for Channels 1, 2, 3, and 4 is serially received on either the DRA or DRB port during user-programmed time slots. Data is always received with the most significant bit first. For compressed signals, 1 byte of data for each channel is received every 125 μs at the PCLK rate. In the Linear mode, 2 consecutive bytes of data for each channel are received every 125 μs at the PCLK rate. DRB is not available on all package types.

GCI Data Downstream (Input)

In GCI mode, the B1, B2, Monitor and SC channel data is serially received on the Data Downstream input for all four channels of the QSLAC device. The QSLAC device requires two of the eight GCI channels for operation. The two GCI Channels, out of the eight possible, are determined by the S0 and S1 inputs. Data is always received with the most significant bit first. 4 bytes of data for each GCI channel is received every 125 μs at the 2.048 Mbit/s data rate.

DXA, DXB/DU

PCM Data Transmit (Outputs)

In the PCM/MPI mode, the transmit data from Channels 1, 2, 3, and 4 is sent serially out on either the DXA or DXB port or on both ports during user-programmed time slots. Data is always transmitted with the most significant bit first. The output is available every 125 μs and the data is shifted out in 8-bit (16-bit in Linear or PCM Signaling mode) bursts at the PCLK rate. DXA and DXB are High impedance between time slots, while the device is in the Inactive mode with no PCM signaling, or while the Cutoff Transmit Path bit (CTP) is on. DXB is not available on all package types.

GCI Data Upstream (Output)

In the GCI mode, the B1, B2, Monitor and SC channel data is serially transmitted on the Data Upstream output for all four channels of the QSLAC device. Which GCI channels the device uses is determined by the S0 and S1 inputs. Data is always transmitted with the most significant bit first. 4 bytes of data for each GCI channel is transmitted every 125 μs at the DCL rate.

FS/FSC

Frame Sync (Input)

In the PCM/MPI mode, the Frame Sync (FS) pulse is an 8 kHz signal that identifies Time Slot 0 and Clock Slot 0 of a system's PCM frame. The QSLAC device references individual time slots with respect to this input, which must be synchronized to PCLK.

Frame Sync (Input)

In GCI mode, the Frame Sync (FSC) pulse is an 8 kHz signal that identifies the beginning of GCI channel 0 of a system's GCI frame. The QSLAC device references individual GCI channels with respect to this input, which must be synchronized to DCL.

$\overline{\text{INT}}$

Interrupt (Output)

$\overline{\text{INT}}$ is an active Low output signal, which is programmable as either TTL-compatible or open drain. The $\overline{\text{INT}}$ output goes Low any time one of the input bits in the Real Time Data register changes state and is not masked. It also goes Low any time new transmit data appears if this interrupt is armed. $\overline{\text{INT}}$ remains Low until the appropriate register is read via the microprocessor interface, or the QSLAC device receives either a software or hardware reset. The individual CDx_y bits in the Real Time Data register can be masked from causing an interrupt by using MPI Command 26 or SOP Command 14. The transmit data interrupt must be armed with a bit in the Operating Conditions Register.

MCLK/E1

Master Clock (Input)/Enable CD1 Multiplex (Output)

In PCM/MPI mode only, the Master Clock can be a 1.536 MHz, 1.544 MHz, or 2.048 MHz (times 1, 2, or 4) clock for use by the digital signal processor. MCLK may be asynchronous to PCLK. If the internal clock is derived from the PCM Clock Input (PCLK) or if GCI mode is selected, this pin can be used as an E1 output to control AMD SLICs having multiplexed switchhook and ground key detector outputs.

PCLK/DCL

PCM Clock (Input)

In the PCM/MPI mode, the PCM clock determines the rate at which PCM data is serially shifted into or out of the PCM ports. PCLK is an integer multiple of the frame sync frequency. The maximum clock frequency is 8.192 MHz and the minimum clock frequency is 128 kHz for dual PCM highway versions and 256 kHz for single PCM highway versions. The minimum clock rate must be doubled if Linear mode or PCM signaling is used. PCLK frequencies between 1.03 MHz and 1.53 MHz are not allowed. The PCLK clock may be asynchronous to MCLK. Optionally, the digital signal processor clock can be derived from PCLK rather than MCLK. In PCM/MPI mode, PCLK can be operated at twice the PCM data rate in the Double PCLK mode (bit 1 of PCM/MPI Command 45).

GCI Data Clock (Input)

In GCI mode, DCL is either 2.048 MHz or 4.096 MHz, which is an integer multiple of the frame sync frequency. Circuitry internal to the QSLAC device monitors this input to determine which frequency is being used, 2.048 MHz or 4.096 MHz. When 4.096 MHz clock operation is detected, internal timing is adjusted so that DU and DD operate at the 2.048 Mbit/s rate.

$\overline{\text{RST}}$

Reset (Input)

A logic Low signal at this pin resets the QSLAC device to its default state.

$\overline{\text{TSCA}}$, $\overline{\text{TSCB}}$

Time Slot Control (Outputs)

The Time Slot Control outputs are open drain outputs (requiring pull-up resistors to V_{DCC}) and are normally inactive (high impedance). In the PCM/MPI mode, $\overline{\text{TSCA}}$ or $\overline{\text{TSCB}}$ is active (low) when PCM data is transmitted on the DXA or DXB pin respectively. In GCI mode, $\overline{\text{TSCA}}$ is active (low) during the two GCI time slots selected by the S1 and S0. $\overline{\text{TSCB}}$ is not available on all package types.

VIN_1–VIN_4

Analog (Inputs)

The analog voice band signal is applied to the VIN input of the QSLAC device. The VIN input is biased at VREF by a large internal resistor. The audio signal is sampled, digitally processed and encoded, and then made available at the TTL-compatible PCM output (DXA or DXB) or in the B1 and B2 of the GCI channel. If the digitizer saturates in the positive or negative direction, VIN is pulled by a reduced resistance toward AGND or VCCD, respectively. VIN_1 is the input for Channel 1, VIN_2 is the input for Channel 2, VIN_3 is the input for Channel 3, and VIN_4 is the input for Channel 4.

$VOUT_1$–$VOUT_4$

Analog (Outputs)

The received digital data at DRA/DRB or DD (GCI mode) is processed and converted to an analog signal at the VOUT pin. $VOUT_1$ is the output from Channel 1, $VOUT_2$ is the output for Channel 2, $VOUT_3$ is the output from Channel 3, and $VOUT_4$ is the output for Channel 4. The VOUT voltages are referenced to VREF.

VREF

Analog Voltage Reference (Output)

The VREF output is provided in order for an external 0.1 μF capacitor to be connected from VREF to ground, filtering noise present on the internal voltage reference. VREF is buffered before it is used by internal circuitry. The voltage on VREF is nominally 2.1 V, and the output resistance is 100 kΩ ±30%. The leakage current in the capacitor must be less than 20 nA.

Power Supply for the Am79Q06X

AGND	Analog Ground
DGND	Digital Ground
VCCA	+5 V Analog Power Supply
VCCD	+5 V Digital Power Supply

Two separate power supply inputs allow for noise isolation and proper power supply decoupling techniques; however, the two pins have a low impedance connection inside the part. For best performance, connect all of the +5 V power supply pins together at the connector of the printed circuit board, and all of the grounds should be connected together at the connector of the printed circuit board.

FUNCTIONAL DESCRIPTION

The QSLAC device performs the codec/filter and two- to four-wire conversion functions required of the subscriber line interface circuitry in telecommunications equipment. These functions involve converting audio signals into digital PCM samples and converting digital PCM samples back into audio signals. During conversion, digital filters are used to band limit the voice signals. All of the digital filtering is performed in digital signal processors operating from a master clock, which can be derived either from PCLK or MCLK in the PCM/MPI mode and DCL in the GCI mode.

Four independent channels allow the QSLAC device to function as two DSLAC devices. In the PCM/MPI mode, each channel has its own enable bit (EC1, EC2, EC3, and EC4) to allow individual channel programming. If more than one Channel Enable bit is High or if all Channel Enable bits are High, all channels enabled will receive the programming information written; therefore, a Broadcast mode can be implemented by simply enabling all channels in the device to receive the information. The Channel Enable bits are contained in the Channel Enable Register, which is written and read using Commands 14 and 15. The Broadcast mode is useful in initializing QSLAC devices in a large system.

In GCI mode, one GCI channel controls two channels of the QSLAC device. The Monitor channel and SC channel within the GCI channel are used to read/write filter coefficient data, read/write operating conditions and to read/write data to/from the programmable I/O ports of the two channels. Two consecutive GCI channels control all four channels of the QSLAC device. The two GCI channels used, of the eight total available, are determined by S0 and S1 inputs.

The user-programmable filters set the receive and transmit gain, perform the transhybrid balancing function, permit adjustment of the two-wire termination impedance, and provide equalization of the receive and transmit paths. All programmable digital filter coefficients can be calculated using the AmSLAC4 or WinSLAC™ software.

In PCM/MPI mode, Data transmitted or received on the PCM highway can be 8-bit companded code (with an optional 8-bit signaling byte in the transmit direction) or 16-bit linear code. The 8-bit codes appear 1 byte per time slot, while the 16-bit code appears in two consecutive time slots. The compressed PCM codes can be either 8-bit companded A-law or μ-law. The PCM data is read from and written to the PCM highway in user-programmable time slots at rates of 128 kHz to 8.192 MHz. The transmit clock edge and clock slot can be selected for compatibility with other devices that can be connected to the PCM highway.

In GCI mode, two 8-bit companded codes are received or transmitted per GCI channel. The compressed PCM codes can be either 8-bit companded A-law or μ-law. There is no Signaling or Linear mode available when GCI mode is selected.

Three configurations of the QSLAC device are offered with single or dual PCM highways (PCM/MPI mode) in PLCC packages, shown in *Connection Diagrams* on page 7 and page 8. The Am79Q06JC and Am79Q061JC, with dual and single PCM highways, respectively, are available in the 44-pin PLCC package. The Am79Q062 is a single PCM highway version in a 32-pin package. All 32- and 44-pin packaging options include the programmable GCI interface as an option.

PCM/GCI Highway	Programmable I/O	Chopper Clock	Package	Part Number
Dual/Single*	Four	Yes	44 PLCC/TQFP	Am79Q06V, JC
Single/Single	Five	No	44 PLCC/TQFP	Am79Q061V, JC
Single/Single	Two	No	32 PLCC	Am79Q062JC
Dual/Single	Seven	Yes	64 TQFP	Am79Q063VC

Note:
** Dual PCM highways in PCM mode. Single GCI interface in GCI mode.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... –60°C < T_A < +125°C

Ambient Operating Temperature .... –40°C < T_A < +85°C

Ambient Relative Humidity...... 5% to 95% (non condensing)

VCCA with respect to AGND ....–0.4 V to +7.0 V

VCCA with respect to VCCD................................... ±50 mV

VCCD with respect to DGND......................–0.4 V to +7.0 V

VIN with respect to AGND ....–0.4 V to VCCA +0.4 V

AGND with respect to DGND..................................... ±0.4 V

Other pins ......with respect to DGND–0.4 V to VCCD +0.4 V

Total combined CD1–C5 current per device:

- Source from VCCD... 40 mA
- Sink into DGND .... 40 mA
- Latch-up immunity (any pin) .... ±30 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

VCCA, Analog Supply .... +5.0 V ±0.25 V

VCCA, Analog Supply ....VCCD ±10 mV

VCCD, Digital Supply .... +5.0 V ±0.25 V

DGND... 0 V

AGND..±50 mV

Ambient Temperature ....0°C < T_A < +70°C

Ambient Relative Humidity................................15% to 95%

Operating Ranges define those limits between which functionality of the device is guaranteed by production testing.

Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.

ELECTRICAL CHARACTERISTICS over operating range (unless otherwise noted)

Typical values are for T_A = 25°C and nominal supply voltages. Minimum and maximum specifications are over the temperature and supply voltage ranges shown in Operating Ranges.

Symbol	Parameter Descriptions	Min	Typ	Max	Unit
V_{IL}	Input Low voltage			0.8	V
V_{IH}	Input High voltage	2.0			
I_{IL}	Input leakage current	–10		+10	µA
V_{OL}	Output Low voltage CD1–C7 (I_{OL} = 4 mA) CD1–C7 (I_{OL} = 8 mA) (Note 1) $\overline{TSCA}$, $\overline{TSCB}$ (I_{OL} =14 mA) Other digital outputs (I_{OL} = 2 mA)			 0.4 0.8 0.4 0.4	V
V_{OH}	Output High voltage CD1–C7 (I_{OH}=4 mA) CD1–C7 (I_{OH}= 8 mA[1] Other digital outputs (I_{OH} = 400 µA)	 VCCD – 0.4 V VCCD – 0.8 V 2.4			
I_{OL}	Output leakage current (H_I = Z State)	–10		10	µA
V_{IR}	Analog input voltage range (AX = 0 dB) (Relative to VREF) (AX = 6.02 dB)		±1.584 ±0.792		Vpk
V_{IOS}	Offset voltage allowed on VIN	–50		50	mV
Z_{IN}	Analog input impedance to VREF300 to 3400 Hz	0.43		3.4	MΩ
I_{IP}	Current into analog input for input voltages 3.8 V to 5.0 V[2]	54		170	µA
I_{IN}	Current out of analog input for input voltages 0 V to 0.5 V[2]	50		170	
Z_{OUT}	VOUT output impedance		1	10	Ω
I_{OUT}	VOUT output current (F< 3400 Hz)[3]	–4		4	mA
Z_{REF}	VREF output impedance (F < 3400 Hz)	70		130	kΩ
V_{OR}	VOUT voltage range (AR = 0 dB) (Relative to VREF) (AR = 6.02 dB)		±1.584 ±0.792		Vpk
V_{OOS}	VOUT offset voltage (AISN off)	–40		40	mV
V_{OOSA}	VOUT offset voltage (AISN on)[4]	–80		80	
LIN_{AISN}	Linearity of AISN circuitry (input = 0 dBm0)	–0.25		0.25	LSB
PD	Power dissipation All channels active 1 channel active All channels inactive, (in normal state) All channels inactive (in low power state, see Note 5)		 200 70 18 6	 260 130 25 12	mW
C_I	Input capacitance (Digital)		15		pF
C_O	Output capacitance (Digital)		15		
PSRR	Power supply rejection ratio (1.02 kHz, 100 mV_{RMS}, either path, GX=GR=0 dB)	40			dB

Notes:

1. *The CD1, CD2, C3–C7 outputs are resistive for less than a 0.8 V drop. Total current must not exceed absolute maximum ratings.*
2. *When the digitizer saturates, a resistor of 50 kΩ ±20 kΩ is connected either to DGND or to VCCD – (1 diode drop) as appropriate to discharge the coupling capacitor.*
3. *When the QSLAC device is in the Inactive mode, the analog output presents a VREF DC output level through a 15 kΩ resistor.*
4. *If there is an external DC path from VOUT to VIN with a gain of G_{DC} and the AISN has a gain of h_{AISN}, then the output offset is multiplied by $1/[1-(h_{AISN} \bullet G_{DC})]$.*
5. *Power dissipation in the Inactive mode is measured with all digital inputs at $V_{IH} = V_{CC}$ and V_{IL} = DGND and with no load connected to $VOUT_1$, $VOUT_2$, $VOUT_3$, or $VOUT_4$.*

Transmission Characteristics

Table 1. dBm0 Voltage Definitions with Unity Gain in X, R, GX, GR, AX, and AR

Signal at Digital Interface	Transmit	Receive	Unit
A-law digital mW or equivalent (0 dBm0)	0.7804	0.7804	Vrms
µ-law digital mW or equivalent (0 dBm0)	0.7746	0.7746	
±22,827 peak linear coded sine wave	0.7804	0.7804	

When relative levels (dBm0) are used in the following transmission specifications, the specification holds for any setting of the AX + GX gain from 0–12 dB and the AR + GR loss from 0–12 dB.

Description	Test Conditions	Min	Typ	Max	Unit	Note
Gain accuracy D/A or A/D	0 dBm0, 1014 Hz				dB	
	AX = AR = 0 dB					
	0 to 85°C	–0.25		+0.25		
	–40°C	–0.30		+0.30		
	AX = +6.02 dB and /or AR = –6.02 dB					
	0 to 85°C	–0.30		+0.30		
	–40°C	–0.40		+0.40		
Gain accuracy digital-to-digital		–0.25		+0.25		
Gain accuracy analog-to-analog		–0.25		+0.25		
Attenuation distortion	300 Hz to 3 kHz	–0.125		+0.125		1
Single frequency distortion				–46		2
Idle channel noise						
Analog out	Digital looped back weighted			–68	dBm0p	3
	unweighted			–55	dBm0	3
	Digital input = 0 A-law			–78	dBm0p	3
	Digital input = 0 µ-law		0	12	dBrnc0	3, 6
Digital out	Analog V_{IN} = 0 VAC A-law			–68	dBm0p	3
	Analog V_{IN} = 0 VAC µ-law		0	16	dBrnc0	3, 6
Crosstalk same channel					dBm0	
TX to RX	0 dBm0300 Hz to 3400 Hz			–75		
RX to TX	0 dBm0300 Hz to 3400 Hz			–75		
Crosstalk between channels	0 dBm0					
TX or RX to TX	1014 Hz, Average			–76		4
TX or RX to RX	1014 Hz, Average			–78		
End-to-end group delay	B = Z = 0; X = R = 1			678	µs	5

Notes:

1. *Also see Figure 1 and Figure 2.*
2. *0 dBm0 input signal, 300 Hz to 3400 Hz; measurement at any other frequency, 300 Hz to 3400 Hz.*
3. *No single frequency component in the range above 3800 Hz may exceed a level of –55 dBm0.*
4. *The weighted average of the crosstalk is defined by the following equation, where C(f) is the crosstalk in dB as a function of frequency, f_N = 3300 Hz, f_1 = 300 Hz, and the frequency points (f_j, j = 2..N) are closely spaced:*

$$\text{Average} = 20 \bullet \log \left[\frac{\sum_j \frac{10^{\frac{1}{20} \bullet C(f_j)} + 10^{\frac{1}{20} \bullet C(f_{j-1})}}{2} \bullet \log\left(\frac{f_j}{f_{j-1}}\right)}{\log\left(\frac{f_N}{f_1}\right)} \right]$$

5. *The End-to-End Group Delay is the sum of the transmit and receive group delays (measured using same time and clock slot).*
6. *Typical values not tested in production.*

Attenuation Distortion

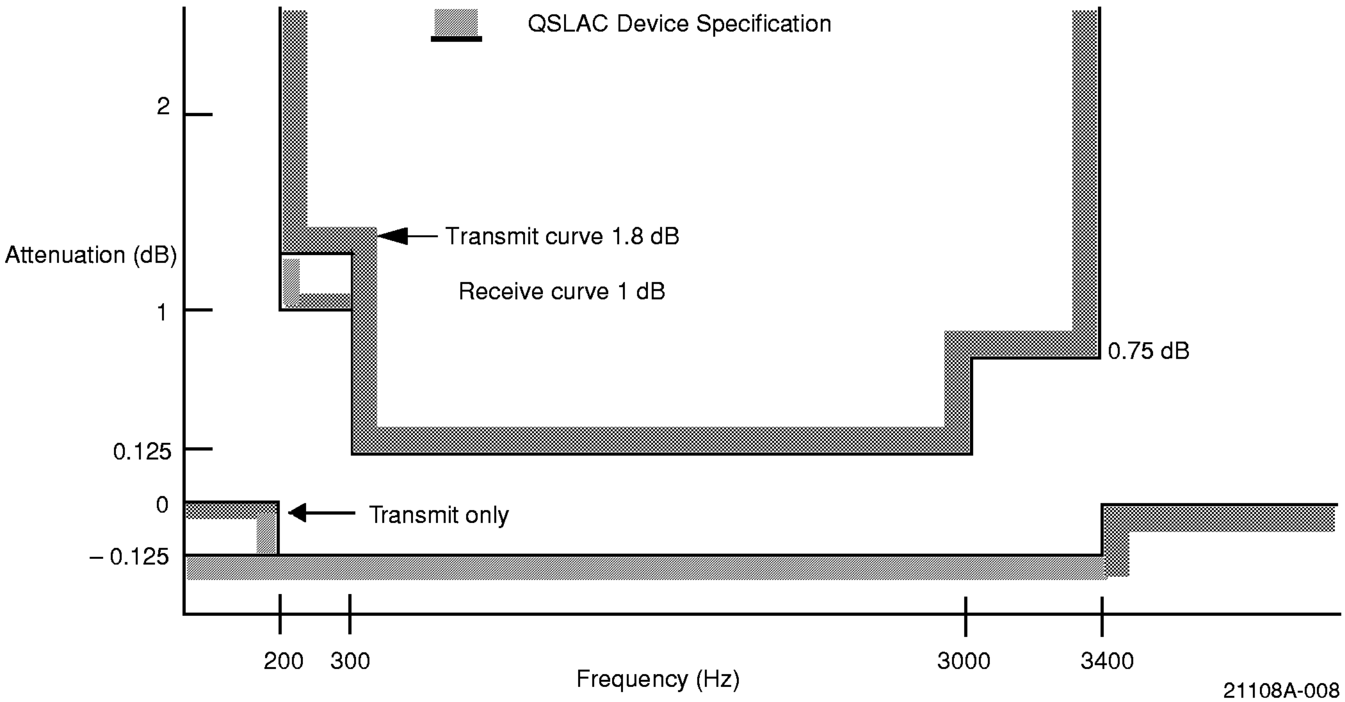


Figure 1. Attenuation Distortion

Group Delay Distortion

For either transmission path, the group delay distortion is within the limits shown in Figure 2. The minimum value of the group delay is taken as the reference. The signal level should be 0 dBm0.

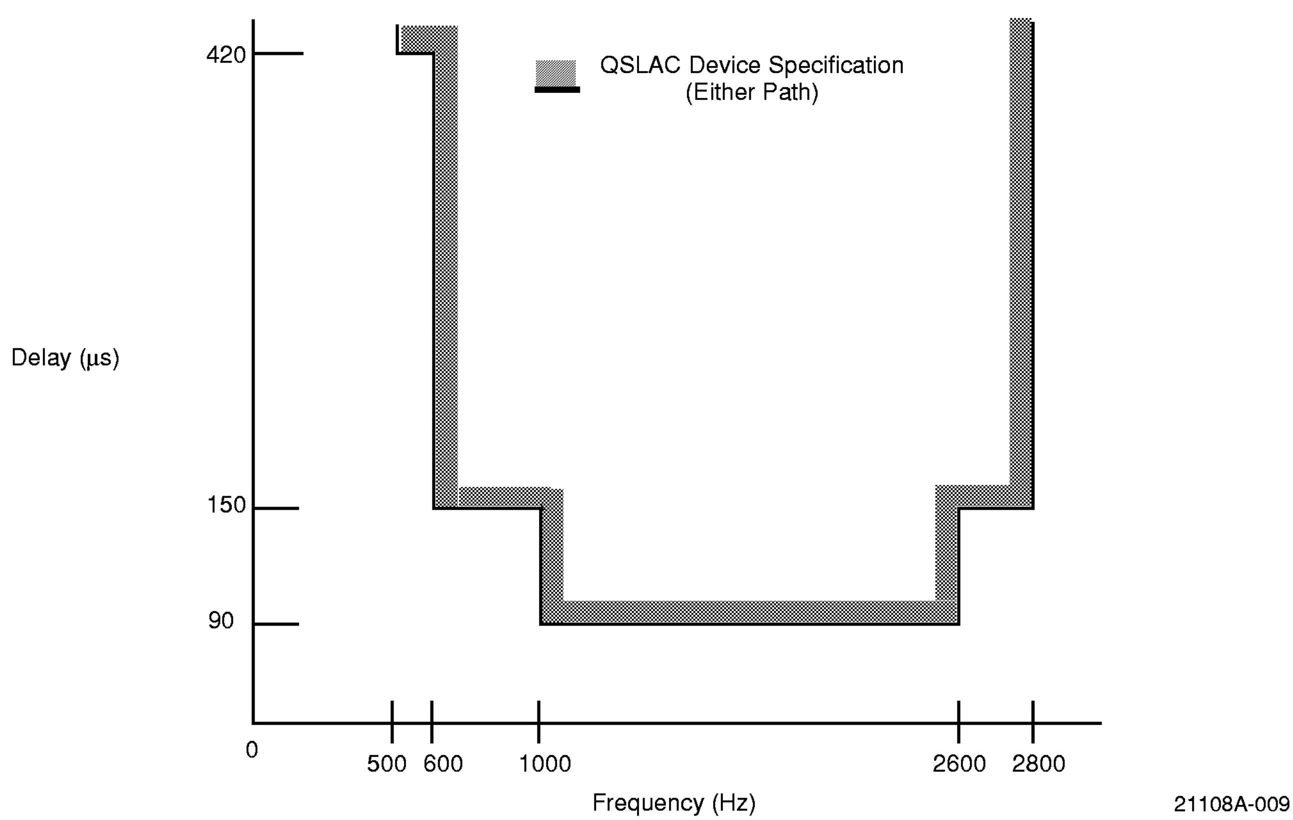
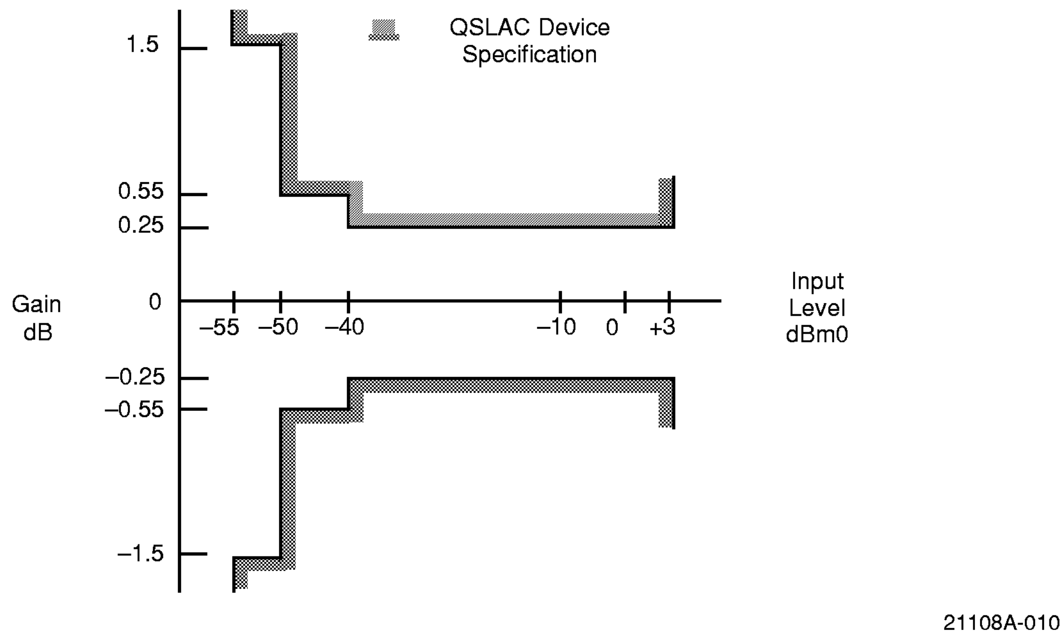


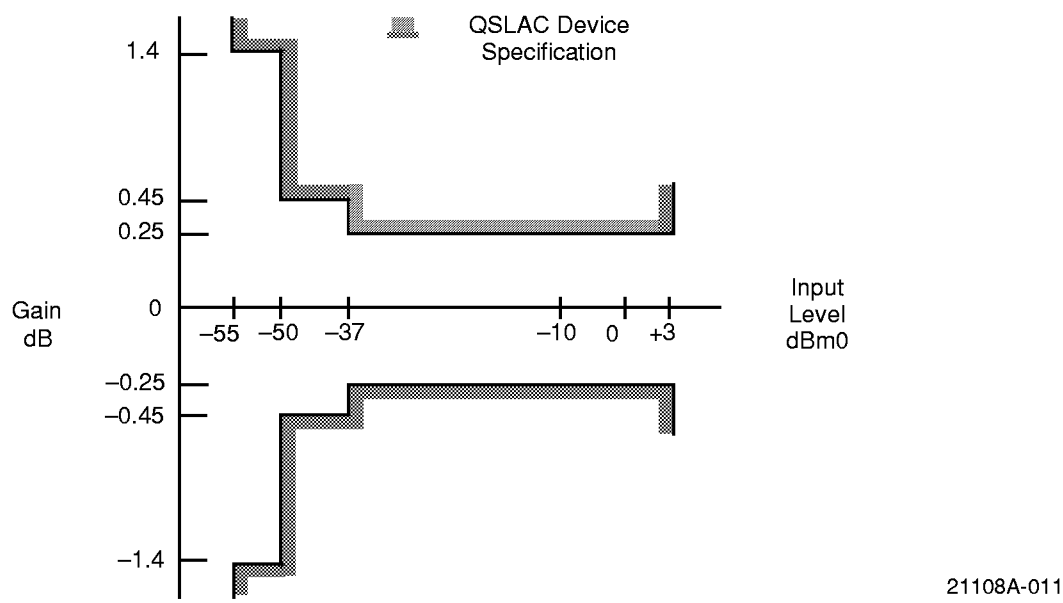
Figure 2. Group Delay Distortion

Variation of Gain with Input Level

The gain deviation relative to the gain at –10 dBm0 is within the limits shown in Figure 3 for either transmission path when the input is a sine wave signal of frequency 1014 Hz.



a. A-law

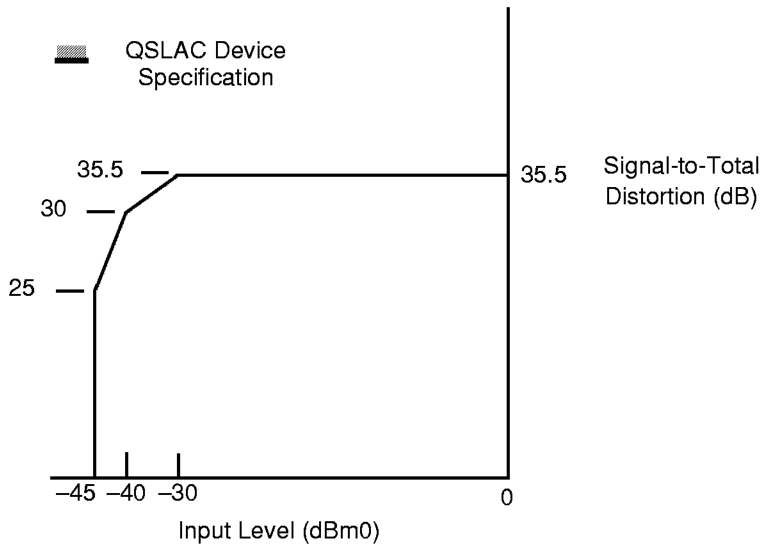


b. μ-law

Figure 3. A-Law/μ-law Gain Tracking with Tone Input (Both Paths)

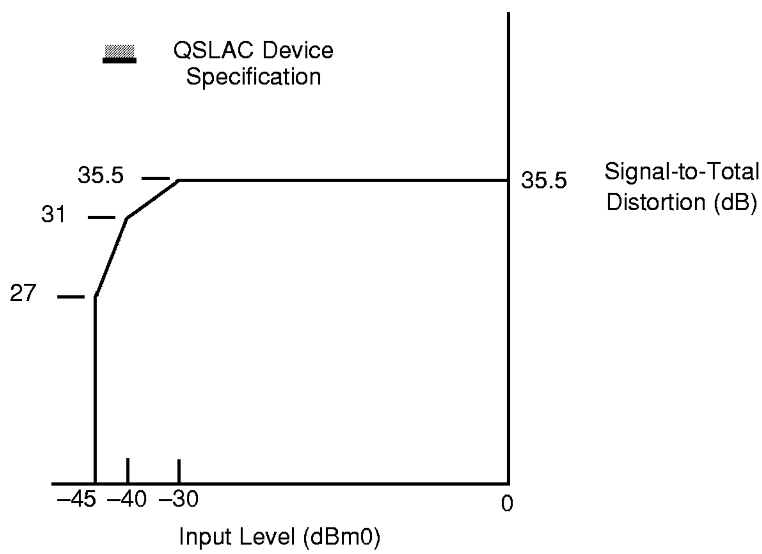
Total Distortion, Including Quantizing Distortion

The signal-to-total distortion will exceed the limits shown in Figure 4 for either transmission path when the input is a sine wave signal of frequency 1014 Hz.



21108A-012

a. A-law



21108A-013

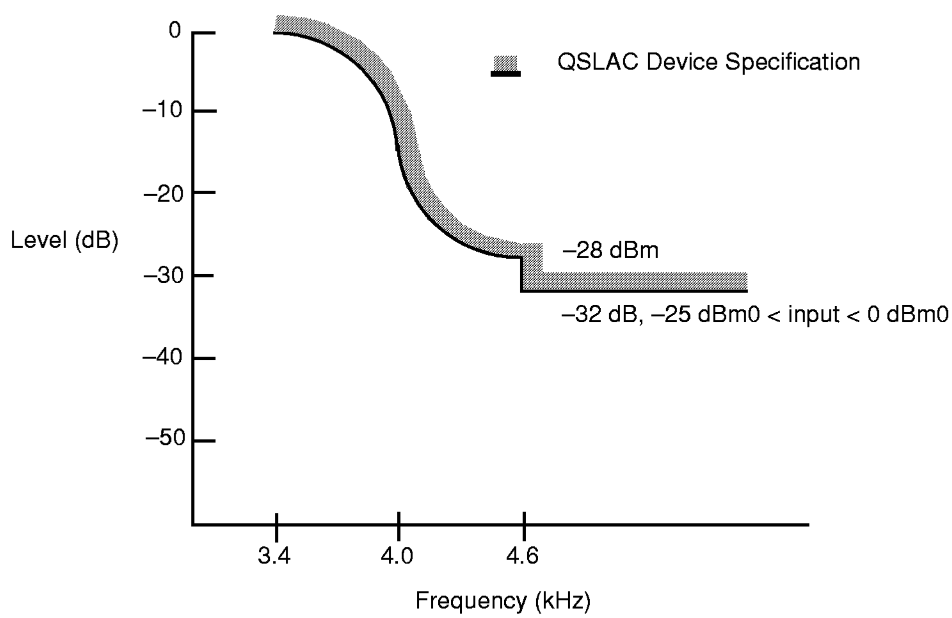
b. μ-law

Figure 4. A-law/μ-law Total Distortion with Tone Input (Both Paths)

Discrimination against Out-of-Band Input Signals

When an out-of-band sine wave signal with frequency and level A is applied to the analog input, there may be frequency components below 4 kHz at the digital output, which are caused by the out-of-band signal. These components are at least the specified dB level below the level of a signal at the same output originating from a 1014 Hz sine wave signal with a level of A dBm0 also applied to the analog input. The minimum specifications are shown in the following table.

Frequency of Out-of-Band Signal	Amplitude of Out-of-Band Signal	Level below A
16.6 Hz < f < 45 Hz	–25 dBm0 < A ≤ 0 dBm0	18 dB
45 Hz < f < 65 Hz	–25 dBm0 < A ≤ 0 dBm0	25 dB
65 Hz < f < 100 Hz	–25 dBm0 < A ≤ 0 dBm0	10 dB
3400 Hz < f < 4600 Hz	–25 dBm0 < A ≤ 0 dBm0	see Figure 5
4600 Hz < f < 100 kHz	–25 dBm0 < A ≤ 0 dBm0	32 dB



Note:
The attenuation of the waveform below amplitude A between 3400 Hz and 4600 Hz is given by the formula:

$$\text{Attenuation (db)} = 14 - 14\sin\frac{\pi(4000 - f)}{1200}$$

Figure 5. Discrimination against Out-of-Band Signals

Discrimination against 12- and 16 kHz Metering Signals

If the QSLAC device is used in a metering application where 12 kHz or 16 kHz tone bursts are injected onto the telephone line toward the subscriber, a portion of these tones also may appear at the VIN terminal. These out-of-band signals may cause frequency components to appear below 4 kHz at the digital output. For a 12 kHz or 16 kHz tone, the frequency components below 4 kHz are reduced from the input by at least 70 dB. The sum of the peak metering and signal voltages must be within the analog input voltage range.

Spurious Out-of-Band Signals at the Analog Output

With PCM code words representing a sine wave signal in the range of 300 Hz to 3400 Hz at a level of 0 dBm0 applied to the digital input, the level of the spurious out-of-band signals at the analog output is less than the limits shown below.

Frequency	Level
4.6 kHz to 40 kHz	–32 dBm0
40 kHz to 240 kHz	–46 dBm0
240 kHz to 1 MHz	–36 dBm0

With code words representing any sine wave signal in the range 3.4 kHz to 4.0 kHz at a level of 0 dBm0 applied to the digital input, the level of the signals at the analog output are below the limits in Figure 6. The amplitude of the spurious out-of-band signals between 3400 Hz and 4600 Hz is given by the formula:

$$A = -14 - 14\sin\frac{\pi(f-4000)}{1200}\,\mathrm{dBm0}$$

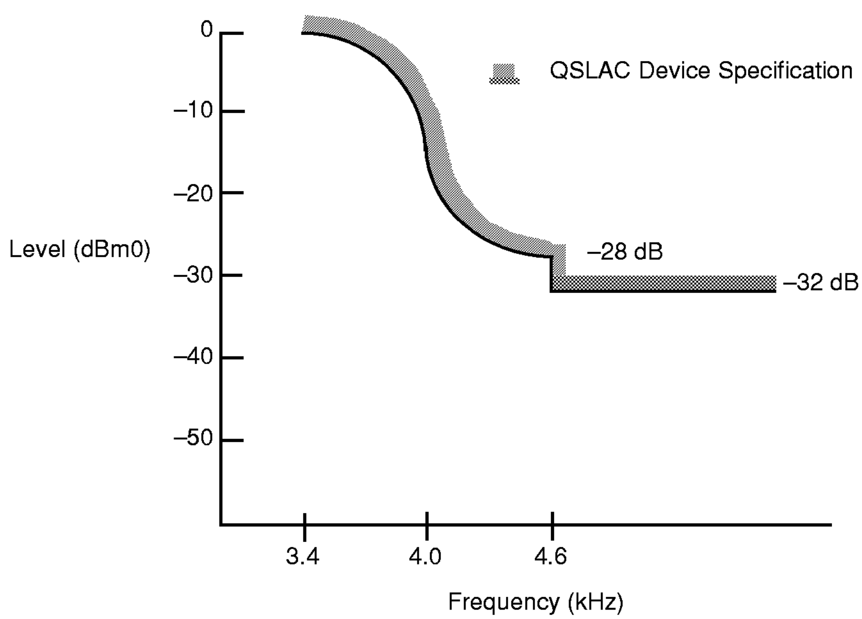


Figure 6. Spurious Out-of-Band Signals

Overload Compression

Figure 7 shows the acceptable region of operation for input signal levels above the reference input power (0 dBm0). The conditions for this figure are:

- 1.2 dB < GX ≤ 12 dB
- –12 dB ≤ GR < –1.2 dB
- PCM output connected to PCM input
- Measurement analog-to-analog

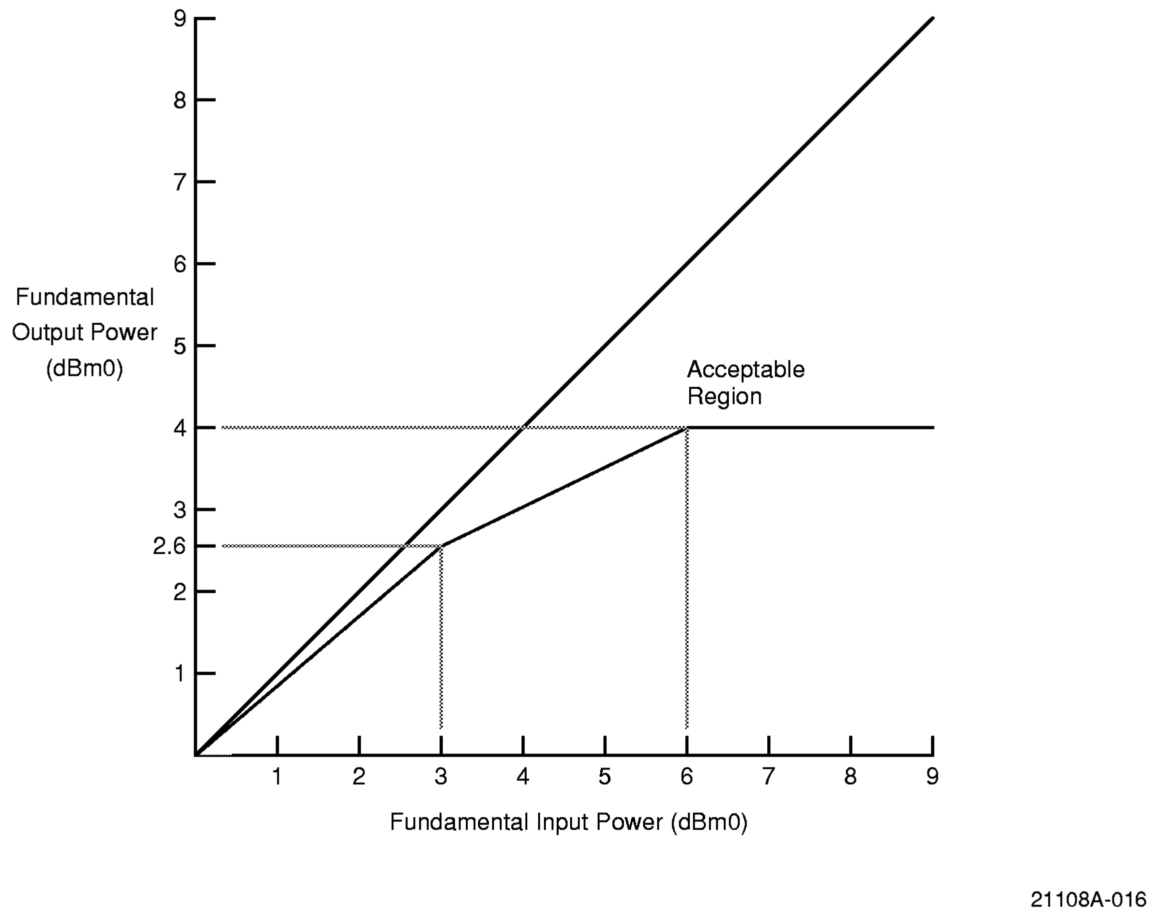


Figure 7. A/A Overload Compression

SWITCHING CHARACTERISTICS (PCM/MPI MODE) over operating range unless otherwise noted

Min and max values are valid for all digital outputs with a 150 pF load, except CD1–C5 with a 30 pF load.

Microprocessor Interface

No.	Symbol	Parameter	Min	Typ	Max	Units
1	t_{DCY}	Data clock period	244		100,000	ns
2	t_{DCH}	Data clock High pulse width	97			
3	t_{DCL}	Data clock Low pulse width	97			
4	t_{DCR}	Rise time of clock			25	
5	t_{DCF}	Fall time of clock			25	
6	t_{ICSS}	Chip select setup time, Input mode	70		t_{DCY} –10	
7	t_{ICSH}	Chip select hold time, Input mode	0		t_{DCH} –20	
8	t_{ICSL}	Chip select pulse width, Input mode		$8t_{DCY}$		
9	t_{ICSO}	Chip select off time, Input mode (Note 1)	2.5			µs
10	t_{IDS}	Input data setup time	30			ns
11	t_{IDH}	Input data hold time	30			
12	t_{OLH}	SLIC output latch valid			1000	
13	t_{OCSS}	Chip select setup time, Output mode	70		t_{DCY} –10	
14	t_{OCSH}	Chip select hold time, Output mode	0		t_{DCH} –20	
15	t_{OCSL}	Chip select pulse width, Output mode		$8t_{DCY}$		
16	t_{OCSO}	Chip select off time, Output mode (Note 1)	2.5			µs
17	t_{ODD}	Output data turn on delay (Note 2)			50	ns
18	t_{ODH}	Output data hold time	0			
19	t_{ODOF}	Output data turn off delay			50	
20	t_{ODC}	Output data valid	0		50	
21	t_{RST}	Reset pulse width	50			µs

PCM Interface

PCLK not to exceed 8.192 MHz, pull-up resistors of 360 Ω are attached to $\overline{TSCA}$ and $\overline{TSCB}$.

No.	Symbol	Parameter	Min	Typ	Max	Units
22	t_{PCY}	PCM clock period (Note 3)	122			ns
23	t_{PCH}	PCM clock High pulse width	48			
24	t_{PCL}	PCM clock Low pulse width	48			
25	t_{PCF}	Fall time of clock			15	
26	t_{PCR}	Rise time of clock			15	
27	t_{FSS}	FS setup time	25		t_{PCY}–50	
28	t_{FSH}	FS hold time	50			
29	t_{FSJ}	FS or PCLK jitter time	–68		+68	
30	t_{TSD}	Delay to $\overline{TSC}$ valid (Note 4)	5		80	
31	t_{TSO}	Delay to $\overline{TSC}$ off (Note 4, 5)	5		80	
32	t_{DXD}	PCM data output delay	5		70	
33	t_{DXH}	PCM data output hold time	5		70	
34	t_{DXZ}	PCM data output delay to High-Z (Note 6)	5		70	
35	t_{DRS}	PCM data input setup time	25			
36	t_{DRH}	PCM data input hold time	5			

Master Clock

No.	Symbol	Parameter	Min	Typ	Max	Unit
37	A_{MCY}	Master clock accuracy	–100		+100	ppM
38	t_{MCR}	Rise time of clock			15	ns
39	t_{MCF}	Fall time of clock			15	ns
40	t_{MCH}	MCLK High pulse width	48			ns
41	t_{MCL}	MCLK Low pulse width	48			ns

Auxiliary Output Clocks

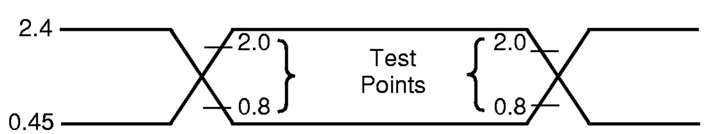
No.	Symbol	Parameter	Min	Typ	Max	Unit
42	f_{CHP}	Chopper clock frequency CHP = 0 CHP = 1		256 292.57		kHz
43	f_{E1}	E1 output frequency (CMODE = EE1 = 1)		4.923		kHz
44	t_{E1}	E1 pulse width (CMODE = EE1 = 1)		31.25		µs

Notes:

1. *If CFAIL = 1 (Command 23), GX, GR, Z, B1, X, R, and B2 coefficients must not be written or read without first deactivating all channels or switching them to default coefficients; otherwise, a chip select off time of 25 µs is required.*
2. *The first data bit is enabled on the falling edge of $\overline{CS}$ or on the falling edge of DCLK, whichever occurs last.*
3. *The PCM clock frequency must be an integer multiple of the frame sync frequency. The maximum allowable PCM clock frequency is 8.192 MHz. The actual PCM clock rate is dependent on the number of channels allocated within a frame. The minimum clock frequency is 128 kHz in Companded mode and 256 kHz in Linear mode or PCM Signaling mode. The minimum PCM clock rates should be doubled for parts with only one PCM highway in order to allow simultaneous access to all four channels.*
4. *$\overline{TSC}$ is delayed from FS by a typical value of $N \cdot t_{PCY}$, where N is the value stored in the time/clock-slot register.*
5. *t_{TSO} is defined as the time at which the output achieves the open circuit condition.*
6. *There is a special conflict detection circuitry that prevents high-power dissipation from occurring when the DXA/DU or DXB pins of two QSLAC devices are tied together and one QSLAC device starts to transmit before the other has gone into a high-impedance state.*

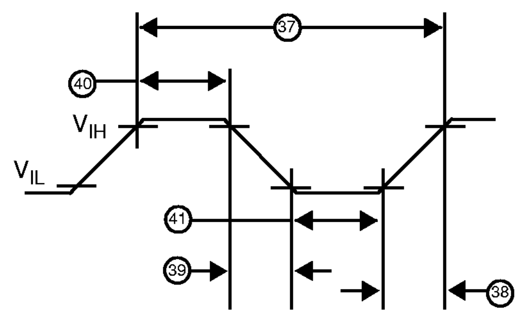
SWITCHING WAVEFORMS

Input and Output Waveforms for AC Tests



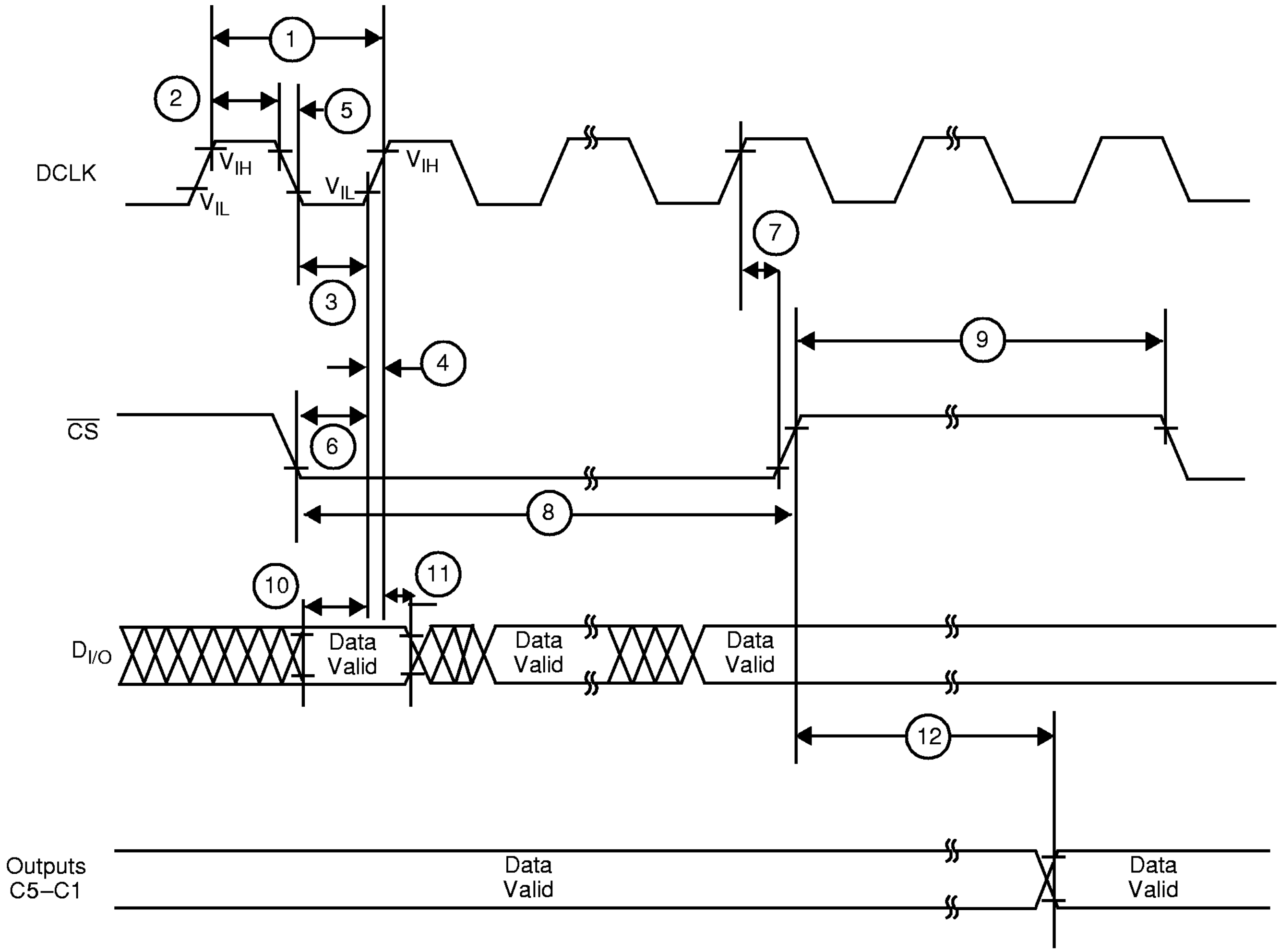
21108A-017

Master Clock Timing



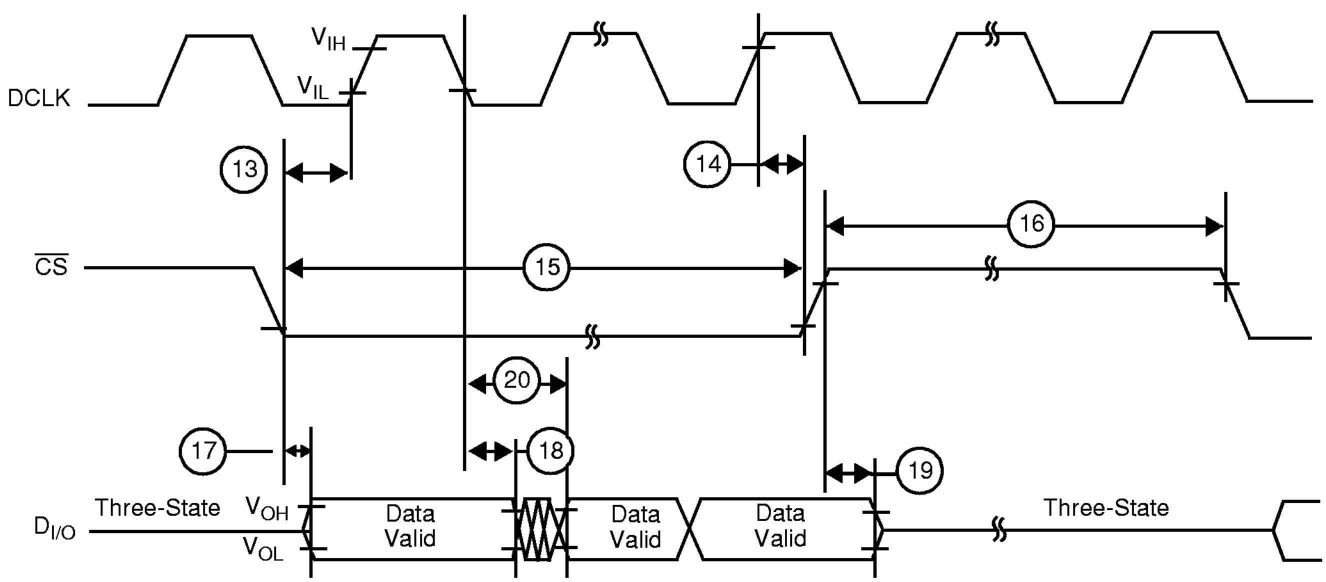
21108A-018

Microprocessor Interface (Input Mode)



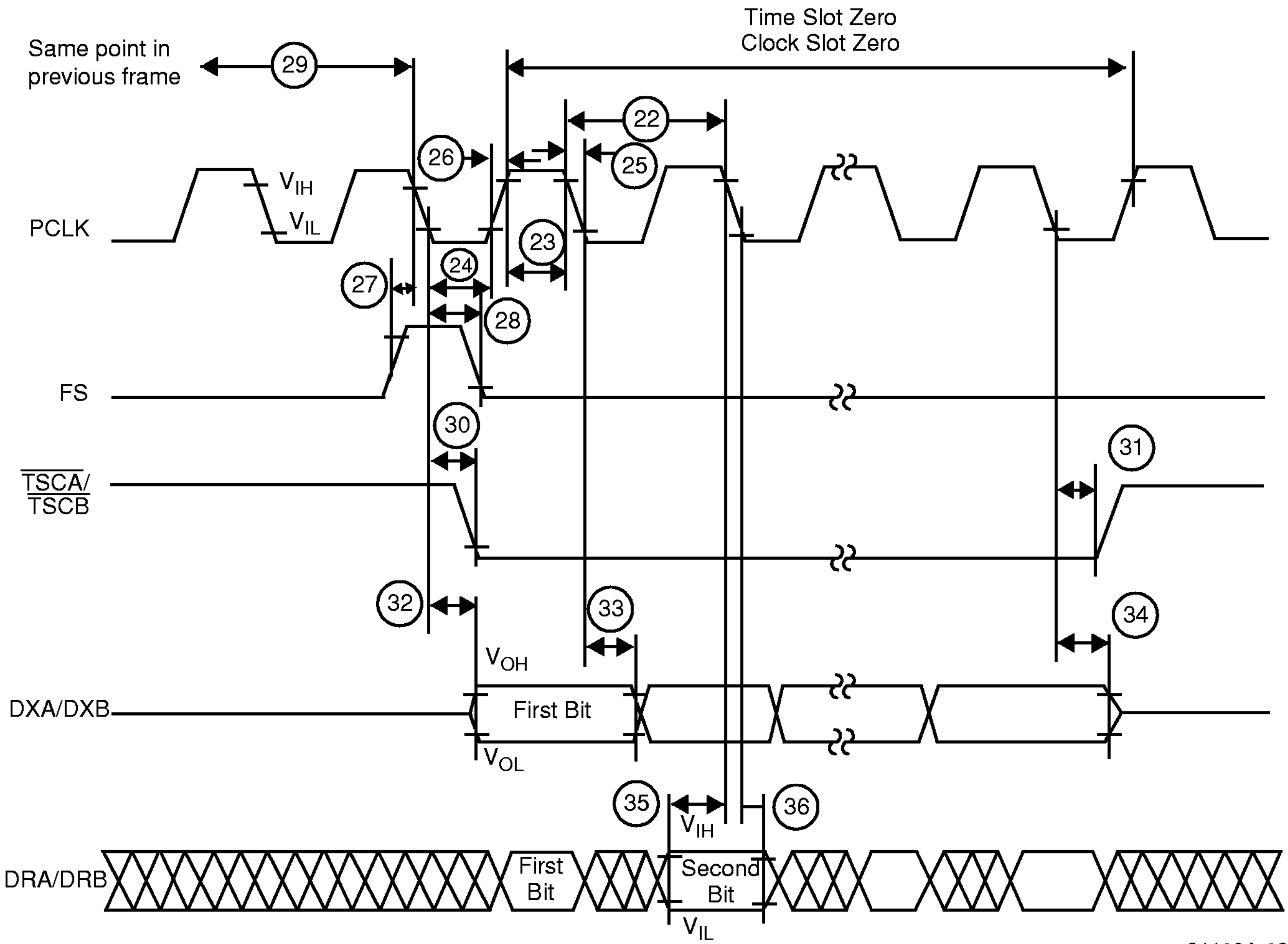
21108-019

Microprocessor Interface (Output Mode)



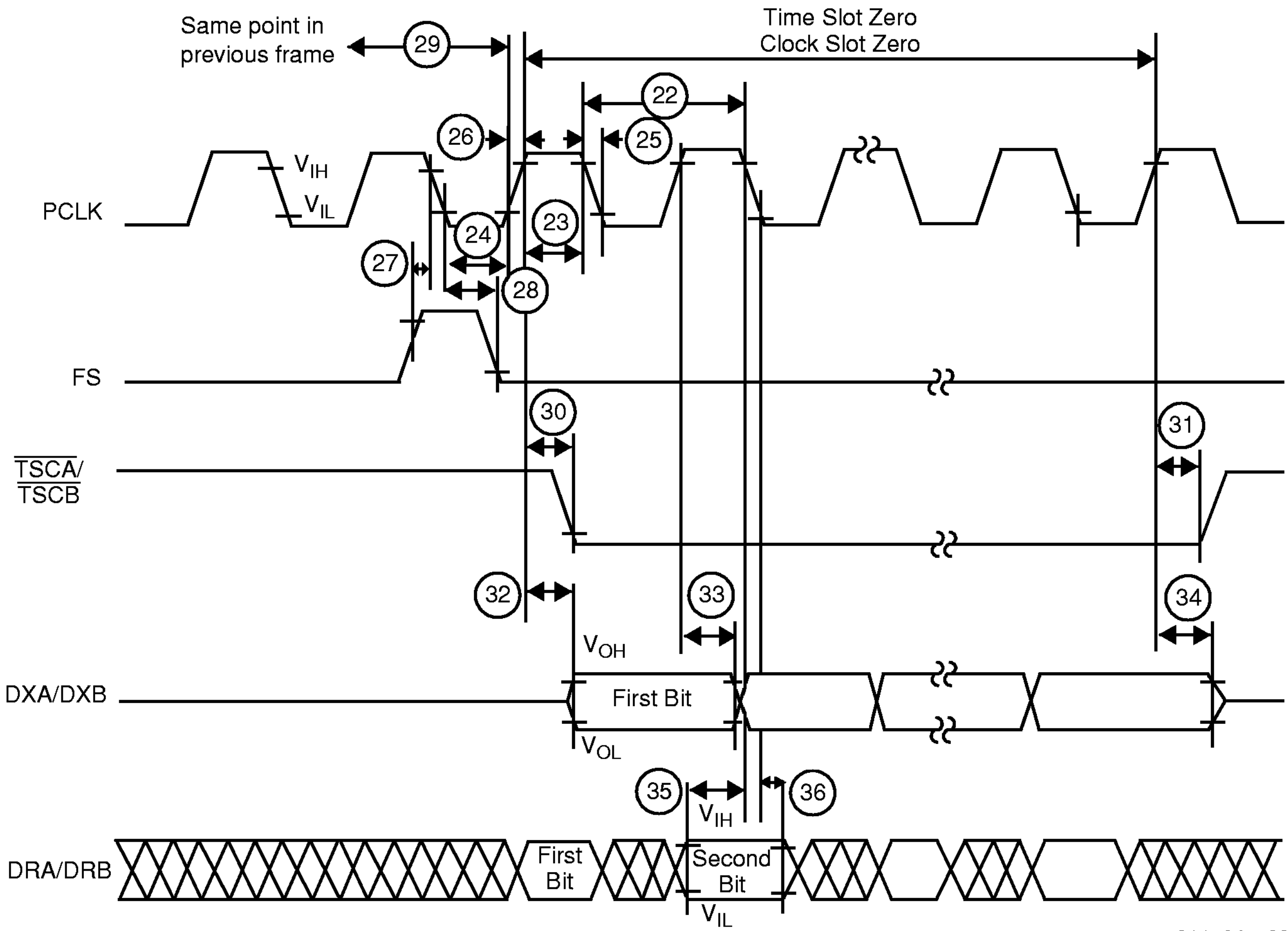
21108A-020

PCM Highway Timing for XE = 0 (Transmit on Negative PCLK Edge)



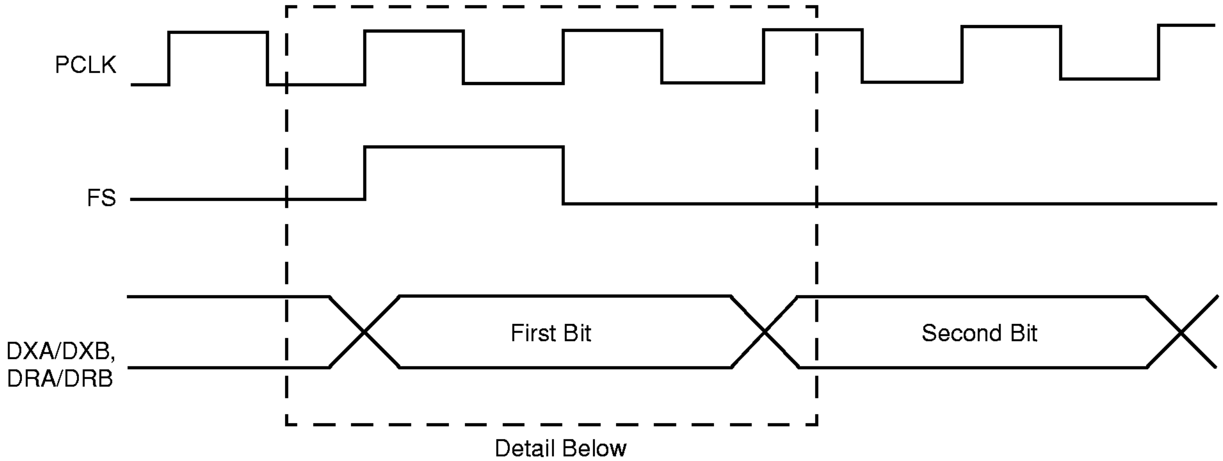
21108A-021

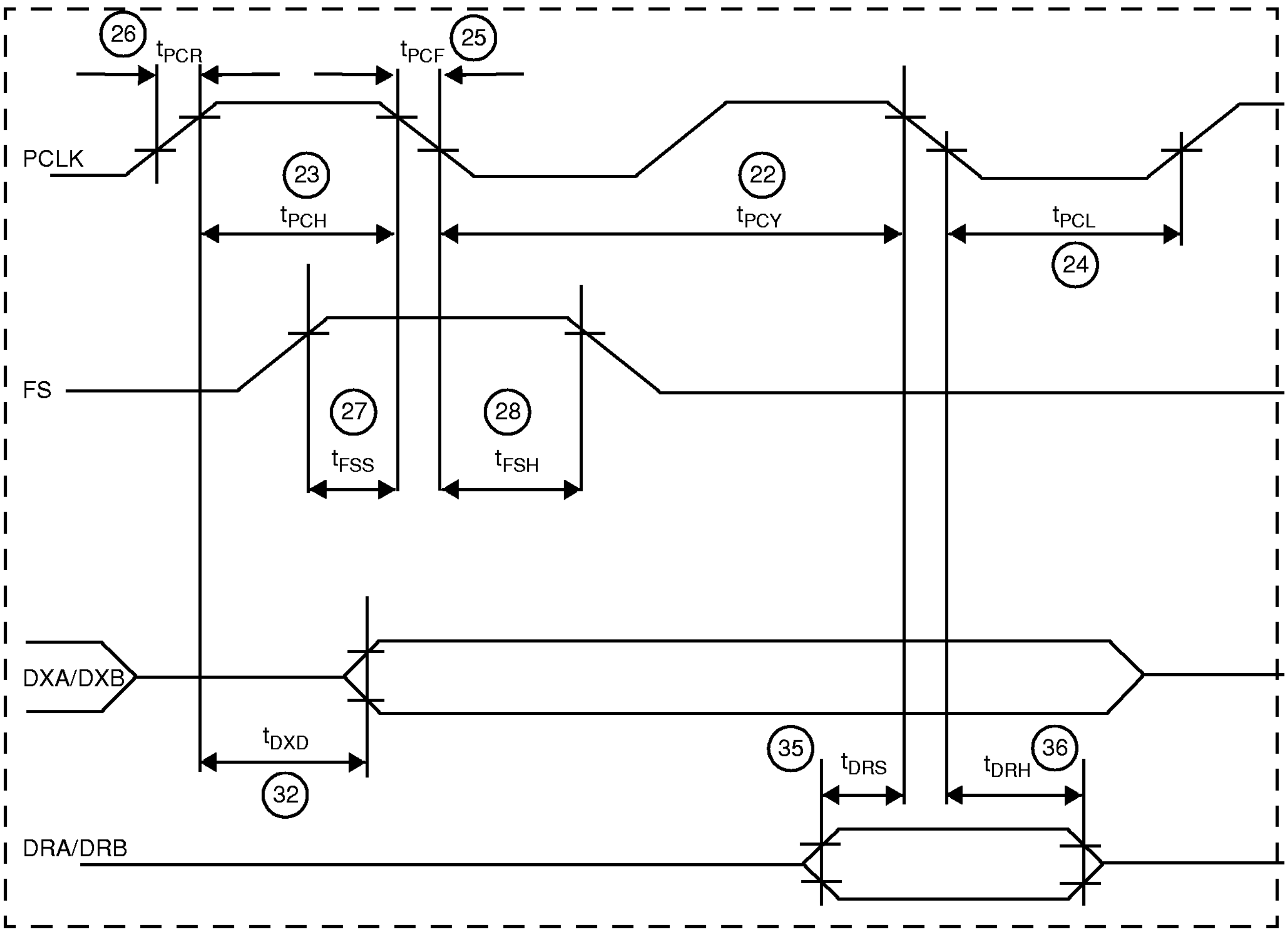
PCM Highway Timing for XE = 1 (Transmit on Positive PCLK Edge)



21108A-022

Double PCLK PCM Timing





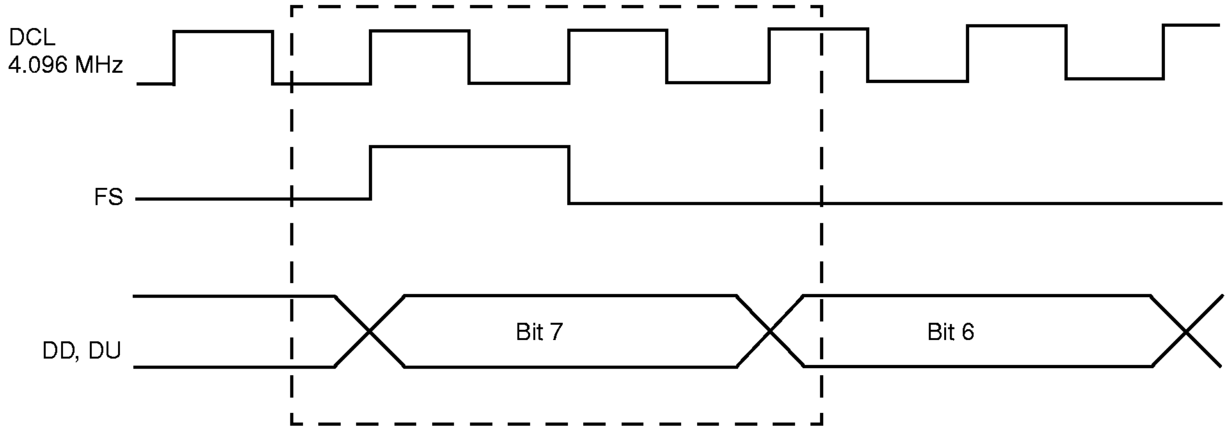
GCI Timing Specifications

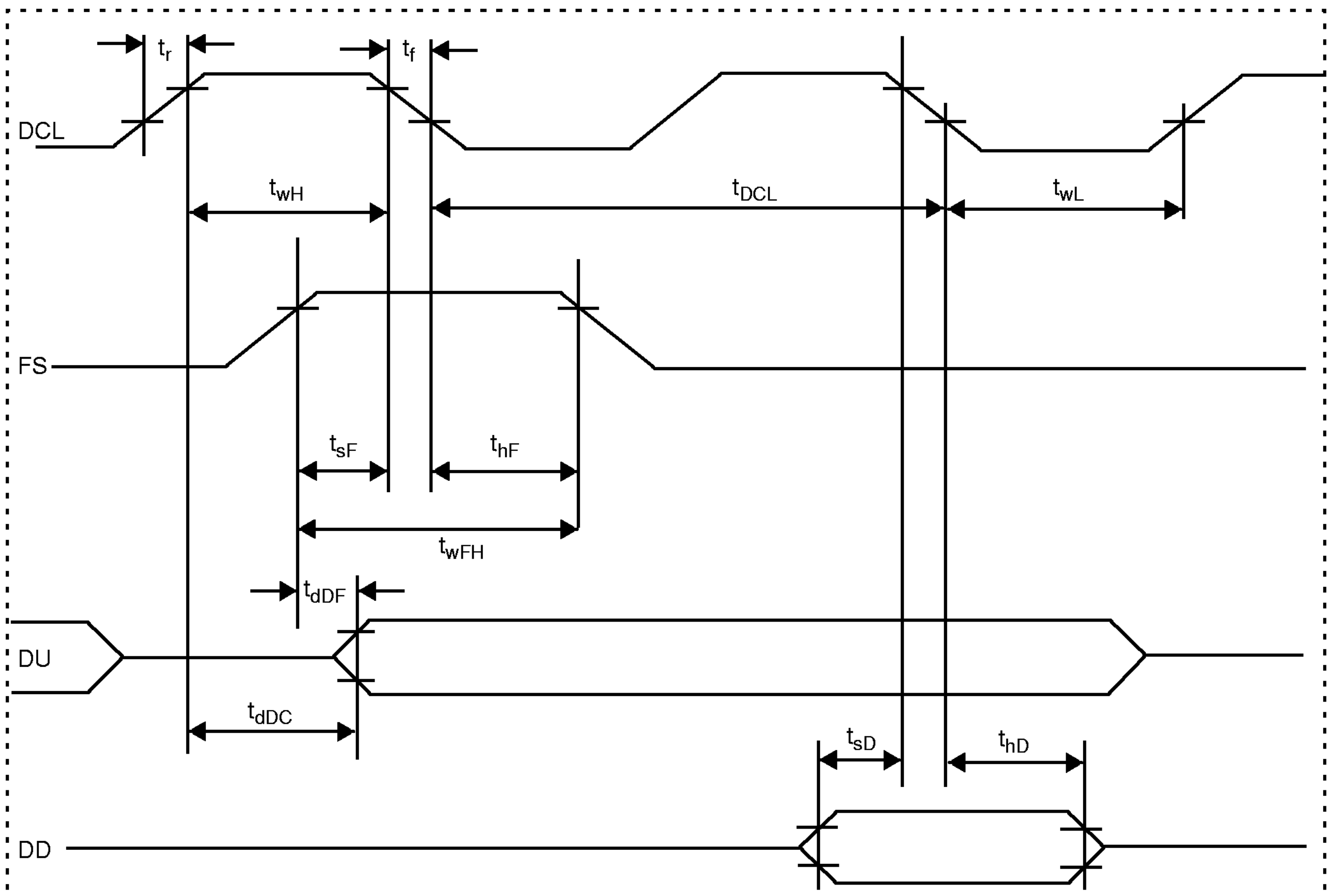
Symbol	Signal	Parameter	Min	Typ	Max	Units
t_r, t_f	DCL	Rise/fall time			60	ns
A_{DCL}	DCL	DCL accuracy F_{DCL} = 2.048 kHz F_{DCL} = 4.096 kHz	–100 –100		+100 +100	PPM
t_{DCL}	DCL	Period F_{DCL} = 2.048 kHz F_{DCL} = 4.096 kHz		488 244		ns
t_{wH}, t_{wL}	DCL	Pulse width	90			
t_r, t_f	FS	Rise/fall time			60	
t_{sF}	FS	Setup time	70		t_{DCL} – 50	
t_{hF}	FS	Hold time	50			
t_{wFH}	FS	High pulse width	130			
t_{dDC}	DU	Delay from DCL edge			100	
t_{dDF}	DU	Delay from FS edge			150	
t_{sD}	DD	Data setup	twH + 20			
t_{hD}	DD	Data hold	50			

Note:
The Data Clock (DCL) can be stopped in the high or low state without loss of information.

GCI Waveforms

4.096 MHz DCL Operation

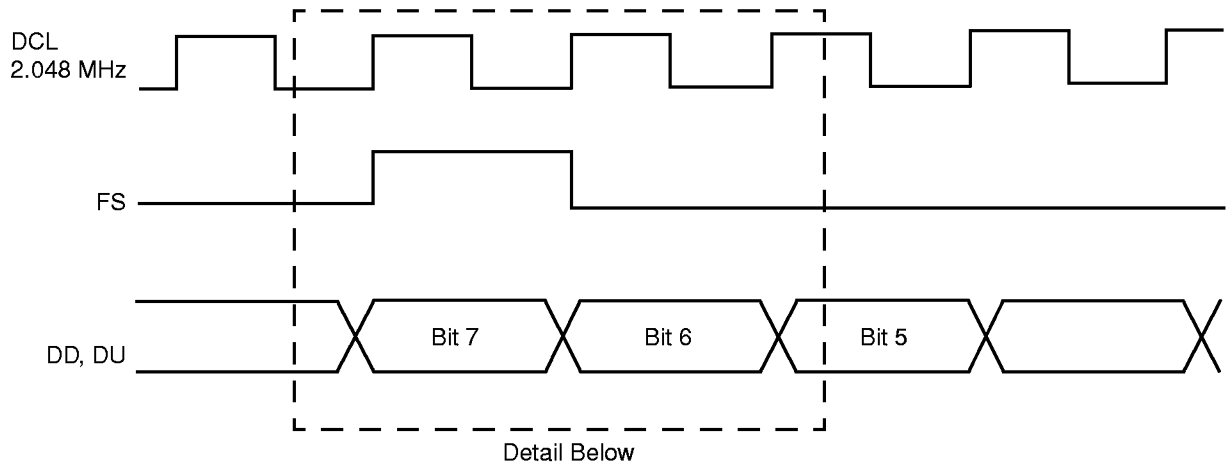


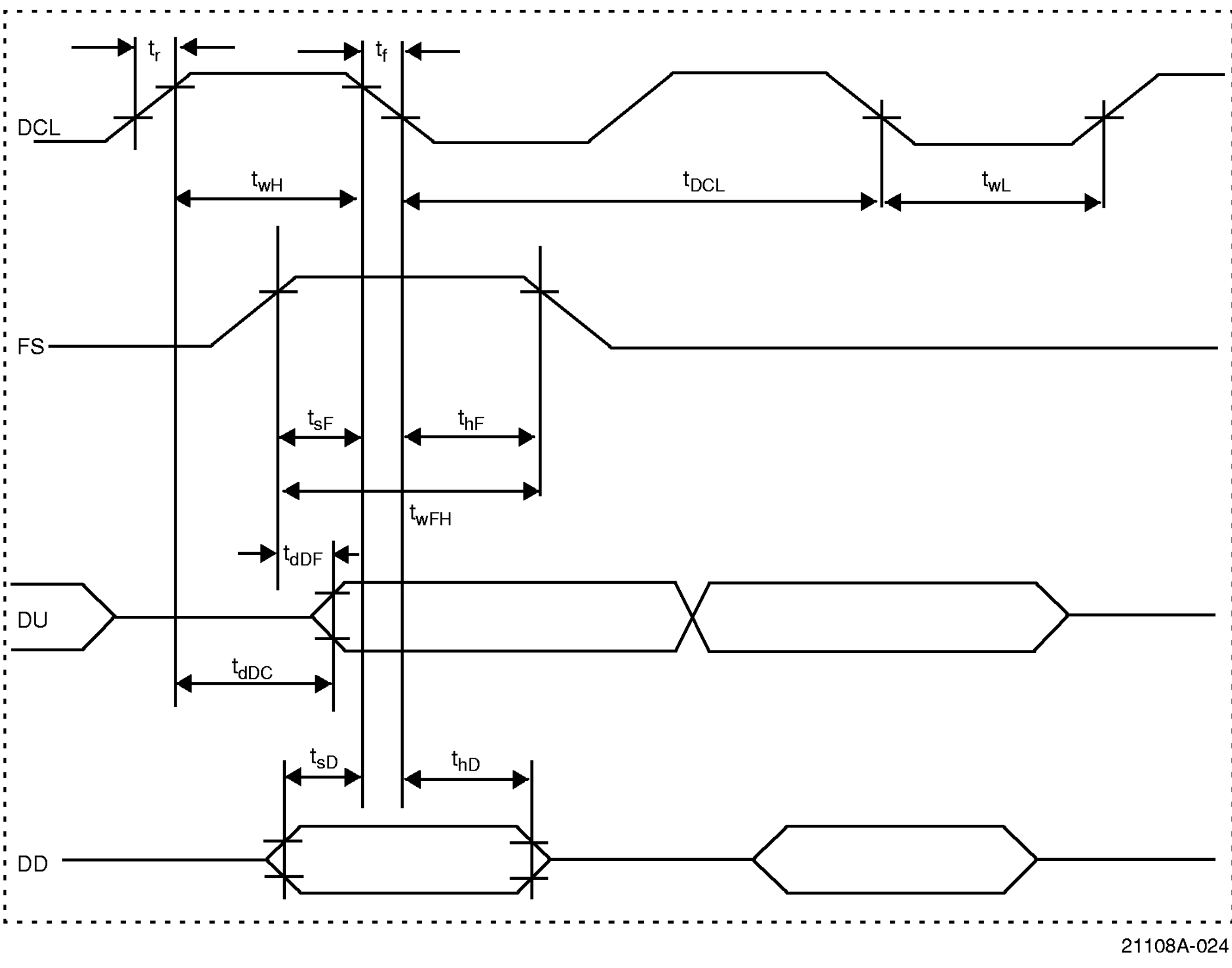


21108A-023

4.096 MHz DCL Operation

2.048 MHz DCL Operation





2.048 MHz DCL Operation

OPERATING THE QSLAC DEVICE

The following sections describe the operation of the four independent channels of the QSLAC device. The description is valid for Channel 1, 2, 3, or 4; consequently, the channel subscripts have been dropped. For example, VOUT refers to either $VOUT_1$, $VOUT_2$, $VOUT_3$, or $VOUT_4$.

Power-Up Sequence

The recommended QSLAC device power-up sequence is to apply:

1. Ground first
2. VCC, signal connections, and Low on $\overline{RST}$
3. High on $\overline{RST}$

The software initialization should then include:

1. Wait 1 ms.
2. For PCM/MPI mode, select master clock frequency and source (Commands 12 and 13). This should turn off the CFAIL bit (Command 23) within 400 µs. While the CFAIL bit is on, normal programming can proceed, but no channels should be activated.

   In GCI mode, DCL is the clock source. The CFAIL bit (GCI Command SOP 8) is set to 1 until the device has determined and synchronized to the DCL frequency, 4.096 MHz or 2.048 MHz. While the CFAIL bit is on, normal programming can proceed, but no channels should be activated. If channels are activated while CFAIL is a 1, no device damage will occur, but high audible noise may appear on the line. Also, CD1, CD2, C3, C4, and C5 bit may not be stable.
3. Program filter coefficients and other parameters as required.
4. Activate (MPI Command 5, GCI Command SOP 04).

If the power supply (VCCD) falls below approximately 1.0 V, the device is reset and requires complete reprogramming with the above sequence. A reset can be initiated by connection of a logic Low to the $\overline{RST}$ pin, or if chip select ($\overline{CS}$) is held low for 16 rising edges of DCLK, a hardware reset is generated when $\overline{CS}$ returns high. The $\overline{RST}$ pin can be tied to VCCD if it is not used in the system.

PCM and GCI State Selection

The Am79Q06/061/062/063 QSLAC device can switch between PCM/MPI and GCI states. Table 2 lists the selection requirements.

Table 2. PCM/GCI State Selection

From State	To State	Requirement
Power On or Hardware Reset	PCM	$\overline{CS}$ = 1 *or* DCLK has ac clock present
Power On or Hardware Reset	GCI	$\overline{CS}$ = 0 *and* DCLK does not have ac clock present
GCI	PCM	$\overline{CS}$ = 1 *or* DCLK has ac clock present
PCM	GCI	No commands yet sent in PCM state *and* $\overline{CS}$ = 0 (for more than 2 FS) *and* DCLK does not have ac clock present
PCM	Power On or Hardware Reset	Commands have been sent in PCM state *and* Hardware Reset generated
GCI	Power On or Hardware Reset	Not allowed

Channel Enable Register

In PCM/MPI mode, a channel enable register has been implemented in the QSLAC device in order to reduce the effort required to address individual or multiple channels of the QSLAC device. The register is written using MPI Command 14. Each bit of the register is assigned to one unique channel, bit 0 for Channel 1, bit 1 for Channel 2, bit 2 for Channel 3, and bit 3 for Channel 4. The channel or channels are enabled when their corresponding enable bits are High. All enabled channels receive the data written to the QSLAC device. This enables a Broadcast mode (all channels enabled) to be implemented simply and efficiently, and multiple channel addressing is accomplished without increasing the number of I/O pins on the device. The Broadcast mode can be further enhanced by providing the ability to select many chips at once; however, care should be taken not to enable more than one chip in the Read mode. This can lead to an internal bus contention, where excess power is dissipated. (Bus contention will not damage the device.) Most MPI commands defined for the DSLAC device are compatible with the QSLAC device, thereby minimizing the impact to existing system software.

In GCI mode, the individual channels are controlled by their respective Monitor and SC channels embedded in the GCI channels selected by the device (S0, S1).

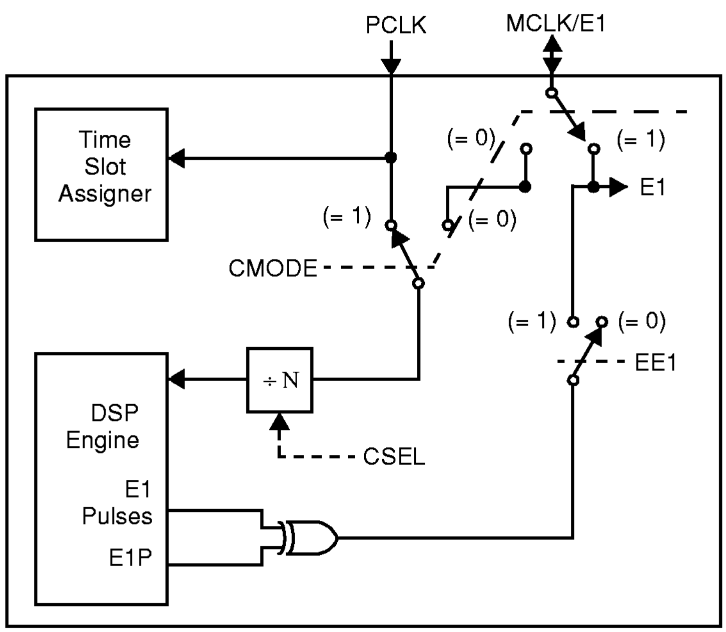
SLIC Control and Data Lines

The QSLAC device has up to five programmable Input/Output pins per channel (CD1–C5). Each of these pins can be programmed as either an input or an output using the I/O Direction Register (MPI Commands 22 and 23, GCI Command SOP 8). Also, the Am79Q063VC 64-pin package includes two additional output pins per channel, C6-C7 (see Figure 9). The output latches can be written with MPI Command 20 or through the CI1 to CI5 bits present in the downstream SC channel; however, only those bits programmed as outputs actually drive the pins. The inputs can be read with MPI Command 21, GCI Command SOP 10 or on the Upstream CI bits, in the SC channel. If a pin is programmed as an output, the data read from it is the contents of the output latch. In the GCI mode, this data can be read using SOP 10, but the output bits are not sent upstream in the SC channel.

Clock Mode Operation

The QSLAC device operates with multiple clock signals. The master clock (MCLK) is used for internal timing including operation of the digital signal processing. In PCM/MPI mode, the master clock may be derived from either the MCLK or PCLK source. In GCI mode, the master clock is obtained from the DCL clock only. The source for the master clock must be essentially jitter free, but it can be asynchronous to PCLK in the PCM/MPI mode. The allowed frequencies are listed under Commands 12 and 13 for PCM/MPI mode. In GCI mode, DCL can be only 2.048 MHz or 4.096 MHz.

In PCM/MPI mode, the PCM clock (PCLK) is used for PCM timing and is an integer multiple of the frame sync frequency. The internal device clock (MCLK) can be optionally derived from the PCLK source by setting the CMODE bit (bit 4, commands 12 and 13, 46/47h) to one. In this mode, the MCLK/E1 pin is free to be used as an E1 signal output. In GCI mode, since the master clock is derived only from the DCL clock, this MCLK/E1 pin is always available as an E1 output. Clock mode options and E1 output functions are shown in Figure 8.



Notes:

1. *CMODE = Command 12, 13 Bit 4*
2. *CSEL = Command 12, 13 Bits 0–3*
3. *EE1 = Command 45, 46 Bit 7*
4. *E1P = Command 45, 46 Bit 6*

Figure 8. Clock Mode Option (PCM/MPI Mode)

E1 Mulitplex Operation

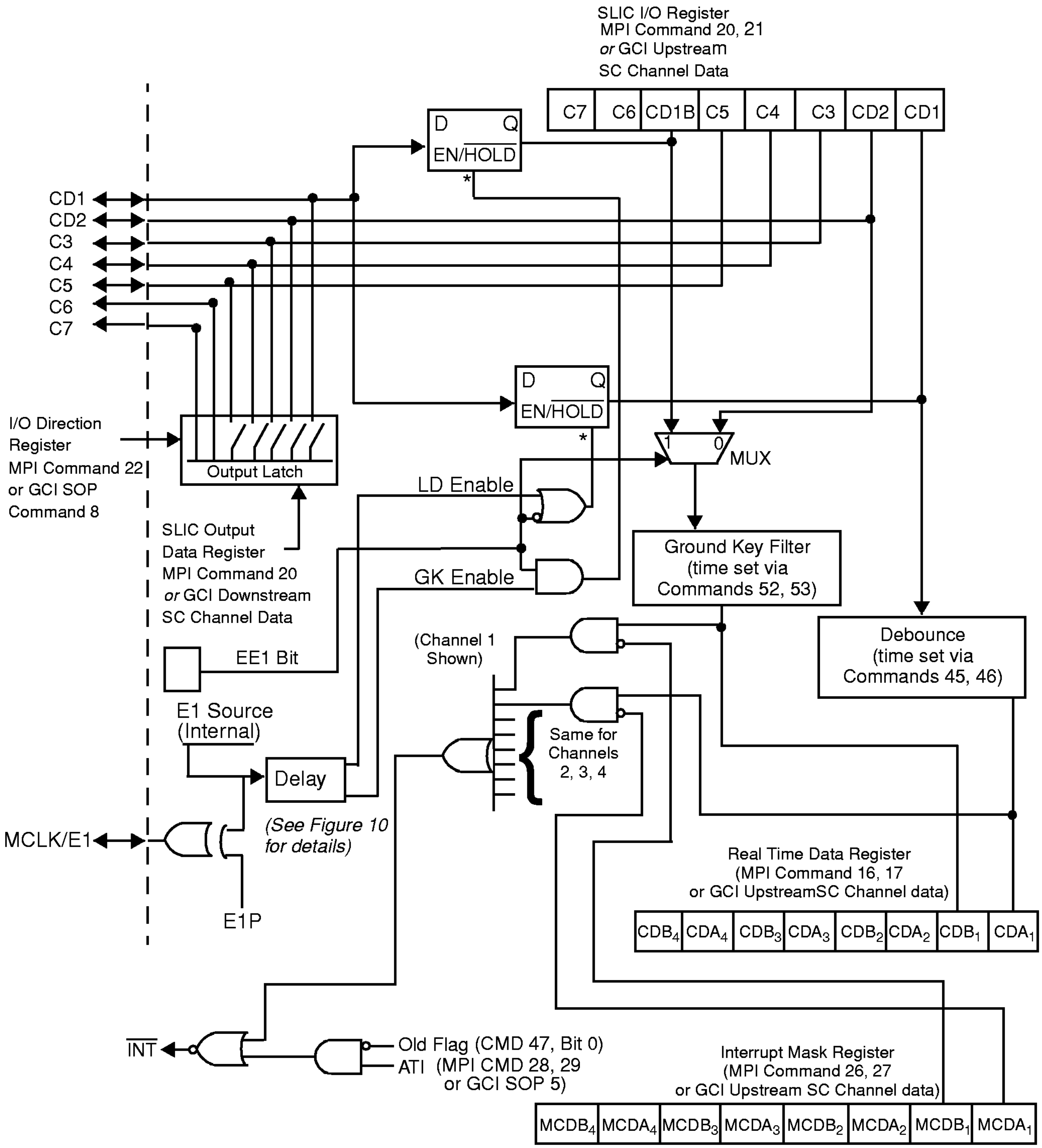
The QSLAC device can multiplex input data from the CD1 SLIC I/O pin into two separate status bits per channel (CD1 and CD1B bits in the SLIC Input/Output register, Commands 52/53h, and CDA and CDB bits in the Real Time Data register, Commands 4D/4Fh) using the E1 multiplex mode. This multiplex mode provides the means to accommodate dual detect states when connected to an AMD SLIC device, which also supports ground-key detection in addition to loop detect. AMD SLICs that support ground-key detect use their E1 pin as an input to switch the SLIC's single detector (DET) output between internal loop detect or ground-key detect comparators. Using the E1 multiplex mode, a single QSLAC device can monitor both loop detect and ground-key detect states of all four connected SLICs without additional hardware. Although normally used for ground key detect, this multiplex function can also be used for monitoring other signal states.

The E1 multiplex mode is selected by setting the EE1 bit (bit 7, Command C8/C9h) and CMODE bit (bit 4, Command 46/47h) in the QSLAC device. The CMODE bit must be selected (CMODE = 1) for the master clock to be derived from PCLK so that the MCLK/E1 pin can be used as an output for the E1 signal. The multiplex mode is then turned on by setting the EE1 bit. With the E1 multiplex mode enabled, the QSLAC device generates the E1 output signal. This signal is a 31.25 µs (1/32 kHz) duration pulse occurring at a 4.923 kHz (64 kHz/13) rate. The polarity of this E1 output is selected by the E1P bit (bit 6, Command C8/C9h) allowing this multiplex mode to accommodate all SLICs regardless of their E1 high/low logic definition.

Figure 9 shows the SLIC Input/Output register, I/O pins, E1 multiplex hardware operation for one QSLAC device channel. It also shows the operation of the Real Time Register. The QSLAC device E1 output signal connects directly to the E1 inputs of all four connected SLICs and is used by those SLICs to select an internal comparator to route to the SLIC's DET output. This E1 signal is also used internally by the QSLAC device for controlling the multiplex operation and timing.

The CD1 and CD1B bits of the SLIC Input/Output register are isolated from the CD1 pin by transparent latches. When the E1 pulse is off, the CD1 pin data is routed directly to the CD1 bit of the SLIC I/O register and changes to the CD1B bit of that register are disabled by its own latch. When E1 pulses on, the CD1 latch holds the last CD1 state in its register. At the same time, the CD1B latch is enabled, which allows CD1 pin data to be routed directly to the CD1B bit. Therefore, during this multiplexing, the CD1 bit always has loop-detect status and the CD1B bit always has ground-key detect status.

This multiplexing state changes almost instantaneously within the QSLAC device but the SLIC device may require a slightly longer time period to respond to this detect state change before its DET output settles and becomes valid. To accommodate this delay difference, the internal signals within the QSLAC device are isolated by 15.625 µs before allowing any change to the CD1 bit and CD1B bit latches. This operation is further described by the E1 multiplex timing diagram in Figure 10. In this timing diagram, the E1 signal represents the actual signal presented to the E1 output pin. The GK Enable pulse allows CD1 pin data to be routed through the CD1B latch. The LD Enable pulse allows CD1 pin data to be routed through the CD1 latch. The uncertain states of the SLIC's DET output, and the masked times where that DET data is ignored are shown in this timing diagram. Using this isolation of masked times, the CD1 and CD1B registers are guaranteed to contain accurate representations of the SLIC detector output.



Note:

** Transparent latches: When enable input is high, Q output follows D input. When enable input goes low, Q output is latched at last state.*

Figure 9. SLIC I/O, E1 Multiplex and Real-Time Data Register Operation

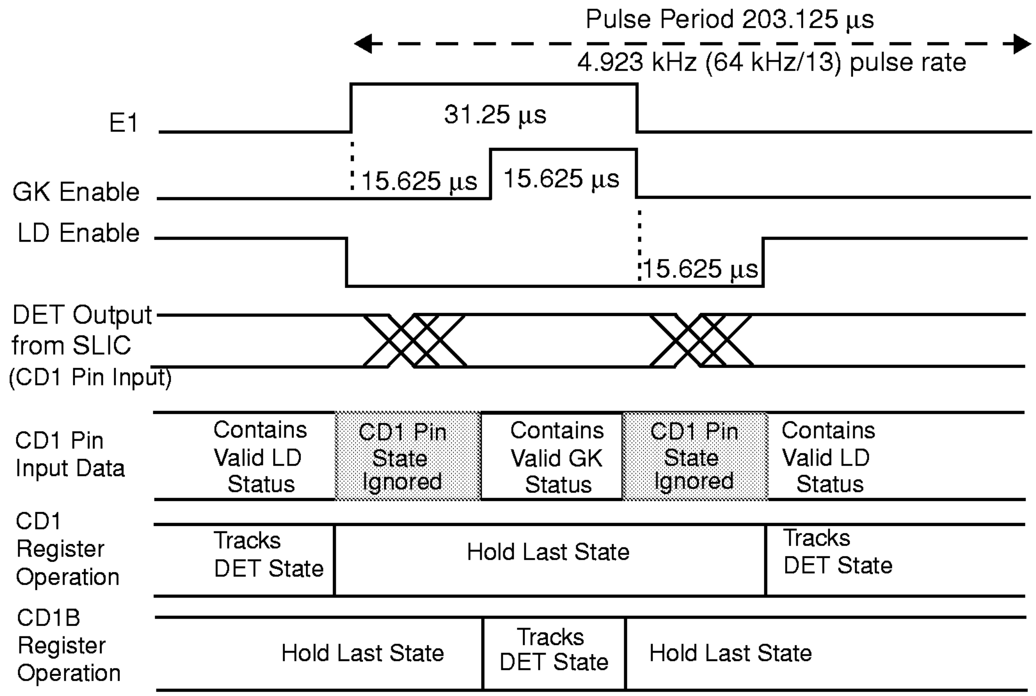


Figure 10. E1 Multiplex Internal Timing

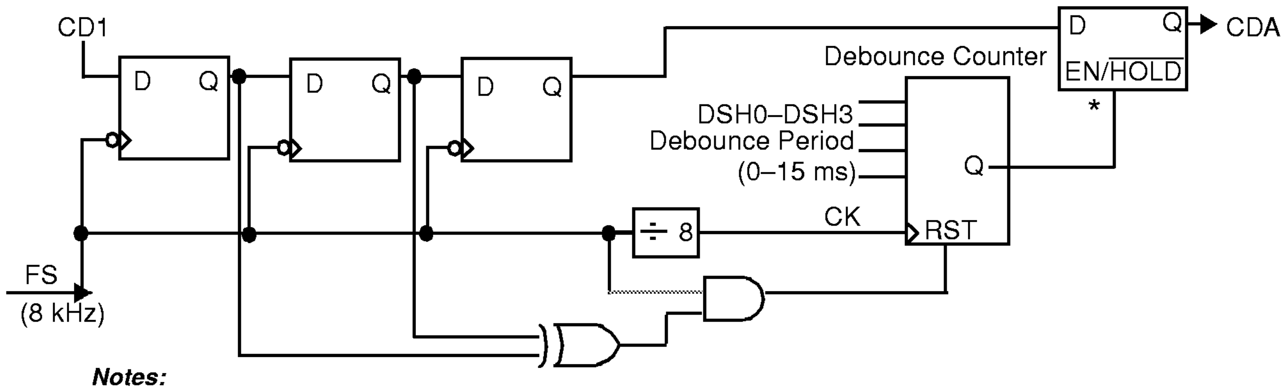
Debounce Filters Operation

Each channel has two debounce filter circuits to buffer the logic status of the CD1 and CD2/CD1B bits of the SLIC I/O Data Register (MPI Commands 20 and 21 and GCI Command SOP 10, 52/53h) before providing filtered bit outputs to the Real-Time Data Register (MPI Commands 16 and 17 or GCI Command SOP 13, 4D/4Fh). One filter is for the CD1 bit. The other filter either acts upon the CD1B bit if E1 multiplexing is enabled or on the CD2 bit if the multiplexing is not enabled.

The CD1 bit normally contains SLIC loop-detect status. The CD1 debouncing time is programmable with the Debounce Time Register (MPI Commands 45 and 46 or GCI Command SOP 11, C8/C9h), and even though each channel has its own filter, the programmed value is common to all four channels. This debounce filter is initially clocked at the frame sync rate of 125 µs, and any occurrence of changing data at this sample rate resets a programmable counter. This programmable counter is clocked at a 1 ms rate, and the programmed count value of 0–15 ms, as defined by the Debounce Time Register, must be reached before updating the CDA bit of the Real Time Data register with the CD1 state. Refer to Figure 11a for this filter's operation.

The ground-key filter (Figure 11b) provides a buffering of the signal, normally ground-key detect, which appears in the CDB bit of the Real-Time Data Register and the SC upstream channel in GCI mode. Each channel has its own filter, and each filter's time can be individually programmed. The input to the filter comes from either the CD2 bit of the SLIC I/O Data Register (52/53h), when E1 multiplexing is not enabled, or from the CD1B bit of that register when E1 multiplexing is enabled. The feature debounces ground-key signals before passing them to the Real Time Data Register, although signals other than ground-key status can be routed to the CD2 pin and then through the registers.

The ground-key debounce filter operates as a duty-cycle detector and consists of an up/down counter that ranges between 0 and 6. This six-state counter is clocked by the GK timer at the sampling period of 1–15 ms, as programmed by the value of the four GK bits (GK3, GK2, GK1, GK0) of the Ground-Key Filter Data register (Commands 52 and 53 and GCI Command SOP 12, E8/E9h). This sampling period clocks the counter, which buffers the CD2/CD1B bit's status before it is valid for presenting to the CDB bit of the Real Time Data Register. When the sampled value of the ground-key (or CD2) input is high, the counter is incremented by each clock pulse. When the sampled value is low, the counter is decremented. When the counter increments to 6, it sets a latch whose output is routed to the corresponding CDB bit. If the counter decrements to 0, this latch is cleared and the output bit is set to 0. All other times, the latch (and the CDB status) remains in its previous state without change. It therefore takes at least six consecutive GK clocks with the debounce input remaining at the same state to effect an output change. If the GK bit value is set to zero, the buffering is bypassed and the input status is passed directly to CDB.



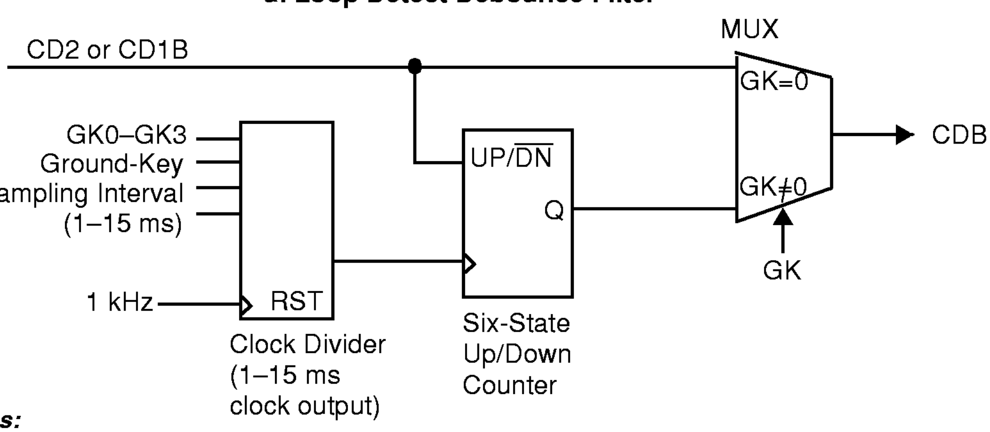
Notes:

** Transparent latch: Output follows input when EN is high; output holds last state when EN is low*

Debounce Counter: Output goes high after counting to programmed (DSH) number of 1 ms clocks; Counter is reset for CD1 input changes at 125 µs sample period.

DSH0–DSH3 programmed value is common for all 4 channels, but debounce counter is separate per channel

a. Loop Detect Debounce Filter



Notes:

Programmed value of GK0–GK3 determines clock rate (1–15 ms) of six-state counter.

If GK value = 0, counter is bypassed and no buffering occurs.

Six-state up/down counter: Counts up when input is high; counts down when input is low. Output goes and stays high when maximum count is reached; output goes and stays low when counts down to zero.

b. Ground-Key Filter

Figure 11. MPI Real-Time Data Register or GCI Upstream SC Channel Data

Real-Time Data Register Operation

To obtain time-critical data such as off/on-hook and ring trip information from the SLIC with a minimum of processor time and effort, the QSLAC device contains an 8-bit Real Time Data register. This register contains CDA and CDB bits from all four channels. The CDA bit for each channel is a debounced version of the CD1 input. The CDA bit is normally used for switchhook. The CDB bit for each channel normally contains the CD2 input bit; however, if the E1 multiplex operation is enabled, the CDB bit will contain the debounced value of the CD1B bit. CD1 and CD2 can be assigned to off-hook, ring trip, ground key signals, or other signals. Frame sync is needed for the debounce and the ground-key signals. If Frame sync is not provided, the real-time register will not work. The register is read using MPI Commands 16 and 17 or GCI Command SOP 13 (4D/4Fh), and may be read at any time regardless of the state of the Channel Enable Register. This allows off/on-hook, ring trip, or ground key information for all four channels to be obtained from the QSLAC device with one read operation versus one read per channel. If these data bits are not used for supervision information, they can be accessed on an individual channel basis in the same way as C3–C5; however, CD1 and CD1B will not be debounced. This Real-Time Data register is available in both MPI and GCI modes. In the GCI mode, this real-time data is also available in the field of the upstream SC octet.

Interrupt

In addition to the Real Time Data register, an interrupt signal is provided by the QSLAC device. The Interrupt signal is an active Low output signal that pulls Low any time any of the unmasked CD bits changes state (Low to High or High to Low); or any time the transmit PCM data changes on a channel where the Arm Transmit Interrupt (ATI) bit is on. The interrupt control is shown in Figure 9. The interrupt remains Low until the appropriate register is read. This output can be programmed as a TTL or open drain output by the INTM bit, MPI Command 12 or GCI Command SOP 6. When an interrupt is generated, all of the unmasked bits in the Real Time Data register are latched and remain latched until the interrupt is cleared. The interrupt is cleared by reading the register with MPI Command 17 or GCI Command SOP 13, by writing to the interrupt mask register (MPI Command 26 or GCI Command SOP 14), or by a reset. If any of the inputs to the unmasked bits in the Real Time Data register are different from the register bits at the time that the interrupt is cleared, a new interrupt is immediately generated with the new data latched into the Real Time Data register. For this reason, the interrupt logic in the controller should be level sensitive rather than edge sensitive.

Interrupt Mask Register

The Real Time Data register data bits can be masked from causing an interrupt to the processor using the interrupt mask register. The contents of the mask register can be written or read via the MPI Commands 26 and 27 or GCI Command SOP 14.

Active State

Each channel of the QSLAC device can operate in either the Active (operational) or Inactive (standby) mode. In the Active mode, individual channels of the QSLAC device can transmit and receive PCM or linear data and analog information. The Active mode is required when a telephone call is in progress. The Activate command, MPI Command 5, GCI Command SOP 4, puts the selected channels (see channel enable register for PCM/MPI Mode) into this state. Bringing a channel of the QSLAC device into the Active mode is only possible through the MPI command or the GCI Command.

Inactive State

All channels of the QSLAC device are forced into the Inactive mode by a power-up or hardware reset. Individual channels can be programmed into this mode by the deactivate command (MPI Command 1, GCI Command SOP 1) or by the software reset command (MPI Command 2, GCI Command 2). Power is disconnected from all nonessential circuitry, while the MPI remains active to receive commands. The analog output is tied to VREF through a resistor whose value depends on the VMODE bit. All circuits that contain programmed information retain their data in the Inactive mode.

Low Power State

If all four channels are deactivated and Low Power mode is selected, the internal clock speed of the part will be reduced to 1/6 of its normal speed. When this happens, the CFAIL bit is set to 1, and the microprocessor interface works at 1/6 its normal speed. That is, the CS must be high six times as long between MPI commands.

Chopper Clock

The Am79Q06 and Am79Q063 devices provide a chopper clock output to drive the switching regulator on some AMD SLICs. The clock frequency is selectable as 256 or 292.57 kHz by the CHP bit (MPI Command 12/GCI Command SOP 6). The chopper output must be turned on with the ECH bit (MPI Command 45, GCI Command SOP 11).

Reset States

The QSLAC device can be reset by application of power, by an active Low on the hardware Reset pin ($\overline{RST}$), by a hardware reset command, or by $\overline{CS}$ Low for 16 or more rising edges of DCLK.

1. A-law companding is selected.
2. Default filter values B, X, R, and Z are selected and the AISN is set to zero.
3. Default digital gain blocks, GX and GR, are selected. The analog gains, AX and AR, are set to 0 dB.
4. SLIC input/outputs CD1, CD2, C3, C4, and C5 are set to the Input mode.
5. All of the test modes in the Operating Conditions Register are turned off (0s).
6. All four channels are placed in the Inactive (standby) mode.
7. For PCM/MPI mode, transmit time slots and receive time slots are set to 0, 1, 2, and 3 for Channels 1, 2, 3, and 4, respectively. The clock slots are set to 0, with transmit on the negative edge. For GCI mode, operation is determined by S0 and S1.
8. DXA/DU port is selected for all channels.
9. DRA/DD port is selected for all channels.
10. The master clock frequency in PCM/MPI mode is selected to be 8.192 MHz and is programmed to come from PCLK. In GCI mode, DCL is 2.048 or 4.096 MHz and is determined by the QSLAC device.
11. All four channels are selected in the Channel Enable Register for PCM/MPI mode.
12. Any pending interrupts are cleared, all interrupts are masked, and the Interrupt Output mode is set to open drain.
13. The supervision debounce time is set to 8 ms.
14. The previously programmed B, Z, X, R, GX, and GR filters are unchanged.
15. The chopper clock frequency is set to 256 kHz, but the chopper clock is turned off.
16. The E1 Multiplex mode is turned off and the polarity is set for high going pulses.
17. No signaling on the PCM highway (PCM/MPI mode).

SIGNAL PROCESSING

Overview of Digital Filters

Several of the blocks in the signal processing section are user-programmable. These allow the user to optimize the performance of the QSLAC device for the system. Figure 12 shows the QSLAC device signal processing and indicates the programmable blocks.

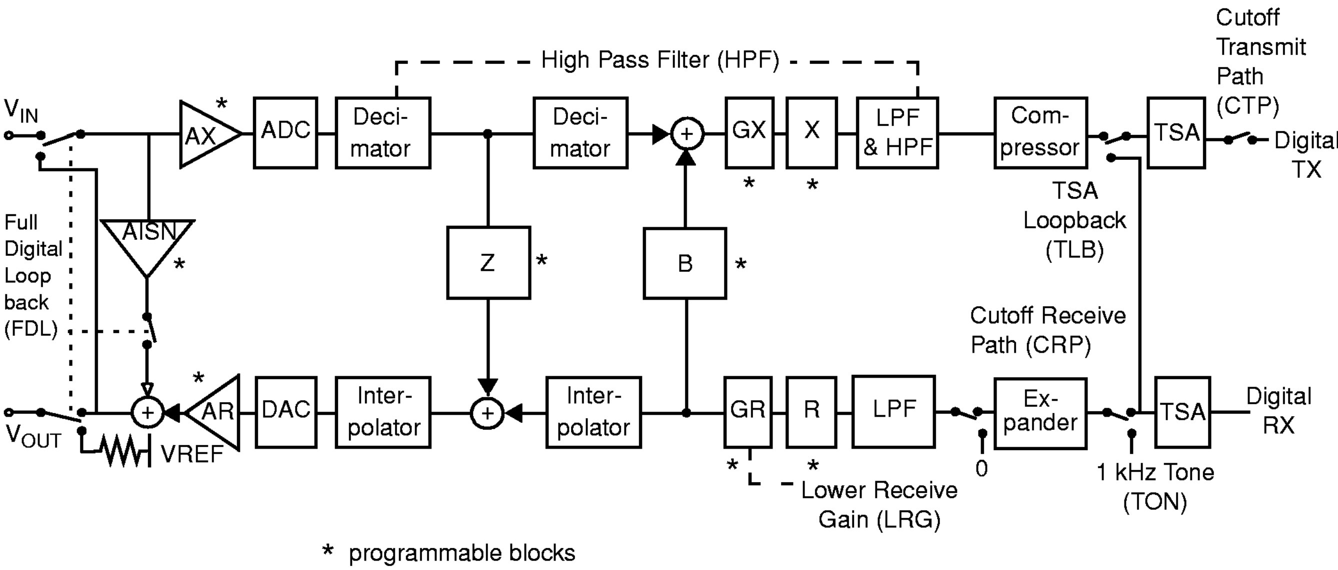


Figure 12. QSLAC Device Block Diagram

The advantages of digital filters are

- High reliability
- No drift with time or temperature
- Unit-to-unit repeatability
- Superior transmission performance
- Flexibility
- Maximum possible bandwidth for V.34 modems.

Two-Wire Impedance Matching

Two feedback paths on the QSLAC device synthesize the two-wire input impedance of the SLIC by providing a programmable feedback path from VIN to VOUT. The Analog Impedance Scaling Network (AISN) is a programmable analog gain of –0.9375 to +0.9375 from VIN to VOUT. The Z filter is a programmable digital filter providing an additional path and programming flexibility over the AISN in modifying the transfer function from VIN to VOUT. Together, the AISN and the Z-filter enable the user to synthesize virtually all required SLIC input impedances.

Frequency Response Correction and Equalization

The QSLAC device contains programmable filters in the receive (R) and transmit (X) directions that can be programmed for line equalization and to correct any attenuation distortion caused by the Z filter.

Transhybrid Balancing

The QSLAC device's programmable B filter is used to adjust transhybrid balance. The filter has a single pole IIR section (BIIR) and an eight-tap FIR section (BFIR), both operating at 16 kHz.

Gain Adjustment

The QSLAC device's transmit path has two programmable gain blocks. Gain block AX is an analog gain of 0 dB or 6.02 dB (unity gain or gain of 2.0), located immediately before the A/D converter. GX is a digital gain block that is programmable from 0 dB to +12 dB, with a worst-case step size of 0.1 dB for gain settings below +10 dB, and a worst-case step size of 0.3 dB for gain settings above +10 dB. The filters provide a net gain in the range of 0 dB to 18 dB.

The QSLAC device receive path has two programmable loss blocks. GR is a digital loss block that is programmable from 0 dB to 12 dB, with a worst-case step size of 0.1 dB (unity gain or gain of 0.5). Loss block AR is an analog loss of 0 dB or 6.02 dB, located immediately after the D/A converter. This provides a net loss in the range of 0 dB to 18 dB.

An additional 6 dB attenuation is provided as part of GR, which can be inserted by setting the RG bit of Command 70/71h. This allows writing of a single bit to introduce 6 dB of attenuation into the receive path without having to reprogram GR. This 6 dB loss is implemented as part of GR and the total receive path attenuation must remain in the specified 0 to –12 dB range. If the RG bit is set, the programmed value of GR must not introduce more than an additional 6 dB attenuation.

Transmit Signal Processing

In the transmit path (A/D), the analog input signal (VIN) is A/D converted, filtered, companded (for A-law or µ-law), and made available to the PCM highway or General Circuit Interface (GCI). Linear mode is only available in the PCM/MPI mode. If linear form is selected, the 16-bit data is transmitted in two consecutive time slots starting at the programmed time slot. The signal processor contains an ALU, RAM, ROM, and control logic to implement the filter sections. The B, X, and GX blocks are user-programmable digital filter sections with coefficients stored in the coefficient RAM, while AX is an analog amplifier that can be programmed for 0 dB or 6.02 dB gain. The B, X, and GX filters can also be operated from an alternate set of default coefficients stored in ROM (MPI Command 24/25, GCI Command SOP 7).

The decimator reduces the high input sampling rate to 16 kHz for input to the B, GX, and X filters. The X filter is a six-tap FIR section that is part of the frequency response correction network. The B filter operates on samples from the receive signal path to provide transhybrid balancing in the loop. The high-pass filter rejects low frequencies such as 50 Hz or 60 Hz, and can be disabled.

Transmit PCM Interface (PCM/MPI Mode)

In PCM/MPI mode, the transmit PCM interface transmits a 16-bit linear code (when programmed) or an 8-bit compressed code from the digital A-law or µ-law compressor. Transmit logic controls the transmission of data onto the PCM highway through output port selection and time/clock slot control circuitry. The linear data requires two consecutive time slots, while a single time slot is required for A-law or µ-law data.

In the PCM Signaling mode (SMODE = 1), the transmit time slot following the A-law or µ-law data is used for signaling information. The two time slots form a single 16-bit data block.

The frame sync (FS) pulse identifies time slot 0 of the transmit frame and all channels (time slots) are referenced to it. The logic contains user-programmable Transmit Time Slot and Transmit Clock Slot registers.

The Time Slot register is 7 bits wide and allows up to 128 8-bit channels (using a PCLK of 8.192 MHz) in each frame. This feature allows any clock frequency between 128 kHz and 8.192 MHz (2 to 128 channels) in a system. The data is transmitted in bytes, with the most significant bit first.

The Clock Slot register is 3 bits wide and may be programmed to offset the time slot assignment by 0 to 7 PCLK periods to eliminate any clock skew in the system. An exception occurs when division of the PCLK frequency by 64 kHz produces a nonzero remainder, R, and when the transmit clock slot is greater than R. In that case, the R-bit fractional time slot after the last full time slot in the frame will contain random information and will have the TSC output turned on. For example, if the PCLK frequency is 1.544 MHz (R = 1) and the transmit clock slot is greater than 1, the 1-bit fractional time slot after the last full time slot in the frame contains random information, and the TSC output remains active during the fractional time slot. In such cases, problems can be avoided by simply not using the last time slot.

The PCM data can be user programmed for output onto either the DXA or DXB port or both ports simultaneously. Correspondingly, either $\overline{\text{TSCA}}$ or $\overline{\text{TSCB}}$ or both are Low during transmission.

The DXA/DXB and $\overline{\text{TSCA}}$/$\overline{\text{TSCB}}$ outputs can be programmed to change either on the negative or positive edge of PCLK.

Transmit data can also be read through the microprocessor interface using Command 47.

Data Upstream Interface (GCI Mode)

In the GCI mode, the Data Upstream (DU) interface transmits a total of 4 bytes per GCI channel. Two bytes are from the A-law or µ-law compressor, one for voice channel 1, one for voice channel 2, a single Monitor channel byte, and a single SC channel byte. Transmit logic controls the transmission of data onto the GCI bus as determined by the frame synchronization signal (FSC) and the S0 and S1 channel select bits. No signaling or Linear mode options are available when GCI mode is selected.

The frame synchronization signal (FSC) identifies GCI channel 0 and all GCI channels are referenced to it.

Upstream Data is always transmitted at a 2.048 MHz data rate.

Receive Signal Processing

In the receive path (D/A), the digital signal is expanded (for A-law or µ-law), filtered, converted to analog, and passed to the VOUT pin. The signal processor contains an ALU, RAM, ROM, and Control logic to implement the filter sections. The Z, R, and GR blocks are user-programmable filter sections with their coefficients stored in the coefficient RAM, while AR is an analog amplifier that can be programmed for a 0 dB or 6.02 dB loss. The Z, R, and GR filters can also be operated from an alternate set of default coefficients stored in ROM (MPI Commands 24 and 25, GCI Command SOP 7).

The low-pass filter band limits the signal. The R filter is composed of a six-tap FIR section operating at a 16 kHz sampling rate and a one-tap IIR section operating at 8 kHz. It is part of the frequency response correction network. The Analog Impedance Scaling Network (AISN) is a user-programmable gain block providing feedback from VIN to VOUT to emulate different SLIC input impedances from a single external SLIC impedance. The Z filter provides feedback from the transmit signal path to the receive path and is used to modify the effective input impedance to the system. The interpolator increases the sampling rate prior to D/A conversion.

Receive PCM Interface (PCM/MPI Mode)

The receive PCM interface logic controls the reception of data bytes from the PCM highway, transfers the data to the A-law or µ-law expansion logic for compressed signals, and then passes the data to the receive path of the signal processor. If the data received from the PCM highway is programmed for linear code, the A-law or µ-law expansion logic is bypassed and the data is presented to the receive path of the signal processor directly. The linear data requires two consecutive time slots, while the A-law or µ-law data requires a single time slot.

The frame sync (FS) pulse identifies time slot 0 of the receive frame, and all channels (time slots) are referenced to it. The logic contains user-programmable Receive Time Slot and Receive Clock Slot registers. The Time Slot register is 7 bits wide and allows up to 128 8-bit channels (using a PCLK of 8.192 MHz) in each frame. This feature allows any clock frequency between 128 kHz and 8.192 MHz (2 to 128 channels) in a system.

The Clock Slot register is 3 bits wide and can be programmed to offset the time slot assignment by 0 to 7 PCLK periods to eliminate any clock skews in the system. An exception occurs when division of the PCLK frequency by 64 kHz produces a nonzero remainder, R, and when the receive clock slot is greater than R. In this case, the last full receive time slot in the frame is not usable. For example, if the PCLK frequency is 1.544 MHz (R = 1), the receive clock slot can be only 0 or 1 if the last time slot is to be used. The PCM data can be user-programmed for input from either the DRA or DRB port.

Data Downstream Interface (GCI Mode)

The Data Downstream (DD) interface logic controls the reception of data bytes from the GCI highway. The GCI channels received by the QSLAC device is determined by the logic levels on S0 and S1, the GCI channel select bits. The two compressed voice channel data bytes of the GCI channel are transferred to the A-law or µ-law expansion logic. The expanded data is passed to the receive path of the signal processor. The Monitor channel and SC channel bytes are transferred to the GCI control logic for processing.

The frame synchronization signal (FSC) identifies GCI channel 0 of the GCI frame, and all other GCI channels are referenced to it.

Downstream Data is always received at a 2.048 MHz data rate.

Analog Impedance Scaling Network (AISN)

The AISN is incorporated in the QSLAC device to scale the value of the external SLIC impedance. Scaling this external impedance with the AISN (along with the Z filter) allows matching of many different line conditions using a single impedance value. Linecards can meet many different specifications without any hardware changes.

The AISN is a programmable transfer function connected from VIN to VOUT of each QSLAC device channel. The AISN transfer function is used to alter the input impedance of the SLIC device to a new value (ZIN) given by:

$$ZIN = ZSL \bullet (1 - G44 \bullet h_{AISN}) / (1 - G440 \bullet h_{AISN})$$

where G440 is the SLIC echo gain into an open circuit, G44 is the SLIC echo gain into a short circuit, and ZSL is the SLIC input impedance without the QSLAC device.

The gain can be varied from –0.9375 to +0.9375 in 31 steps of 0.0625. The AISN gain is determined by the following equation:

$$h_{AISN} = 0.0625\left[\left(\sum_{i=0}^{4} AISNi \bullet 2^{i}\right) - 16\right]$$

where AISN = 0 or 1

There are two special cases to the formula for h_{AISN}: 1) a value of AISN = 00000 specifies a gain of 0 (or cutoff), and 2) a value of AISN = 10000 is a special case where the AISN circuitry is disabled and VOUT is connected internally to VIN with a gain of 0 dB. This allows a Full Digital Loopback mode where an input digital PCM signal is completely processed through the receive section, looped back, processed through the transmit section, and output as digital PCM data. During this test, the VIN input is ignored and the VOUT output is connected to VREF.

Speech Coding

The A/D and D/A conversion follows either the A-law or the µ-law standard as defined in ITU-T Recommendation G.711. A-law or µ-law operation is programmed using MPI Commands 24/25 or GCI Command SOP 7. Alternate bit inversion is performed as part of the A-law coding. In PCM/MPI mode, the QSLAC device provides linear code as an option on both the transmit and receive sides of the device. Linear code is selected using MPI Commands 24 and 25. Two successive time slots are required for linear code operation. The linear code is a 16-bit two's-complement number that appears sign bit first on the PCM highway. Linear code occupies two time slots.

Double PCLK (DPCK) Operation (PCM/MPI Mode)

The Double PCLK Operation allows the PCM clock (PCLK) signal to be clocked at a rate of twice that of the PCM data. This mode provides compatibility of the QSLAC device with other existing system architectures, such as a GCI interface system in terminal mode operating at a 768 kHz data rate with a 1.536 MHz clock rate.

The operation is enabled by setting the DPCK bit of Command 45 and 46 (C8/C9h). When set to zero, operation is unchanged from normal PCM clocking and the PCM data and clock rates are the same. When the bit is set to 1, clocking of PCM data is divided by two and occurs at one half of the PCLK PCM clock rate. The internal PLL used for synchronization of the master DSP clock (MCLK) receives its input from either the MCLK or PCLK pin, depending on the clock mode (CMODE) selection. If PCLK is used for MCLK (CMODE = 1), then the clock input is routed to both the DSP clock input and to the time slot assigner. The timing division related to the double PCLK mode occurs only within the time slot assigner, and therefore, double PCLK operation is available with either CMODE setting. This allows the MCLK/E1 pin to be available for E1 multiplexing operation if both double PCLK and E1 multiplexing modes are simultaneously required.

Specifications for Double PCLK Operation are shown in *Switching Characteristics*.

Signaling on the PCM Highway (PCM/MPI Mode)

If the SMODE bit is set in the Configuration Register, each data point occupies two consecutive time slots. The first time slot contains A-law or µ-law data and the second time slot has the following information:

- Bit 7: Debounced CD1 bit (usually switchhook)
- Bit 6: CD2 bit or CD1B bit
- Bits 5–3: Reserved
- Bit 2: CFAIL
- Bits 1–0: Reserved

Bit 7 of the signaling byte appears immediately after bit 0 of the data byte. A-law or µ-law Companded mode must be specified in order to put signaling information on the PCM highway. The signaling time slot remains active, even when the channel is deactivated.

Robbed-Bit Signaling Compatibility (PCM/MPI Mode)

The QSLAC device supports robbed bit signaling compatibility. Robbed bit signaling allows periodic use of the least significant bit (LSB) of the receive path PCM data to be used to carry signaling information. In this scheme, separate circuitry within the line card or system intercepts this bit out of the PCM data stream and uses this bit to control signaling functions within the system. The QSLAC device does not perform any processing of any of the robbed bits during this operation; it simply allows for the robbed bit presence by performing the LSB substitution.

If the RBE bit is set, then the robbed-bit signaling compatibility mode is enabled. Robbed-bit signaling is only available in the µ-law companding mode of the device. Also, only the receive (digital-to-analog) path is involved. There is no change of operation to the transmit path and PCM data coming out of the QSLAC device will always contain complete PCM byte data for each time slot, regardless of robbed-bit signaling selection.

In the absence of actual PCM data for the affected time slots, there is an uncertainty of the legitimate value of this bit to accurately reconstruct the analog signal. This bit can always be assumed to be a 1 or 0; hence, the reconstructed signal is correct half the time. However, the other half of the time, there is an unacceptable reconstruction error of a significance equal to the value weighting of the LSB. To reduce this error and provide compatibility with the robbed bit signaling scheme, when in the robbed-bit signaling mode, the QSLAC device ignores the LSB of each received PCM byte and replace its value in the expander with a value of half the LSB's weight. This then guarantees the reconstruction is in error by only half this LSB weight. In the expander, the eight bits of the companded PCM byte are expanded into linear PCM data of several more bits within the internal signal processing path of the device. Therefore, accuracy is not limited to the weight of the LSB, and a weight of half this value is realizable.

When this robbed-bit mode is selected, not every frame contains bits for signaling, and therefore not every byte requires its LSB substituted with the half-LSB weight. This substitution only occurs for valid PCM time slots within frames for which this robbed bit has been designated. To determine which time slots are affected, the device monitors the frame sync (FS) pulse. The current frame is a robbed-bit frame and this half-LSB value is used only when this criteria is met:

- The RBE bit is set, *and*
- The device is in the µ-law companding mode, *and*
- The current frame sync pulse (FS) is two PCLK cycles long, *and*
- The previous frame sync pulse (FS) was *not* two PCLK cycles long.

The frame sync pulse is sampled on the falling edge of PCLK. As shown in Figure 13, if the above criteria is met, and if FS is high for two consecutive falling edges of PCLK then low for the third falling edge, it is considered a robbed-bit frame. Otherwise, it is a normal frame.

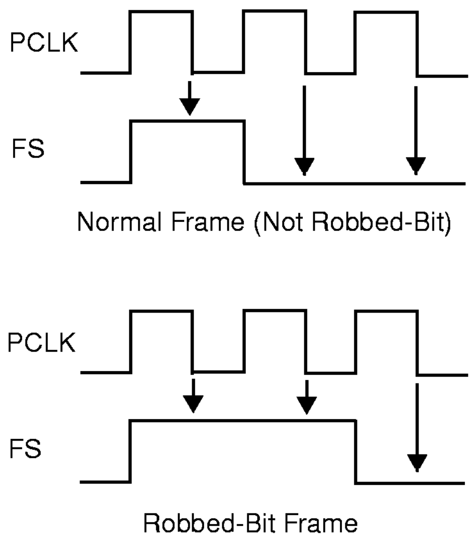


Figure 13. Robbed-Bit Frame

Default Filter Coefficients

The QSLAC device contains an internal set of default coefficients for the programmable filters. These coefficients were determined to allow reasonable system performance for initial power-up non-programmed situations, such as may exist before a system processor has opportunity to program any coefficients.

The default filter coefficients are calculated assuming an Am7920 SLIC with 50 Ω protection resistors, a 178 kΩ transversal impedance (ZT), and a 90.5 kΩ receive impedance (ZRX). This SLIC has a transmit gain of 0.5 (GTX) and a current gain of 500 (K1). The transmit relative level is set to +0.28 dBr, and the receive relative level is set to –4.39 dBr. The equalization filters (X and R) are not optimized. The balance filter was designed to give acceptable balance into a variety of impedances. The nominal input impedance was set to 815 Ω. If the SLIC circuit differs significantly from this design, the default filters cannot be used and must be replaced by programmed coefficients.

To obtain this above-system response, the default filter coefficients are set to produce these values:

GX gain = +6 dB, GR gain = –8.984 dB

AX gain = 0 dB, AR gain = 0 dB

R filter: H(z) = 1, X filter: H(z) = 1

Z filter: H(z) = 0, B filter H(z) = 0

AISN = cutoff

Notice that these default coefficient values are retained in a read-only memory area within the QSLAC device, and those values cannot be read back using any data commands. When the device is selected to use default coefficients, it obtains those values directly from the read-only memory area. The coefficient read operations access the programmable random access data memory only. If an attempt is made to read back any filter values without those values first being written with known programmed data, the values read back are totally random and do not represent the default or any other values.

COMMAND DESCRIPTION AND FORMATS

Microprocessor Interface Description

When PCM/MPI mode is selected via the $\overline{CS}$/PG and DCLK/S0 pins, a microprocessor can be used to program the QSLAC device and control its operation using the Microprocessor Interface (MPI). Data programmed previously can be read out for verification.

Commands are provided to assign values to the following channel parameters:

TTS	-	Transmit time slot
RTS	-	Receive time slot
TCS	-	Transmit clock slot
RCS	-	Receive clock slot
GX	-	Transmit gain
GR	-	Receive loss
B_1, B_2	-	B-filter coefficients
X	-	X-filter coefficients
R	-	R-filter coefficients
Z	-	Z-filter coefficients
AISN	-	AISN coefficient
CD1–C5	-	Read/Write SLIC Input/Output
IOD1–5	-	SLIC Input/Output Direction
A/µ, C/L	-	Select A-law, µ-law, or linear code
TPCM, TAB	-	Select Transmit PCM Port A or B or both
RPCM	-	Select Receive PCM Port A or B
EB	-	Programmed/Default B filter
EZ	-	Programmed/Default Z filter
EX	-	Programmed/Default X filter
ER	-	Programmed/Default R filter
EGX	-	Programmed/Default GX filter
EGR	-	Programmed/Default GR filter
AX	-	Enable/disable AX amplifier
AR	-	Enable/disable AR amplifier

TP - Cutoff Transmit Path
CRP - Cutoff Receive Path
HPF - Disable High Pass Filter
LRG - Lower Receive Gain
ATI - Arm Transmit Interrupt
ILB - Interface Loopback
FDL - Full Digital Loopback
$\overline{TON}$ - 1 kHz Tone On
$\overline{CS}$ - Select Active or Inactive (standby) mode

Commands are provided to read values from the following channel monitors:

SLIC status
XDAT - Transmit PCM data

Commands are provided to assign values to the following global chip parameters:

XE - Transmit PCM Clock Edge
RCS - Receive Clock Slot
TCS - Transmit Clock Slot
INTM - Interrupt Output Drive Mode
CHP - Chopper Clock Frequency
ECH - Enable Chopper Clock Output
SMODE - Select Signaling on the PCM Highway
CMODE - Select Master Clock Mode
CSEL - Select Master Clock Frequency
EC - Channel Enable Register
DSH - Debounce Time for CD1
EE1 - Enable E1 Output
E1P - E1 Polarity
MCDxy - Interrupt Mask Register

Commands are provided to read values from the following global chip status monitors:

CDxy - Real Time Data Register
PI - Power Interruption Bit
CFAIL - Clock Failure Bit
RCN - Revision Code Number

The following description of the MPI (Microprocessor Interface) is valid for Channel 1, 2, 3, or 4. If desired, multiple channels can be programmed simultaneously with identical information by setting multiple Channel Enable bits. Channel enables are contained in the Channel Enable Register and are written or read using Commands 14 and 15. If multiple Channel Enable bits are set for a read operation, only data from the first enabled channel is read.

The MPI physically consists of a serial data input/output (DIO), a data clock (DCLK), and a chip select ($\overline{CS}$). Individual Channel Enable bits EC1, EC2, EC3, and EC4 are stored internally in the Channel Enable Register of the QSLAC device. The serial input consists of 8-bit commands that can be followed with additional bytes of input data, or can be followed by the QSLAC device sending out bytes of data. All data input and output is MSB (D7) first and LSB (D0) last. All data bytes are read or written one at a time, with $\overline{CS}$ going High for at least a minimum off period before the next byte is read or written. Only a single channel should be enabled during read commands.

All commands that require additional input data to the device must have the input data as the next N words written into the device (for example, framed by the next N transitions of $\overline{CS}$). All unused bits should be programmed as 0 to ensure compatibility with future parts. All commands that are followed by output data will cause the device to output data for the next N transitions of $\overline{CS}$ going Low. The QSLAC device will not accept any commands until all the data has been shifted out. The output values of unused bits are not specified.

An MPI cycle is defined by transitions of $\overline{CS}$ and DCLK. If the $\overline{CS}$ lines are held in the High state between accesses, the DCLK runs continuously with no change to the internal control data. Using this method, the same DCLK can be run to a number of QSLAC devices and the individual $\overline{CS}$ lines will select the appropriate device to access. Between command sequences, DCLK can stay in the High state indefinitely with no loss of internal control information regardless of any transitions on the $\overline{CS}$ lines. Between bytes of a multibyte read or write command sequence, DCLK can also stay in the High state indefinitely. DCLK can stay in the Low state indefinitely with no loss of internal control information, provided the $\overline{CS}$ lines remain at a High level.

If a low period of $\overline{CS}$ contains less than 8 positive DCLK transitions, it is ignored. If it contains 8 to 15 positive transitions, only the last 8 transitions matter. If it contains 16 or more positive transitions, a hardware reset in the part occurs. If the chip is in the middle of a read sequence when $\overline{CS}$ goes Low, data will be present at the DIO pin even if DCLK has no activity. If $\overline{CS}$ is held low for two or more cycles of Frame Sync (FS) and DCLK is static (no toggling), then the QSLAC device switches to the General Circuit Interface mode of operation.

Summary of MPI Commands*

Number	Hex	Description
1	00	Deactivate (Standby Mode)
2	02	Software Reset
3	04	Hardware Reset
4	06	No Operation
5	0E	Activate (Operational Mode)
6,7	40/41	Write/Read Transmit Time Slot and PCM Highway Selection
8,9	42/43	Write/Read Receive Time Slot and PCM Highway Selection
10,11	44/45	Write/Read REC & TX Clock Slot and TX Edge
12,13	46/47	Write/Read Configuration Register
14,15	4A/4B	Write/Read Channel Enable & Operating Mode Register
16	4D	Read Real Time Data Register
17	4F	Read Real Time Data Register and Clear Interrupt
18,19	50/51	Write/Read AISN and Analog Gains
20,21	52/53	Write/Read SLIC Input/Output Register
22,23	54,55	Write/Read SLIC Input/Output Direction and Status Bits
24,25	60/61	Write/Read Operating Functions
26,27	6C/6D	Write/Read Interrupt Mask Register
28,29	70/71	Write/Read Operating Conditions
30	73	Read Revision Code Number (RCN)
31,32	80/81	Write/Read GX Filter Coefficients
33,34	82/83	Write/Read GR Filter Coefficients
35,36	84/85	Write/Read Z Filter Coefficients (FIR and IIR)
37, 38	86/87	Write/Read B1 Filter Coefficients (FIR)
39, 40	88/89	Write/Read X Filter Coefficients
41, 42	8A/8B	Write/Read R Filter Coefficients
43, 44	96/97	Write/Read B2 Filter Coefficients (IIR)
45, 46	C8/C9	Write/Read Debounce Time Register
47	CD	Read Transmit PCM Data
48, 49	98/99	Write/Read Z Filter Coefficients (FIR only)
50, 51	9A/9B	Write/Read Z Filter Coefficients (IIR only)
52,53	E8/E9h	Write/Read Ground Key Filter Sampling Interval

Note:
**All codes not listed are reserved by AMD and should not be used.*

MPI COMMAND STRUCTURE

This section details each MPI command. Each command is shown along with the format of any additional data bytes that follow. For details of the filter coefficients of the form $C_{xy}m_{xy}$, refer to the *Description of CSD Coefficients* section on page 85.

Unused bits are indicated by “RSVD”; 0’s should be written to them, but 0’s are not guaranteed when they are read.

*Default field values are marked by an asterisk. A hardware reset forces the default values.

1. Deactivate (Standby State) MPI Command

(00h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	0	0	0	0	0	0	0

In the Deactivated mode:

All programmed information is retained.

The Microprocessor Interface (MPI) remains active.

The PCM inputs are disabled and the PCM outputs are high impedance unless signaling on the PCM highway is programmed (SMODE = 1).

The analog output (VOUT) is disabled and biased at 2.1 V.

The channel status ($\overline{CS}$) bit in the SLIC I/O Direction and Channel Status Register is set to 0.

2. Software Reset MPI Command

(02h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	0	0	0	0	0	1	0

The action of this command is identical to that of the $\overline{RST}$ pin except that it only operates on the channels selected by the Channel Enable Register and it does not change clock slots, time slots, PCM highways, or global chip parameters. See the note under the hardware reset command that follows.

3. Hardware Reset MPI Command

(04h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	0	0	0	0	1	0	0

Hardware reset is equivalent to pulling the $\overline{RST}$ on the device Low. This command does not depend on the state of the Channel Enable Register.

Note: *The action of a hardware reset is described in* Reset States *on page 31 of the section* Operating the QSLAC Device*.*

4. No Operation — MPI Command

(06h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	0	0	0	0	1	1	0

5. Activate Channel (Operational Mode) — MPI Command

(0Eh)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	0	0	0	1	1	1	0

This command places the device in the Active mode and sets $\overline{CS}$ = 1. No valid PCM data is transmitted until after the second FS pulse is received following the execution of the Activate command.

6, 7. Write/Read Transmit Time Slot and PCM Highway Selection — MPI Command

(40/41h)

R/W = 0: Write

R/W = 1: Read

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	0	0	0	0	0	R/W
I/O Data	TPCM	TTS6	TTS5	TTS4	TTS3	TTS2	TTS1	TTS0

Transmit PCM Highway

TPCM = 0* Transmit on Highway A (see TAB in Commands 10, 11)
TPCM = 1 Transmit on Highway B (see TAB in Commands 10, 11)

Transmit Time Slot

TTS = 0–127 Time Slot Number (TTS0 is LSB, TTS6 is MSB)

PCM Highway B is not available on the Am79Q061/062 QSLAC devices.

* Power Up and Hardware Reset ($\overline{RST}$) Value = 00h, 01h, 02h, 03h for Channels 1, 2, 3, and 4, respectively.

8, 9. Write/Read Receive Time Slot and PCM Highway Selection — MPI Command

(42/43h)

R/W = 0: Write

R/W = 1: Read

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	0	0	0	0	1	R/W
I/O Data	RPCM	RTS6	RTS5	RTS4	RTS3	RTS2	RTS1	RTS0

Receive PCM Highway

RPCM = 0* Receive on Highway A
RPCM = 1 Receive on Highway B

Receive Time Slot

RTS = 0–127 Time Slot Number (RTS0 is LSB, RTS6 is MSB)

PCM Highway B is not available on the Am79Q061 and the Am79Q062 QSLAC devices.

* Power Up and Hardware Reset ($\overline{RST}$) Value = 00h, 01h, 02h, 03h for Channels 1, 2, 3, and 4, respectively.

10, 11. Write/Read Transmit Clock Slot, Receive Clock Slot, and Transmit Clock Edge MPI Command

(44/45h)

R/W = 0: Write

R/W = 1: Read

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	0	0	0	1	0	R/W
I/O Data	TAB	XE	RCS2	RCS1	RCS0	TCS2	TCS1	TCS0

Transmit on A and B

TAB = 0*	Transmit data on highway selected by TPCM (See Commands 6,7 on page 46).
TAB = 1	Transmit data on both highways A and B

Transmit Edge

XE = 0*	Transmit changes on negative edge of PCLK
XE = 1	Transmit changes on positive edge of PCLK

Receive Clock Slot

RCS = 0*–7	Receive Clock Slot number

Transmit Clock Slot

TCS = 0*–7	Transmit Clock Slot number

The XE bit and the clock slots apply to all four channels; however, they cannot be written or read unless at least one channel is selected in the Channel Enable Register.

* Power Up and Hardware Reset ($\overline{RST}$) Value = 00h.

12, 13. Write/Read Configuration Register MPI Command

(46/47h)

R/W = 0: Write

R/W = 1: Read

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	0	0	0	1	1	R/W
I/O Data	INTM	CHP	SMODE	CMODE	CSEL3	CSEL2	CSEL1	CSEL0

Interrupt Mode

INTM = 0	TTL-compatible output
INTM = 1*	Open drain output

Chopper Clock Control

CHP = 0*	Chopper Clock is 256 kHz (2048/8 kHz)
CHP = 1	Chopper Clock is 292.57 kHz (2048/7 kHz)

PCM Signaling Mode

SMODE = 0*	No signaling on PCM highway
SMODE = 1	Signaling on PCM highway

Clock Source Mode

CMODE = 0	MCLK used as master clock; no E1 multiplexing allowed
CMODE = 1*	PCLK used as master clock; E1 multiplexing allowed if enabled in commands 49, 50.

The master clock frequency can be selected by CSEL. The master clock frequency selection affects all channels.

Master Clock Frequency

CSEL = 0000	1.536 MHz
CSEL = 0001	1.544 MHz
CSEL = 0010	2.048 MHz
CSEL = 0011	Reserved
CSEL = 01xx	Two times the frequency specified above (2 x 1.536 MHz, 2 x 1.544 MHz, or 2 x 2.048 MHz)
CSEL = 10xx	Four times frequency specified above (4 x 1.536 MHz, 4 x 1.544 MHz, or 4 x 2.048 MHz)
CSEL = 11xx	Reserved
CSEL = 1010*	8.192 MHz is the default

These commands do not depend on the state of the Channel Enable Register.

* Power Up and Hardware Reset ($\overline{RST}$) Value = 9Ah.

14, 15. Write/Read Channel Enable and Operating Mode Register (4A/4B) — MPI Command

R/W = 0: Write

R/W = 1: Read

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	0	0	1	0	1	R/W
I/O Data	RSVD	RBE	VMODE	LPM	EC4	EC3	EC2	EC1

RSVD Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

Robbed-bit Mode

RBE = 0*	Robbed-bit Signaling mode is disabled.
RBE = 1	Robbed-bit Signaling mode is enabled on PCM receiver if μ-law is selected.

VOUT Mode

VMODE = 0*	VOUT = VREF through a resistor when channel is deactivated
VMODE = 1	VOUT high impedance when channel is deactivated.

Low Power Mode

LPM = 0*	Low Power mode off
LPM = 1	Low Power mode on while all channels are inactive

Enable Channel 4

EC4 = 0	Disabled, Channel 4 cannot receive commands
EC4 = 1*	Enabled, Channel 4 can receive commands

Enable Channel 3

EC3 = 0	Disabled, Channel 3 cannot receive commands
EC3 = 1*	Enabled, Channel 3 can receive commands

Enable Channel 2

EC2 = 0	Disabled, Channel 2 cannot receive commands
EC2 = 1*	Enabled, Channel 2 can receive commands

Enable Channel 1

EC1 = 0	Disabled, Channel 1 cannot receive commands
EC1 = 1*	Enabled, Channel 1 can receive commands

* Power Up and Hardware Reset ($\overline{RST}$) Value = 0Fh.

16, 17. Read Real-Time Data Register — MPI Command

(4D/4Fh)

C = 0: Do not clear interrupt

C = 1: Clear interrupt

This register writes/reads real-time data with or without clearing the interrupt.

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	0	0	1	1	C	1
Output Data	CDB4	CDA4	CDB3	CDA3	CDB2	CDA2	CDB1	CDA1

Real Time Data

CDA1	Debounced data bit 1 on Channel 1
CDB1	Data bit 2 or multiplexed data bit 1 on Channel 1
CDA2	Debounced data bit 1 on Channel 2
CDB2	Data bit 2 or multiplexed data bit 1 on Channel 2
CDA3	Debounced data bit 1 on Channel 3
CDB3	Data bit 2 or multiplexed data bit 1 on Channel 3
CDA4	Debounced data bit 1 on Channel 4
CDB4	Data bit 2 or multiplexed data bit 1 on Channel 4

This command does not depend on the state of the Channel Enable Register.

18, 19. Write/Read AISN and Analog Gains — MPI Command

(50/51h)

R/W = 0: Write

R/W = 1: Read

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	0	1	0	0	0	R/W
I/O Data	RSVD	AX	AR	AISN4	AISN3	AISN2	AISN1	AISN0

RSVD Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

Transmit Analog Gain

AX = 0*	0 dB gain
AX = 1	6.02 dB gain

Receive Analog Loss

AR = 0*	0 dB loss
AR = 1	6.02 dB loss

AISN coefficient

AISN = 0* – 31 See below (Default value = 0)

The Impedance Scaling Network (AISN) gain can be varied from –0.9375 to 0.9375 in multiples of 0.0625. The gain coefficient is decoded using the following equation:

$$h_{AISN} = 0.0625[(16 \bullet AISN4 + 8 \bullet AISN3 + 4 \bullet AISN2 + 2 \bullet AISN1 + AISN0) - 16]$$

where h_{AISN} is the gain of the AISN. A value of AISN = 10000 turns on the Full Digital Loopback mode and a value of AISN = 0000* indicates a gain of 0 (cutoff).

* Power Up and Hardware Reset ($\overline{RST}$) Value = 00h.

20, 21. Write/Read SLIC Input/Output Register — MPI Command

(52/53h)

R/W = 0: Write

R/W = 1: Read

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	0	1	0	0	1	R/W
I/O Data	C7	C6	CD1B	C5	C4	C3	CD2	CD1

Pins CD1, CD2, and C3 through C7 are set to 1 or 0. The data appears latched on the CD1, CD2, and C3 through C5 SLIC I/O pins, provided they were set in the Output mode (see Command 22). The data sent to any of the pins set to the Input mode is latched, but does not appear at the pins. The CD1B bit is only valid if the E1 Multiplex mode is enabled (EE1 = 1). C7 and C6 are outputs only and are not available on all package types.

* Power Up and Hardware Reset ($\overline{RST}$) Value = 00h

22, 23. Write/Read SLIC Input/Output Direction, Read Status Bits — MPI Command

(54/55h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	0	1	0	1	0	R/W
Input Data	RSVD	CSTAT	CFAIL	IOD5	IOD4	IOD3	IOD2	IOD1

RSVD   Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

Channel Status (Read status only, write as 0)

CSTAT = 0   Channel is inactive (Standby mode).
CSTAT = 1   Channel is active.

Clock Fail (Read status only, write as 0)

CFAIL* = 0   The internal clock is synchronized to frame synch.
CFAIL = 1   The internal clock is not synchronized to frame synch.
* The CFAIL bit is independent of the Channel Enable Register.

I/O Direction (Read/Write)

IOD5 = 0*   C5 is an input
IOD5 = 1   C5 is an output
IOD4 = 0*   C4 is an input
IOD4 = 1   C4 is an output
IOD3 = 0*   C3 is an input
IOD3 = 1   C3 is an output
IOD2 = 0*   CD2 is an input
IOD2 = 1   CD2 is an output
IOD1 = 0*   CD1 is an input
IOD1 = 1   CD1 is an output

Pins CD1, CD2, and C3 through C5 are set to Input or Output modes individually. Pins C3–C5 are not available on the Am79Q062 QSLAC device, and C5 is available only on the Am79Q061 QSLAC device.

* Power Up and Hardware Reset ($\overline{RST}$) Value = 00h

24, 25. Write/Read Operating Functions MPI Command

(60/61h)

R/W = 0: Write
R/W = 1: Read

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	1	0	0	0	0	R/W
I/O Data	C/L	A/μ	EGR	EGX	EX	ER	EZ	EB

Linear Code

C/L = 0*	Compressed coding
C/L = 1	Linear coding

A-law or μ-law

A/μ = 0*	A-law coding
A/μ = 1	μ-law coding

GR Filter

EGR = 0*	Default GR filter enabled
EGR = 1	Programmed GR filter enabled

GX Filter

EGX = 0*	Default GX filter enabled
EGX = 1	Programmed GX filter enabled

X Filter

EX = 0*	Default X filter enabled
EX = 1	Programmed X filter enabled

R Filter

ER = 0*	Default R filter enabled
ER = 1	Programmed R filter enabled

Z Filter

EZ = 0*	Default Z filter enabled
EZ = 1	Programmed Z filter enabled

B Filter

EB = 0*	Default B filter enabled
EB = 1	Programmed B filter enabled

* Power Up and Hardware Reset ($\overline{RST}$) Value = 00h.

26, 27. Write/Read Interrupt Mask Register — MPI Command

(6C/6Dh)

R/W = 0: Write

R/W = 1: Read

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	1	0	1	1	0	R/W
I/O Data	MCDB4	MCDA4	MCDB3	MCDA3	MCDB2	MCDA2	MCDB1	MCDA1

Mask CD Interrupt

MCDxy = 0 — CDxy bit is NOT MASKED
MCDxy = 1* — CDxy bit is MASKED
x — Bit number (A or B)
y — Channel number (1 through 4)
Masked: A change does not cause the Interrupt Pin to go Low.

This command does not depend on the state of the Channel Enable Register.

* Power Up and Hardware Reset ($\overline{RST}$) Value = FFh.

28, 29. Write/Read Operating Conditions — MPI Command

(70/71h)

R/W = 0: Write

R/W = 1: Read

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	1	1	0	0	0	R/W
I/O Data	CTP	CRP	HPF	LRG	ATI	ILB	FDL	TON

Cutoff Transmit Path

CTP = 0* — Transmit path connected
CTP = 1 — Transmit path cut off

Cutoff Receive Path

CRP = 0* — Receive path connected
CRP = 1 — Receive path cutoff (see note)

High Pass Filter

HPF = 0* — Transmit Highpass filter enabled
HPF = 1 — Transmit Highpass filter disabled

Lower Receive Gain

LRG = 0* — 6 dB loss not inserted
LRG = 1 — 6 dB loss inserted

Arm Transmit Interrupt

ATI = 0* — Transmit Interrupt not Armed
ATI = 1 — Transmit Interrupt Armed

Interface Loopback

ILB = 0* — TSA loopback disabled
ILB = 1 — TSA loopback enabled

Full Digital Loopback

FDL = 0* — Full digital loopback disabled
FDL = 1 — Full digital loopback enabled

1 kHz Receive Tone

TON = 0* 1 kHz receive tone off
TON = 1 1 kHz receive tone on

* Power Up and Hardware Reset ($\overline{RST}$) Value = 00h.

The B Filter is disabled during receive cutoff.

30. Read Revision Code Number (RCN) MPI Command

(73h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	1	1	0	0	1	1
I/O Data	RCN7	RCN6	RCN5	RCN4	RCN3	RCN2	RCN1	RCN0

This command returns an 8-bit number (RCN) describing the revision number of the QSLAC device. This command does not depend on the state of the Channel Enable Register.

31, 32. Write/Read GX Filter Coefficients MPI Command

(80/81h)

R/W = 0: Write

R/W = 1: Read

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	0	0	0	0	R/W
I/O Data Byte 1	C40	m40			C30	m30		
I/O Data Byte 2	C20	m20			C10	m10		

The coefficient for the GX filter is defined as:

$$H_{GX} = 1 + (C10 \bullet 2^{-m10}\{1 + C20 \bullet 2^{-m20}[1 + C30 \bullet 2^{-m30}(1 + C40 \bullet 2^{-m40})]\})$$

Power Up and Hardware Reset ($\overline{RST}$) Values = A9F0 (Hex) (H_{GX} = 1.995 (6 dB)).

Note: *The default value is contained in a ROM register separate from the programmable coefficient RAM. There is a filter enable bit in Operating Functions Register to switch between the default and programmed values.*

33, 34. Write/Read GR Filter Coefficients MPI Command

(82/83h)

R/W = 0: Write

R/W = 1: Read

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	0	0	1	R/W
I/O Data Byte 1	C40	m40			C30	m30		
I/O Data Byte 2	C20	m20			C10	m10		

The coefficient for the GR filter is defined as:

$$H_{GR} = C10 \bullet 2^{-m10}\{1 + C20 \bullet 2^{-m20}[1 + C30 \bullet 2^{-m30}(1 + C40 \bullet 2^{-m40})]\}$$

Power Up and Hardware Reset ($\overline{RST}$) Values = 23A1 (Hex) (H_{GR} = 0.35547 (–8.984 dB)).

See note under Commands 31 and 32.

35, 36. Write/Read Z Filter Coefficients (FIR and IIR) MPI Command

(84/85h)

R/W = 0: Write

R/W = 1: Read

This command writes and reads both the FIR and IIR filter sections simultaneously.

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	0	0	1	0	R/W
I/O Data Byte 1	C40	m40			C30	m30		
I/O Data Byte 2	C20	m20			C10	m10		
I/O Data Byte 3	C41	m41			C31	m31		
I/O Data Byte 4	C21	m21			C11	m11		
I/O Data Byte 5	C42	m42			C32	m32		
I/O Data Byte 6	C22	m22			C12	m12		
I/O Data Byte 7	C43	m43			C33	m33		
I/O Data Byte 8	C23	m23			C13	m13		
I/O Data Byte 9	C44	m44			C34	m34		
I/O Data Byte 10	C24	m24			C14	m14		
I/O Data Byte 11	C45	m45			C35	m35		
I/O Data Byte 12	C25	m25			C15	m15		
I/O Data Byte 13	C26	m26			C16	m16		
I/O Data Byte 14	C47	m47			C37	m37		
I/O Data Byte 15	C27	m27			C17	m17		

The Z-transform equation for the Z filter is defined as:

$$H_z(z) = z_0 + z_1 \bullet z^{-1} + z_2 \bullet z^{-2} + z_3 \bullet z^{-3} + z_4 \bullet z^{-4} + \frac{z_5 \bullet z_6 \bullet z_7 \bullet z^{-1}}{1 - z_7 \bullet z^{-1}}$$

Sample rate = 32 kHz

For i = 0 to 5 and 7

$$z_i = C1i \bullet 2^{-m1i}\{1 + C2i \bullet 2^{-m2i}[1 + C3i \bullet 2^{-m3i}(1 + C4i \bullet 2^{-m4i})]\}$$

$$z_6 = C16 \bullet 2^{-m16}\{1 + C26 \bullet 2^{-m26}\}$$

Power Up and Hardware Reset ($\overline{RST}$) Values = 0190 0190 0190 0190 0190 0190 01 0190 (Hex)

($H_z(z) = 0$)

See note under Commands 31 and 32.

Note: *Z_6 is used for IIR filter scaling only. Its value is typically greater than zero but less than or equal to one. The input to the IIR filter section is first increased by a gain of $1/Z_6$, improving dynamic range and avoiding truncation limitations through processing within this filter. The IIR filter output is then multiplied by Z_6 to normalize the overall gain. Z_5 is the actual IIR filter gain value defined by the programmed coefficients, but it also includes the initial $1/Z_6$ gain. The theoretical effective IIR gain, without the Z_6 gain and normalization, is actually Z_5/Z_6.*

37, 38. Write/Read B1 Filter Coefficients — MPI Command

(86/87h)

R/W = 0: Write

R/W = 1: Read

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	0	0	1	1	R/W
I/O Input Data Byte 1	C32	m32			C22	m22		
I/O Input Data Byte 2	C12	m12			C33	m33		
I/O Input Data Byte 3	C23	m23			C13	m13		
I/O Input Data Byte 4	C34	m34			C24	m24		
I/O Input Data Byte 5	C14	m14			C35	m35		
I/O Input Data Byte 6	C25	m25			C15	m15		
I/O Input Data Byte 7	C36	m36			C26	m26		
I/O Input Data Byte 8	C16	m16			C37	m37		
I/O Input Data Byte 9	C27	m27			C17	m17		
I/O Input Data Byte 10	C38	m38			C28	m28		
I/O Input Data Byte 11	C18	m18			C39	m39		
I/O Input Data Byte 12	C29	m29			C19	m19		
I/O Input Data Byte 13	C310	m310			C210	m210		
I/O Input Data Byte 14	C110	m110			RSVD	RSVD		

The Z-transform equation for the B filter is defined as:

$$H_B(z) = B_2 \bullet z^{-2} + \ldots + B_9 \bullet z^{-9} + \frac{B_{10} \bullet z^{-10}}{1 - B_{11} \bullet z^{-1}}$$

Sample rate = 16 kHz

The coefficients for the FIR B section and the gain of the IIR B section are defined as:

For i = 2 to 10,

$$B_i = C1i \bullet 2^{-m1i}[1 + C2i \bullet 2^{-m2i}(1 + C3i \bullet 2^{-m3i})]$$

The feedback coefficient of the IIR B section is defined as:

$$B_{11} = C111 \bullet 2^{-m111}\{1 + C211 \bullet 2^{-m211}[1 + C311 \bullet 2^{-m311}(1 + C411 \bullet 2^{-m411})]\}$$

Refer to Commands 43, 44 for programming the B_{11} coefficient.

Power Up and Hardware Reset ($\overline{RST}$) Values = 36 AB B8 22 93 AB 2B 6C 46 2C 63 B6 9F 60 (Hex)

$$(H_B(z) = -0.254 \bullet z^{-2} - 0.891 \bullet z^{-3} - 0.656 \bullet z^{-4} - 0.090 \bullet z^{-5} + 0.013 \bullet z^{-6} + 0.017 \bullet z^{-7}$$
$$+ 0.014 \bullet z^{-8} + 0.013 \bullet z^{-9} + \frac{0.016 \bullet z^{-10}}{1 - 0.97656 \bullet z^{-1}})$$

See note under Commands 31 and 32.

RSVD Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

39, 40. Write/Read X Filter Coefficients — MPI Command

(88/89h)

R/W = 0: Write

R/W = 1: Read

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	0	1	0	0	R/W
I/O Input Data Byte 1	C40	m40			C30	m30		
I/O Input Data Byte 2	C20	m20			C10	m10		
I/O Input Data Byte 3	C41	m41			C31	m31		
I/O Input Data Byte 4	C21	m21			C11	m11		
I/O Input Data Byte 5	C42	m42			C32	m32		
I/O Input Data Byte 6	C22	m22			C12	m12		
I/O Input Data Byte 7	C43	m43			C33	m33		
I/O Input Data Byte 8	C23	m23			C13	m13		
I/O Input Data Byte 9	C44	m44			C34	m34		
I/O Input Data Byte 10	C24	m24			C14	m14		
I/O Input Data Byte 11	C45	m45			C35	m35		
I/O Input Data Byte 12	C25	m25			C15	m15		

The Z-transform equation for the X filter is defined as:

$$H_x(z) = x_0 + x_1 z^{-1} + x_2 z^{-2} + x_3 z^{-3} + x_4 z^{-4} + x_5 z^{-5}$$

Sample rate = 16 kHz

For i = 0 to 5, the coefficients for the X filter are defined as:

$$Xi = C1i \bullet 2^{-m1i}\{1 + C2i \bullet 2^{-m2i}[1 + C3i \bullet 2^{-m3i}(1 + C4i \bullet 2^{-m4i})]\}$$

Power Up and Hardware Reset ($\overline{RST}$) Values = 0111 0190 0190 0190 0190 0190 (Hex)

($H_x(z) = 1$)

See note under Commands 31 and 32.

41, 42. Write/Read R Filter Coefficients — MPI Command

(8A/8Bh)

R/W = 0: Write

R/W = 1: Read

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	0	1	0	1	R/W
I/O Input Data Byte 1	C46	m46			C36	m36		
I/O Input Data Byte 2	C26	m26			C16	m16		
I/O Input Data Byte 3	C40	m40			C30	m30		
I/O Input Data Byte 4	C20	m20			C10	m10		
I/O Input Data Byte 5	C41	m41			C31	m31		
I/O Input Data Byte 6	C21	m21			C11	m11		
I/O Input Data Byte 7	C42	m42			C32	m32		
I/O Input Data Byte 8	C22	m22			C12	m12		
I/O Input Data Byte 9	C43	m43			C33	m33		
I/O Input Data Byte 10	C23	m23			C13	m13		
I/O Input Data Byte 11	C44	m44			C34	m34		
I/O Input Data Byte 12	C24	m24			C14	m14		
I/O Input Data Byte 13	C45	m45			C35	m35		
I/O Input Data Byte 14	C25	m25			C15	m15		

$$HR = H_{IIR} \bullet H_{FIR}$$

The Z-transform equation for the IIR filter is defined as:

$$H_{IIR} = \frac{1 - z^{-1}}{1 - (R_6 \bullet z^{-1})}$$

Sample rate = 8 kHz

The coefficient for the IIR filter is defined as:

$$R_6 = C16 \bullet 2^{-m16}\{1 + C26 \bullet 2^{-m26}[1 + C36 \bullet 2^{-m36}(1 + C46 \bullet 2^{-m46})]\}$$

The Z-transform equation for the FIR filter is defined as:

$$H_{FIR}(z) = R_0 + R_1 z^{-1} + R_2 z^{-2} + R_3 z^{-3} + R_4 z^{-4} + R_5 z^{-5}$$

Sample rate = 16 kHz

For i = 0 to 5, the coefficients for the R2 filter are defined as:

$$R_i = C1i \bullet 2^{-m1i}\{1 + C2i \bullet 2^{-m2i}[1 + C3i \bullet 2^{-m3i}(1 + C4i \bullet 2^{-m4i})]\}$$

Power Up and Hardware Reset ($\overline{RST}$) Values = 2E01 0111 0190 0190 0190 0190 0190 (Hex)

(H_{FIR} (z) = 1, R_6 = 0.9902)

See note under Commands 31 and 32.

43, 44. Write/Read B2 Filter Coefficients (IIR) — MPI Command

(96/97h)

R/W = 0: Write

R/W = 1: Read

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	1	0	1	1	R/W
I/O Data Byte 1	C411	m411			C311	m311		
I/O Data Byte 2	C211	m211			C111	m111		

This function is described in *Write/Read B1 Filter Coefficients (FIR)* on page 55.

Power Up and Hardware Reset ($\overline{RST}$) Values = AC01 (Hex) (B_{11} = 0.97656)

See note under Commands 31 and 32.

45, 46. Write/Read Debounce Time Register** — MPI Command

(C8/C9h)

R/W = 0: Write

R/W = 1: Read

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	1	0	0	1	0	0	R/W
I/O Data	EE1	E1P	DSH3	DSH2	DSH1	DSH0	DPCK	ECH

Enable E1

EE1 = 0* E1 multiplexing turned off
EE1 = 1 E1 multiplexing turned on

E1 Polarity

E1P = 0* E1 is a high-going pulse
E1P = 1 E1 is a low-going pulse
There is no E1 output unless CMODE = 1.

Debounce for Switchhook

DSH = 0–15 Debounce period in ms
DSH contains the debouncing time (in ms) of the CD1 data (usually switchhook) entering the Real Time Data register described earlier. The input data must remain stable for the debouncing time in order to change the appropriate real time bit.

Double PCLK Operation

DPCK = 0* Double PCLK operation is off. PCLK and PCM data at same rate.
DPCK = 1 Double PCLK enabled. PCLK operates at twice the PCM data rate.

Enable Chopper

ECH = 0* Chopper output (CHCLK) turned off
ECH = 1 Chopper output (CHCLK) turned on

* Power Up and Hardware Reset ($\overline{RST}$) Value = 20h.

** This command applies to all channels and does not depend on the state of the Channel Enable Register.

47. Read Transmit PCM Data (PCM/MPI Mode Only) — MPI Command

(CDh)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	1	0	0	1	1	0	1
Output Data Byte 1	XDAT7	XDAT6	XDAT5	XDAT4	XDAT3	XDAT2	XDAT1	XDAT0
Output Data Byte 2	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	OLD

RSVD Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

Upper Transmit Data

XDAT contains A-law or µ-law transmit data in Companded mode.
XDAT contains upper data byte in Linear mode with sign in XDAT7.

Old Data Flag

OLD = 0 Transmit data byte contains new data.
OLD = 1 Transmit data byte contains old data.

This command will return the 2 byte GCI channel ID if GCI mode is selected.

48, 49. Write/Read FIR Z Filter Coefficients (FIR only) — MPI Command

(98/99h)

R/W = 0: Write

R/W = 1: Read

This command writes and reads only the FIR filter section without affecting the IIR.

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	1	1	0	0	R/W
I/O Data Byte 1	C40	m40			C30	m30		
I/O Data Byte 2	C20	m20			C10	m10		
I/O Data Byte 3	C41	m41			C31	m31		
I/O Data Byte 4	C21	m21			C11	m11		
I/O Data Byte 5	C42	m42			C32	m32		
I/O Data Byte 6	C22	m22			C12	m12		
I/O Data Byte 7	C43	m43			C33	m33		
I/O Data Byte 8	C23	m23			C13	m13		
I/O Data Byte 9	C44	m44			C34	m34		
I/O Data Byte 10	C24	m24			C14	m14		

The Z-transform equation for the Z filter is defined as:

$$H_z(z) = z_0 + z_1 \bullet z^{-1} + z_2 \bullet z^{-2} + z_3 \bullet z^{-3} + z_4 \bullet z^{-4} + \frac{z_5 \bullet z_6 \bullet z_7 \bullet z^{-1}}{1 - z_7 \bullet z^{-1}}$$

Sample rate = 32 kHz

For i = 0 to 5 and 7

$$z_i = C1i \bullet 2^{-m1i}\{1 + C2i \bullet 2^{-m2i}[1 + C3i \bullet 2^{-m3i}(1 + C4i \bullet 2^{-m4i})]\}$$

$$z_6 = C16 \bullet 2^{-m16}\{1 + C26 \bullet 2^{-m26}\}$$

Power Up and Hardware Reset ($\overline{RST}$) Values = 0190 0190 0190 0190 0190 0190 01 0190 (Hex)

($H_z(z) = 0$)

See note under Commands 31 and 32.

Note: *Z_6 is used for IIR filter scaling only. Its value is typically greater than zero but less than or equal to one. The input to the IIR filter section is first increased by a gain of $1/Z_6$, improving dynamic range and avoiding truncation limitations through processing within this filter. The IIR filter output is then multiplied by Z_6 to normalize the overall gain. Z_5 is the actual IIR filter gain value defined by the programmed coefficients, but it also includes the initial $1/Z_6$ gain. The theoretical effective IIR gain, without the Z_6 gain and normalization, is actually Z_5/Z_6.*

50, 51. Write/Read IIR Z Filter Coefficients (IIR only) MPI Command

(9A/9Bh)

R/W = 0: Write

R/W = 1: Read

This command writes/reads the IIR filter section only, without affecting the FIR.

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	1	1	0	1	R/W
I/O Data Byte 11	C45	m45			C35	m35		
I/O Data Byte 12	C25	m25			C15	m15		
I/O Data Byte 13	C26	m26			C16	m16		
I/O Data Byte 14	C47	m47			C37	m37		
I/O Data Byte 15	C27	m27			C17	m17		

The Z-transform equation for the Z filter is defined as:

$$H_z(z) = z_0 + z_1 \bullet z^{-1} + z_2 \bullet z^{-2} + z_3 \bullet z^{-3} + z_4 \bullet z^{-4} + \frac{z_5 \bullet z_6 \bullet z_7 \bullet z^{-1}}{1 - z_7 \bullet z^{-1}}$$

Sample rate = 32 kHz

For i = 0 to 5 and 7

$$z_i = C1i \bullet 2^{-m1i}\{1 + C2i \bullet 2^{-m2i}[1 + C3i \bullet 2^{-m3i}(1 + C4i \bullet 2^{-m4i})]\}$$

$$z_6 = C16 \bullet 2^{-m16}\{1 + C26 \bullet 2^{-m26}\}$$

Power Up and Hardware Reset ($\overline{RST}$) Values = 0190 0190 0190 0190 0190 0190 01 0190 (Hex)

($H_z(z) = 0$)

See note under Commands 31 and 32.

Note: *Z_6 is used for IIR filter scaling only. Its value is typically greater than zero but less than or equal to one. The input to the IIR filter section is first increased by a gain of $1/Z_6$, improving dynamic range and avoiding truncation limitations through processing within this filter. The IIR filter output is then multiplied by Z_6 to normalize the overall gain. Z_5 is the actual IIR filter gain value defined by the programmed coefficients, but it also includes the initial $1/Z_6$ gain. The theoretical effective IIR gain, without the Z_6 gain and normalization, is actually Z_5/Z_6.*

52, 53. Write/Read Ground Key Filter — MPI Command

(E8/E9h)

R/W = 0: Write

R/W = 1: Read

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	1	1	0	1	0	0	R/W
I/O Data	RSVD	RSVD	RSVD	RSVD	GK3	GK2	GK1	GK0

Filter Ground Key

GK = 0–15 Filter sampling period in 1 ms

GK contains the filter sampling time (in ms) of the CD1B data (usually Ground Key) or CD2 entering the Real Time Data register described earlier. A value of 0 disables the Ground Key filter for that particular channel.

Power Up and Hardware Reset ($\overline{RST}$) Value = 00h.

RSVD Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

GENERAL CIRCUIT INTERFACE (GCI) SPECIFICATIONS

GCI General Description

When the $\overline{CS}$/PG device pin is connected to GND and DCLK/S0 is static (not toggling), GCI operation is selected. The QSLAC device conforms to the GCI standard where data for eight GCI channels are combined into one serial bit stream. A GCI channel contains the control and voice data for two analog channels of the QSLAC device. Two GCI channels are required to access all four channels of the QSLAC device. The QSLAC device sends Data Upstream out of the DU pin and receives Downstream Data on the DD pin. Data clock rate and frame synchronization information goes to the QSLAC device on the DCL (Data Clock) and FSC input pins, respectively. Two of eight GCI channels are selected by connecting the S0 and S1 channel selection pins on the QSLAC device to GND or VCC as shown in Table 3.

Table 3. GCI Channel Assignment Codes

S1	S0	GCI Channels #
GND	GND	0 & 1
GND	VCC	2 & 3
VCC	GND	4 & 5
VCC	VCC	6 & 7

In the time slot control block (shown in Figure 14), the Frame Sync (FSC) pulse identifies the beginning of the Transmit and Receive frames and all GCI channels are referenced to it. Voice (B1 and B2), C/I, and monitor data are sent to the Upstream Multiplexer where they are combined and serially shifted out of the DU pin during the selected GCI Channels. The Downstream Demultiplexer uses the same channel control block information to demultiplex the incoming GCI channels into separate voice (B1 and B2), C/I, and monitor data bytes.

The QSLAC device supports an eight GCI channel bus (16 analog channels). The external clock applied to the DCL pin is either 2.048 MHz or 4.096 MHz. The QSLAC device determines the incoming clock frequency and adjusts internal timing automatically to accommodate single or double clock rates.

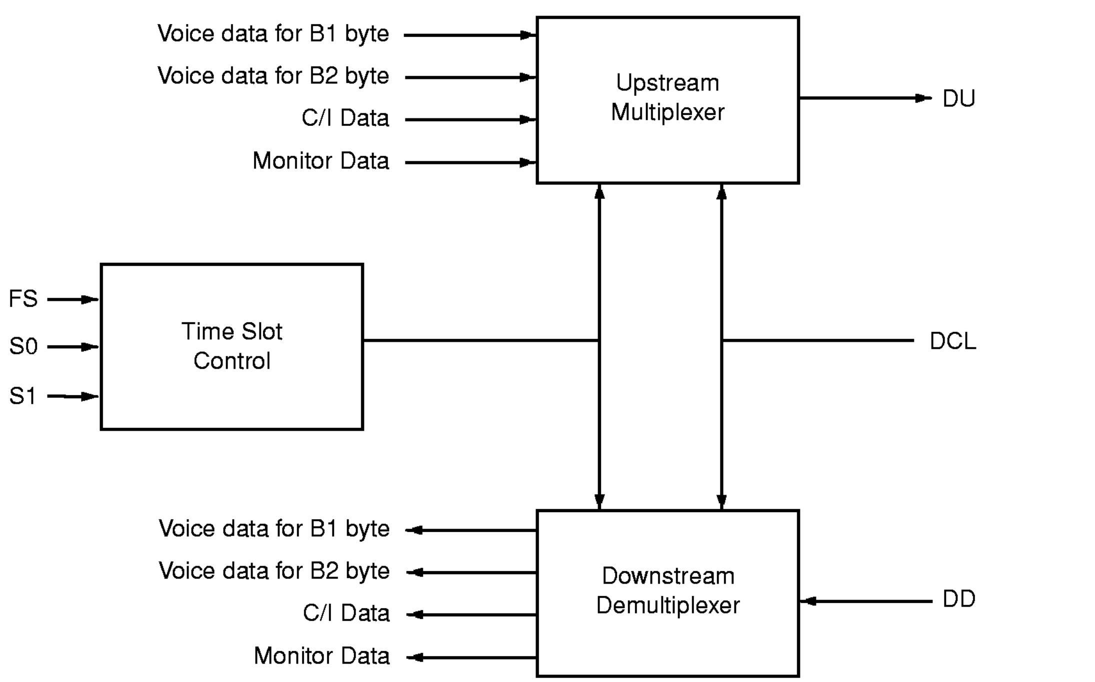


Figure 14. Time Slot Control and GCI Interface

GCI Format and Command Structure

The GCI interface provides communication of both control and voice data between the GCI highway and subscriber line circuits over a single pair of pins on the QSLAC device. A complete GCI frame is sent upstream on the DU pin and received downstream on the DD pin every 125 µs. Each frame consists of eight 4 byte GCI channels (CHN0 to 7) that contain voice and control information for eight pairs of channels. A particular channel pair is identified by its position within the frame (see Figure 15). Therefore, a total of 16 voice channels can be uniquely addressed each frame. The overall structure of the GCI frame is shown in Figure 15.

The 4 byte GCI channel contains the following:

- 2 bytes; B1 and B2 for voice channels 1 and 2.
- One Monitor (M) byte for reading/writing control data/coefficients to the QSLAC for both channels.
- One Signaling and Control (SC) byte containing a 6-bit Command/Indicate (C/I) channel for control information and a 2-bit field with Monitor Receive and Monitor Transmit (MR, MX) bits for handshaking functions for both channels. All principal signaling (real-time critical) information is carried on the C/I channel. The QSLAC device utilizes the full C/I channel capacity of the GCI channel.

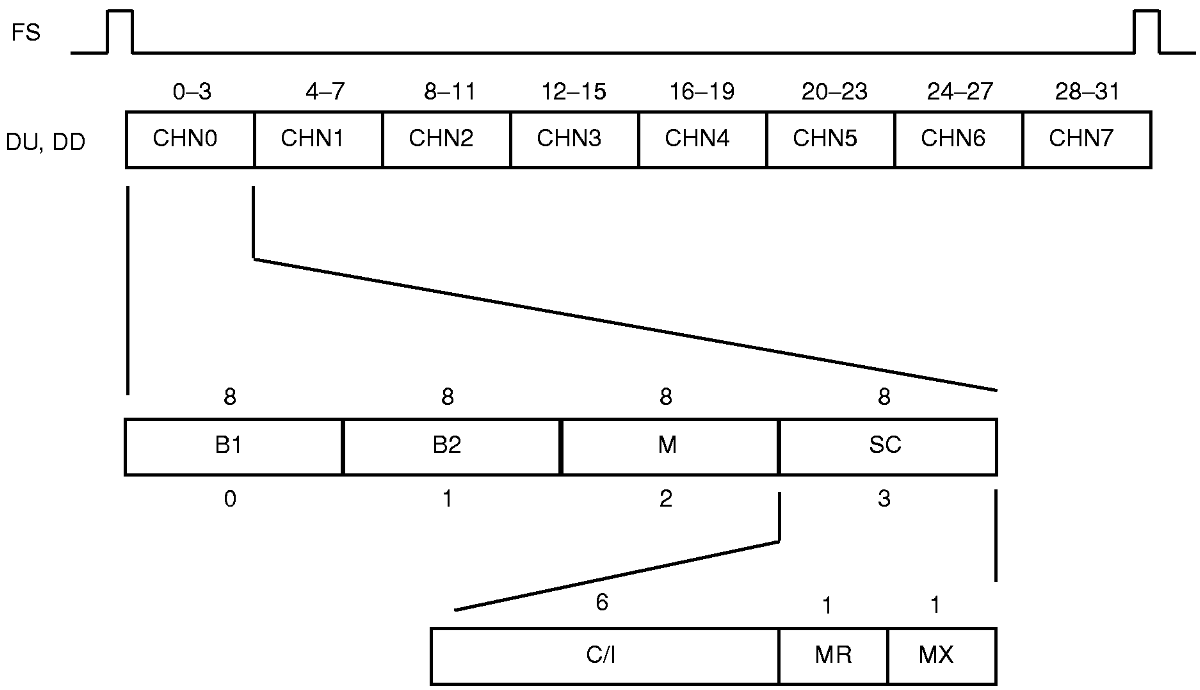


Figure 15. Multiplexed GCI Time Slot Structure

21108A-029

SC Channel

The upstream and downstream SC channels are continuously carrying I/O information every frame to and from the QSLAC device in the C/I field. This allows the upstream processor to have immediate access to the output (downstream) and input (upstream) data present on the QSLAC device's programmable I/O port.

The MR and MX bits are used for handshaking during data exchanges on the monitor channel.

Downstream C/I Channel

The QSLAC device receives the MSBs first.

The downstream C/I channel SC octet definition depends on the device package type. The 44-pin and 32-pin packages do not have provisions for pin connections to accommodate all SLIC outputs, which otherwise are available on the higher pin count devices. For the 32-pin and 44-pin package devices, the downstream SC octet is defined as:

<---------------- Downstream SC Octet ------------------>

MSB							LSB
7	6	5	4	3	2	1	0
A	$C5_x$	$C4_x$	$C3_x$	$CD2_x$	$CD1_x$	MR	MX

|<------------------- C/I Field ------------------->|

For the 64-pin packages, this octet is defined as:

<---------------- Downstream SC Octet ------------------>

MSB							LSB
7	6	5	4	3	2	1	0
A	$C7_x$	$C6_x$	$C5_x$	$CD4_x$	$CD3_x$	MR	MX

|<------------------- C/I Field ------------------->|

A: Channel Address Bit

0: Selects CH 1 as the downstream data destination
1: Selects CH 2 as the downstream data destination

$C5_x$–$CD2_x$, $CD1_x$: Output bits 5–1 for CHx of the channel selected by A. (32- and 44-pin packages)

$C7_x$–$C3_x$: SLIC output bits 7–3 of the channel selected by A. (64-pin packages)

x = 1 or 2, the channel selected by A

If the QSLAC device's programmable I/O ports, CD1, CD2, and C3 are programmed for Input mode, then data is obtained through the Upstream C/I channel.

Figure 16 shows the transmission protocol for the downstream C/I. Whenever the received pattern of C/I bits 6–1 is different from the pattern currently in the C/I input register, the new pattern is loaded into a secondary C/I register and a latch is set. When the next pattern is received (in the following frame) while the latch is set, the following rules apply:

1. If the received pattern corresponds to the pattern in the secondary register, the new pattern is loaded into the C/I register for the addressed channel and the latch is reset. The updated C/I register data appears at the programmable I/O pins of the device one frame (125 µs) later if they are programmed as outputs.
2. If the received pattern is different from the pattern in the secondary register and different from the pattern currently in the C/I register, the newly received pattern is loaded into the secondary C/I register and the latch remains set. The data at the PI/O port remains unchanged.
3. If the received pattern is the same as the pattern currently in the C/I register, the C/I register is unchanged and the latch is reset.

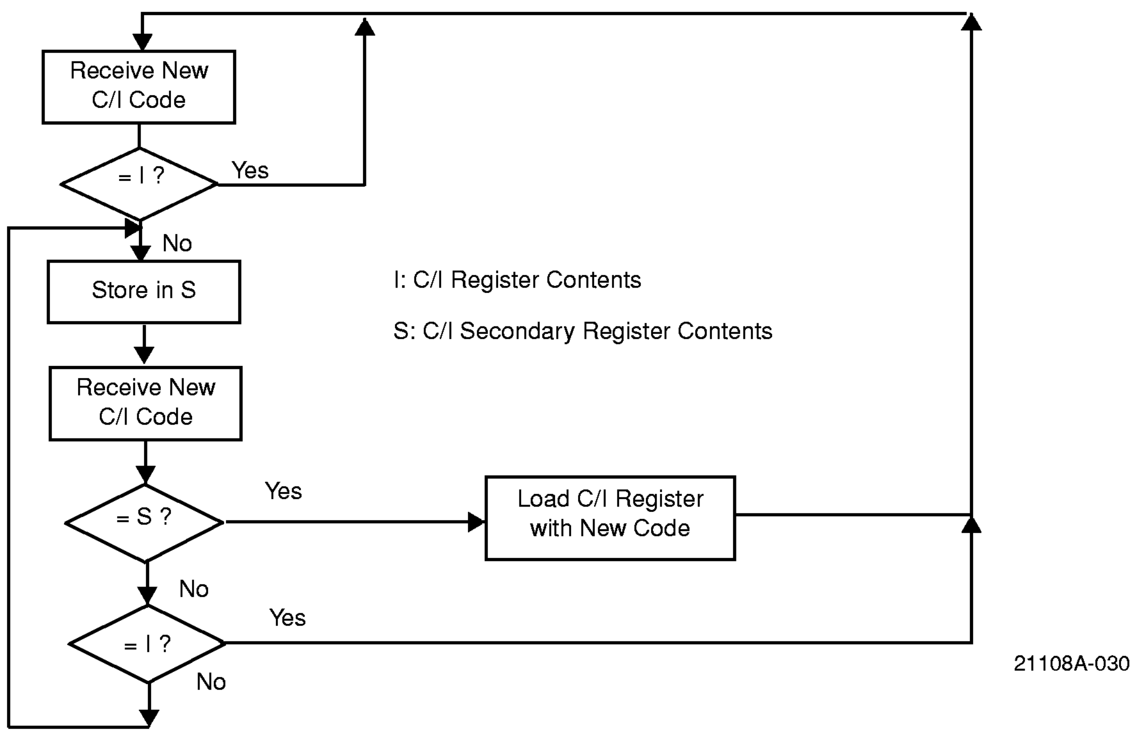


Figure 16. Security Procedure for C/I Downstream Bytes

Upstream C/I Channel

The SC channel, which includes the six C/I channel bits, is transmitted upstream every frame. The bit definitions for the upstream C/I channel are shown below. These bits are transmitted by the QSLAC device (Most significant bit first).

GCI Format

<------------------------ Upstream SC Octet ------------------>

MSB 7	6	5	4	3	2	1	LSB 0
$C3_1$	CDB_1	CDA_1	$C3_2$	CDB_2	CDA_2	MR	MX

|<----------------------- C/I FIELD ------------->|

Upstream Bit Definitions of the C/I field require the programmable I/O ports to be programmed as inputs. Otherwise, these bits follow the downstream C/I bits for $CD1_x$, $CD2_x$, and $C3_x$.

CDA_x: Debounced $CD1_x$ bit of channel x.

CDB_x: The filtered $CD2_x$ bit of channel x in non-E1 demultiplexed mode or the filtered $CD1B_x$ bit in the E1 demultiplexed mode.

$C3_x$–$C3_x$ of channel x.

The logic state of the CDA, CDB, and C3 device pins are read and transmitted in the upstream C/I channel only if they are programmed as an Input. In GCI mode, C4 and C5 are not available as upstream C/I data but can be obtained by reading the SLIC I/O register.

Monitor Channel

The Monitor Channel (see Figure 17) is used to read and write the QSLAC device's coefficient registers, to read the status of the device and the contents of the internal registers, and to provide supplementary signaling. Information is transferred on the Monitor Channel using the MR and MX bits of the SC channel, providing a secure method of data exchange between the upstream and downstream devices.

The Monitor byte is the third byte in the 4 byte GCI channel and is received every 125 μs over the DU or DD pins. A Monitor command consists of one address byte, one or more command bytes, and is followed by additional bytes of input data as required. The command may be followed by the QSLAC device sending data bytes upstream via the DU pin.

Monitor Channel Protocol

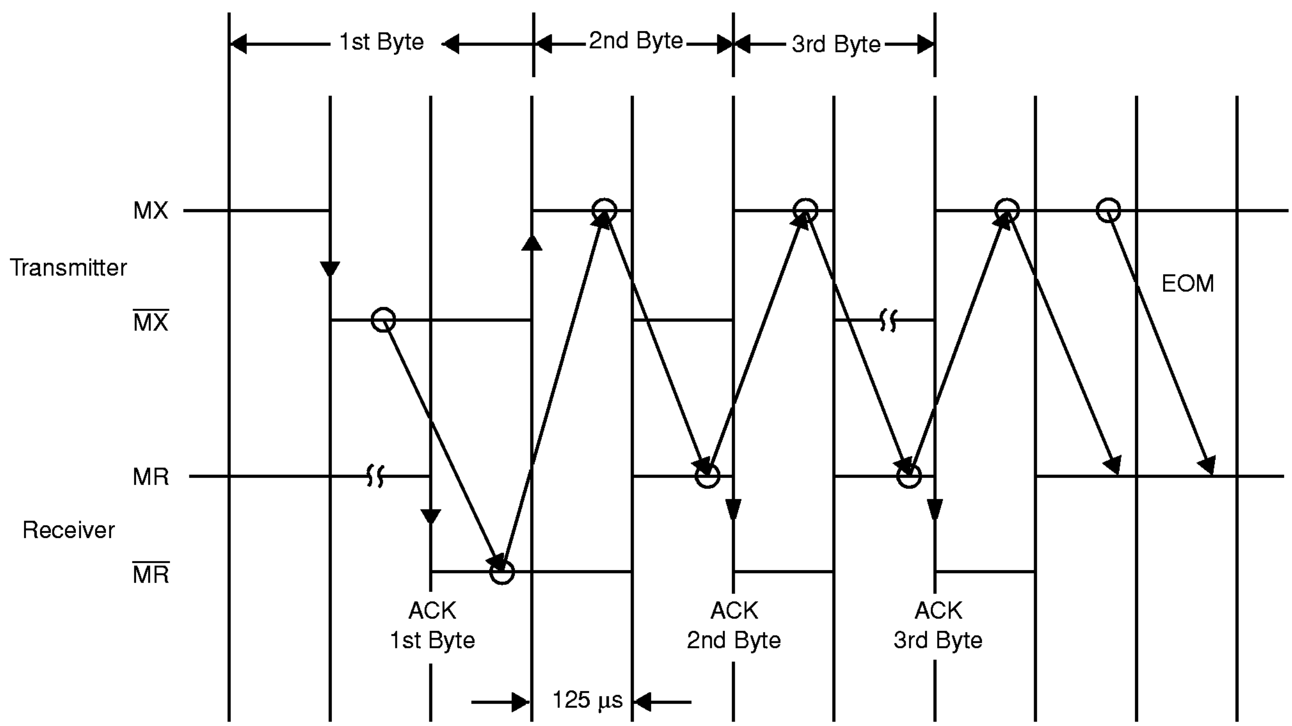
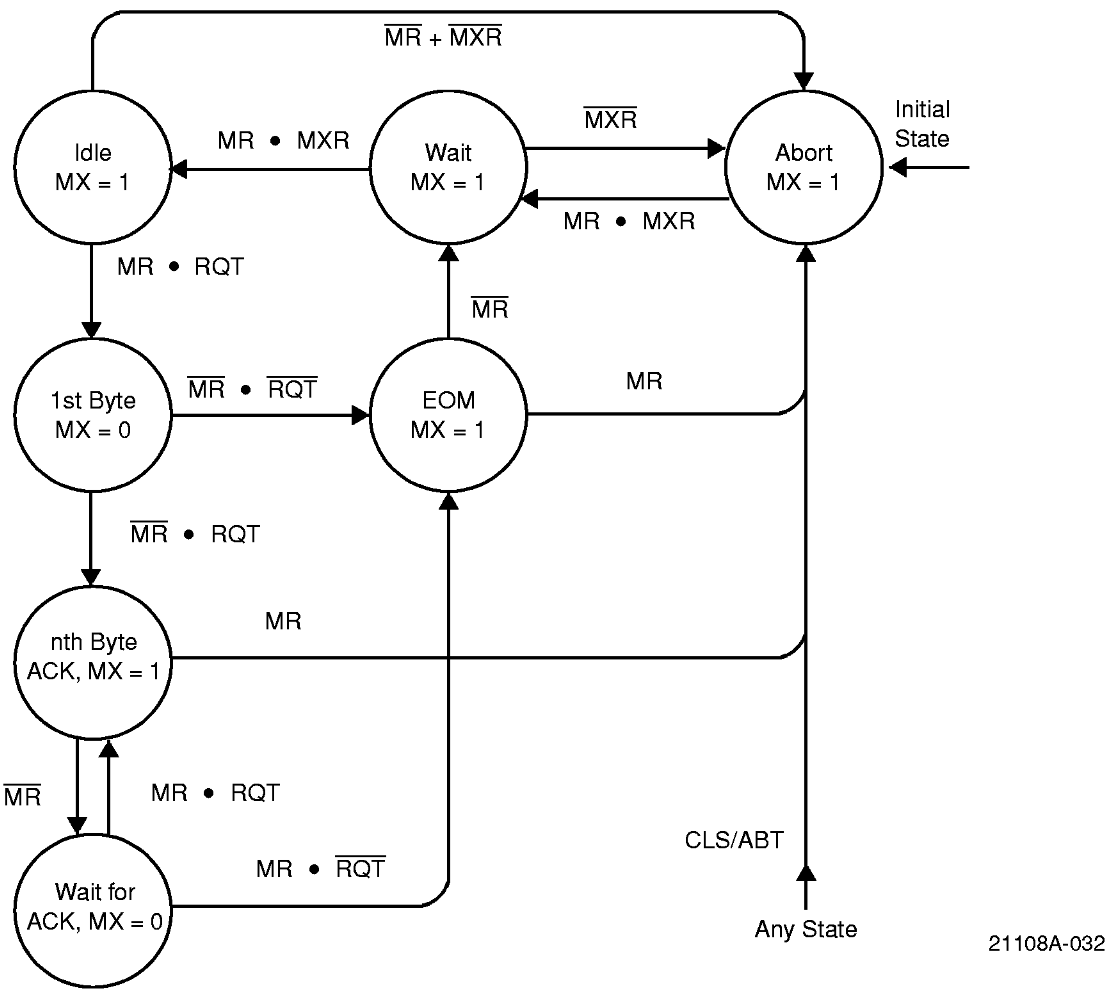


Figure 17. Maximum Speed Monitor Handshake Timing

21108A-031

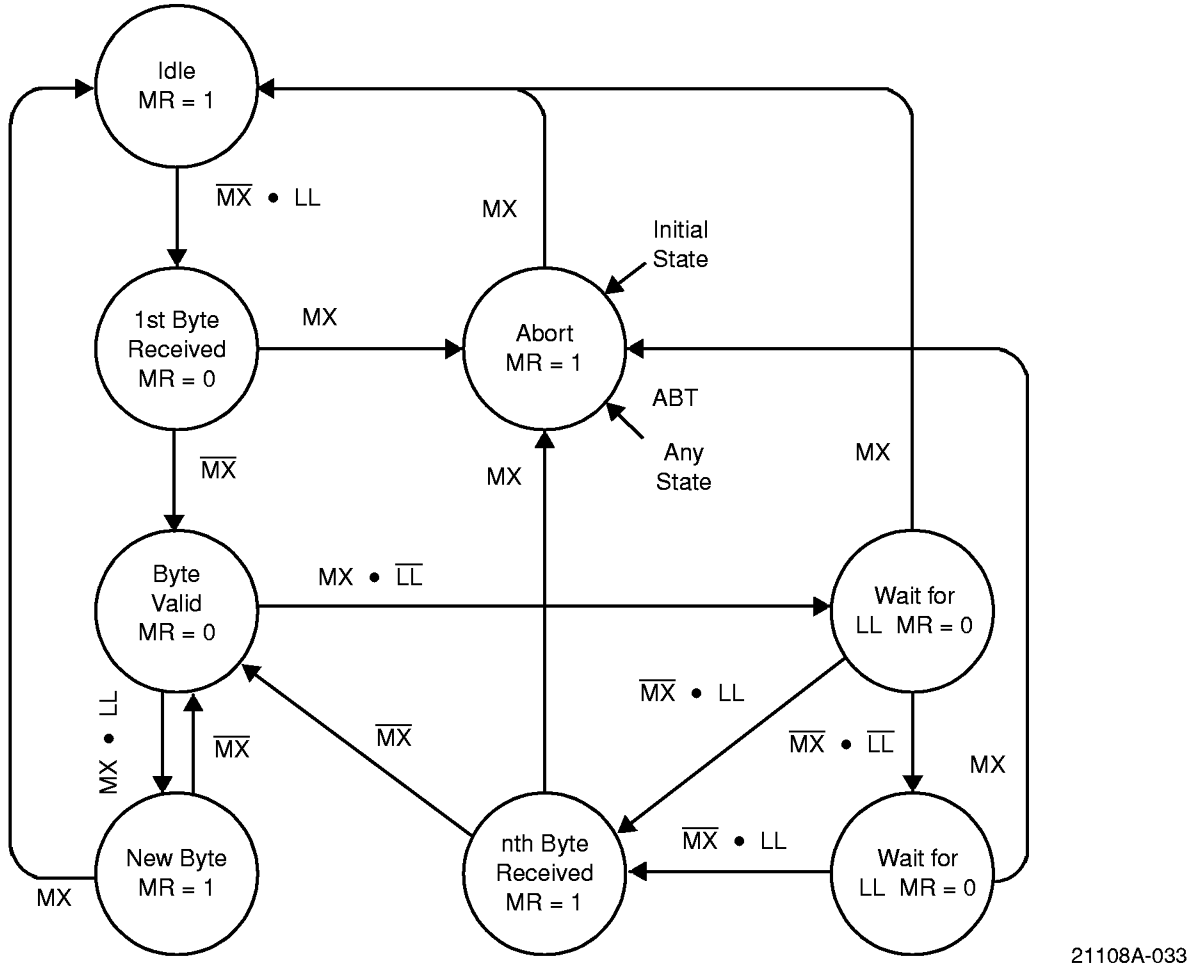
- An inactive (high) MX and MR pair bit for two or more consecutive frames shows an idle state on the monitor channel and the end of message (EOM).
- Figure 17 shows that transmission is initiated by the transition of the transmitter MX bit from the inactive to the active state. The transition coincides with the beginning of the first byte sent on the monitor channel. The receiver acknowledges the first byte by setting MR bit to active and keeping it active for at least one more frame.
- The same byte is sent continuously in each of the succeeding frames until either a new byte is transmitted, the end of message, or an abort.
- Any false MX or MR bit received by the receiver or transmitter leads to a request for abort or an abort, respectively.
- The same data must be received in two consecutive frames in order to be accepted by the receiver.
- A bus collision resolution mechanism is implemented in the transmitter. Before a device can send a monitor channel message, it must detect the idle condition (MR and MX both high).
- Any abort command leads to a reset of any pending commands in the QSLAC device. The device remains in the previous configuration and is ready to receive a new command.
- For maximum data transfer speed, the transmitter anticipates the falling edge of the receiver's acknowledgment, as shown in Figure 17.

Figure 18 and Figure 19 are state diagrams that define the operation of the monitor transmitter and receiver sections in the QSLAC device.



MR: MR bit received
MR: MR bit calculated and expected on the DU line
MXR: MX - bit sampled on the DU line
CLS: Collision within the monitor byte
RQT: Request for transmission from internal source
ABT: Abort request/indication

Figure 18. Monitor Transmitter State Diagram



MR: MR bit transmitted on DU line
MX: MX bit received on DD line
LL: Last look at monitor byte received
ABT: Abort indication from internal source

Figure 19. Monitor Receiver State Diagram

Programming with the Monitor Channel

The QSLAC device uses the monitor channel for the transfer of status or mode information to and from higher level processors.

The messages transmitted in the monitor channel have different data structures. The first byte of monitor channel data indicates the address of the device either sending or receiving the data.

All Monitor channel messages to and from the QSLAC device begin with the following address byte::

Bit	7	6	5	4	3	2	1	0
	1	0	0	A	B	0	0	C

A = 0; Channel 1 is the source (upstream) or destination (downstream)
A = 1; Channel 2 is the source (upstream) or destination (downstream)

B = 0; Data destination determined by A
B = 1; Both channels, 1 and 2, receive the data

C = 0; Address for channel identification command
C = 1; Address for all other commands

The monitor channel address byte is followed by a command byte. If the command byte specifies a write, then from 1 to 14 additional data bytes may follow (see Table 4). If the control byte specifies a read, additional data bytes may follow. The QSLAC device responds to the read command by sending up to 14 data bytes upstream containing the information requested by the upstream controller. Shown next is the generic byte transmission sequence over the GCI monitor channel.

Table 4. Generic Byte Transmission Sequence

GCI Monitor Channel	
Downstream	**Upstream**
ADDRESS Control byte, write Data byte 1* • Data byte m* ADDRESS Control byte, read	
	Data byte 1 • Data Byte n
m ≤ 14	n ≤ 14

Note:

** May or may not be present*

Channel Identification Command (CIC)

When the monitor channel address byte is 80H or 90H, a command of 00H is interpreted by the QSLAC device as a two byte Channel Identification Command (CIC).

The format for this command is shown next.:

Bit	7	6	5	4	3	2	1	0
Address Byte	1	0	0	B	0	0	0	0
Command Byte	0	0	0	0	0	0	0	0

B = 0 Channel 1 is the destination
B = 1 Channel 2 is the destination

Immediately after the last bit of the CIC command is received, the QSLAC device responds with the 2 byte channel ID code:

Bit	7	6	5	4	3	2	1	0
Byte 1	1	0	0	B	CONF	CONF	CONF	CONF
Byte 2	DT	DT	0	0	0	1	1	0

B = 0 Channel 1 is the source
B = 1 Channel 2 is the source

CONF Configuration value is always 0000 for the QSLAC device

DT Device Type value is always 1,0: Analog Transceiver. Other types are defined as:

Bit 7	Bit 6	Description
0	0	U Transceiver
0	1	S Transceiver
1	0	Analog Transceiver
1	1	Future

General Structure of Other Commands

When the QSLAC device has completed transmission of the channel ID information, it sends an EOM (MX = 1 for two successive frames) on the upstream C/I channel. The QSLAC device also expects an EOM to be received on the downstream C/I channel before any further message sequences are received.

When the monitor channel address byte is 81H, 89H, 91H, or 99H, the command byte is interpreted by the QSLAC device as either a Transfer Operation (TOP), Status Operation (SOP), or a Coefficient Operation (COP).

Bit	7	6	5	4	3	2	1	0
Address Byte	1	0	0	A	B	0	0	1

A = 0; Channel 1 is the destination
A = 1; Channel 2 is the destination

B = 0; Data destination determined by A
B = 1; Both channels 1 and 2 receive the data

Commands are sent to the QSLAC device to:

- Read the status of the system without changing its operation (Transfer Operation (TOP) command)
- Write/read the QSLAC operating state (Status Operation (SOP) command)
- Write/read filter coefficients (Coefficient Operation (COP) command).

SUMMARY OF MONITOR CHANNEL COMMANDS

GCI COMMANDS

Commands	C#	Hex	Binary	Description
Transfer Operation Commands (TOP)	01	00	00000000	Channel Identification Command (CIC); Requires unique address byte (80h, 90h)
	02	73	01110011	Read revision code number
Status Operation Commands (SOP)	01	00	00000000	Deactivate channel
	02	02	00000010	Software Reset
	03	04	00000100	Hardware Reset
	04	0E	00001110	Activate channel
	05	70/71	0111011W/R	Write/Read Operating Conditions (Configuration Register 1, CR1)
	06	46/47	0100011W/R	Write/Read Configuration Register 2, CR2
	07	60/61	0110011W/R	Write/Read Operating Functions (Configuration Register 3, CR3)
	08	54/55	0101010W/R	Write/Read SLIC I/O direction and Status Bits (Configuration Register 4, CR4)
	09	4A/4B	0100101W/R	Write/Read Operating Mode (Configuration Register 5, CR5)
	10	53	01010011	Read SLIC I/O Register
	11	C8/C9	1100100W/R	Write/Read Debounce Time Register
	12	E8/E9	1110100W/R	Write/Read Ground Key Filter Sampling Interval
	13	4D/4F	010011W/R1	Read Real-Time Data Register
	14	6C/6D	0110110W/R	Write/Read Interrupt Mask Register
Coefficient Operation Commands (COP)	01	50/51	0101000W/R	Write/Read AISN & Analog gains
	02	80/81	1000000W/R	Write/Read GX Filter Coefficients
	03	82/83	1000001W/R	Write/Read GR Filter Coefficients
	04	98/99	1001100W/R	Write/Read Z Filter Coefficients (FIR)
	05	86/87	1000011W/R	Write/Read B1 Filter Coefficients (FIR)
	06	88/89	1000000W/R	Write/Read X Filter Coefficients
	07	8A/8B	1000101W/R	Write/Read R Filter Coefficients
	08	96/97	1001011W/R	Write/Read B2 Filter Coefficients (IIR)
	09	9A/9B	1001101W/R	Write/Read Z Filter (IIR)

TOP (Transfer Operation) Command — GCI Command

The TOP (transfer operation) command is used when no status modification of the QSLAC device is required. The byte transmission sequence for a TOP command is shown in Table 5.

Table 5. Byte Transmission Sequence for TOP Command

GCI Monitor Channel	
Downstream	**Upstream**
ADDRESS Control byte, TOP read	
	TOP Byte 1 • • TOP Byte n n ≤ 14

TOP 2.Read Revision Code Number (RCN) — GCI Command

(73h)

Bit	7	6	5	4	3	2	1	0
Command	RCN7	RCN6	RCN5	RCN4	RCN3	RCN2	RCN1	RCN0

SOP (Status Operation) Command — GCI Command

To modify or evaluate the QSLAC device status, the contents of configuration registers CR1–CR5 and the SLIC I/O register can be transferred to and from the QSLAC device. This is done by a SOP (Status Operation) command. The general transmission sequence of the SOP command is shown in Table 5.

Table 6. General Transmission Sequence of SOP Command

GCI Monitor Channel	
Downstream	**Upstream**
ADDRESS Control byte, SOP write CR1 • • CRm SOP Read	
	CR1 • • CRn
m ≤ 7	n ≤ 8

SOP Control Byte Command Format

SOP 1.Deactivate Channel (Standby Mode) — GCI Command

(00h)

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0

In the Deactivated mode:

All of the programmed information is retained.
The upstream and downstream Monitor and SC channels remain active.
The B channel for a deactivated channel is idle, no data is received or transmitted.
The analog output (VOUT) is disabled and biased at 2.1 V.

The Channel Status ($\overline{CS}$) bit in the SLIC I/O and Status Bits register is set to 0.

SOP 2.Software Reset — GCI Command

(02h)

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	1	0

The action of this command is identical to that of the $\overline{RST}$ pin except it only operates on the address channel.

SOP 3.Hardware Reset — GCI Command

(04h)

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	1	0	0

The Hardware reset command is equivalent to pulling the $\overline{RST}$ pin on the device low. This command resets all four channels of the device. The action of the Hardware reset function is described in *Reset States* on page 31.

SOP 4.Activate Channel (Operational Mode) — GCI Command

(0Eh)

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	1	1	1	0

This command places the addressed channel of the device in the Active mode. No valid B-Channel data is transmitted until after the second FSC pulse is received following the execution of the Activate command.

SOP 5.Write/Read Operating Conditions — GCI Command

(70/71h)

Operating Conditions (Configuration Register 1, CR1)

Bit	7	6	5	4	3	2	1	0
	CTP	CRP	HPF	RG	ATI	ILB	FDL	TON

Configuration register CR1 enables or disables test features and controls feeding states. The reset value of CR1 = 04H

Cutoff Transmit Path

CTP = 0* Transmit path connected
CTP = 1 Transmit path disconnected

Cutoff Receive Path**

CRP = 0* Receive path connected
CRP = 1 Receive path cutoff

High Pass Filter

HPF = 0*	Transmit Highpass filter enabled
HPF = 1	Transmit Highpass filter disabled

Lower Receive Gain

RG = 0*	6 dB loss not inserted
RG = 1	6 dB loss inserted

Arm Transmit Interrupt

ATI = 0*	Transmit interrupt not armed
ATI = 1	Transmit interrupt armed

Interface Loop Back

ILB = 0*	Interface (GCI) loopback disabled
ILB = 1	Interface (GCI) loopback enabled

Full Digital Loopback

FDL = 0*	Full Digital Loopback disabled
FDL = 1	Full Digital Loopback enabled

1 kHz Receive Tone

TON = 0*	1 kHz receive tone off
TON = 1	1 kHz receive tone on

Power Up and Hardware Reset ($\overline{RST}$) Value = 00h

**B Filter is disabled during receive cutoff.

SOP 6.Write/Read Configuration Register 2, CF2 (46/47h) — GCI Command

Operating Conditions (Configuration Register 2, CR2)

Bit	7	6	5	4	3	2	1	0
	INTM	CHP	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Interrupt Mode

INTM = 0	TTL-compatible output
INTM = 1	Open drain output

Cutoff Transmit Path

CHP = 0*	Chopper Clock is 256 kHz (2048/8 kHz)
CHP = 1	Chopper Clock is 292.57 kHz (2048/7 kHz)

RSVD: Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

* Power Up and Hardware Reset ($\overline{RST}$) Value = 9Ah

SOP 7.Write/Read Operating Functions (60/61h) — GCI Command

Operating Functions (Configuration Register 3, CR3)

Bit	7	6	5	4	3	2	1	0
	RSVD	A/µ	EGR	EGX	EX	ER	EZ	EB

RSVD: Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

A-law/µ-law

A/µ = 0*	A-law coding
A/µ = 1	µ-law coding

GR filter

EGR = 0* GR filter default coefficients used:
EGR = 1 GR filter programmed coefficients used

GX filter

EGX = 0* GX filter default coefficients used
EGX = 1 GX filter programmed coefficients used

X filter

EX = 0* X filter default coefficients used
EX = 1 X filter programmed coefficients used

R filter

ER = 0* R filter default coefficients used
ER = 1 R filter programmed coefficients used

Z filter

EZ = 0* Z filter default coefficients used
EZ = 1 Z filter programmed coefficients used

B filter

EB = 0* B filter default coefficients used
EB = 1 B filter programmed coefficients used

*Power Up and Hardware Reset ($\overline{RST}$) Value = 00h

SOP 8.Write/Read SLIC I/O Direction and Status Bits **GCI Command**

(54/55h)

SLIC I/O Direction and Status Bits (Configuration Register 4, CR4)

Bit	7	6	5	4	3	2	1	0
	RSVD	CSTAT	CFAIL	IOD5	IOD4	IOD3	IOD2	IOD1

Pins CD1, CD2 and C3 through C5 are set to Input or Output modes individually. Pin C5 is not available on the Am79Q06 and Pins C3–C5 are not available on the Am79Q062 QSLAC devices.

RSVD: Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

Channel Status (Read only, write as 0)

CSTAT = 0 Channel is inactive (Standby mode)
CSTAT = 1 Channel is active

Clock Fail (Read only, write as 0)

CFAIL = 0 The internal clock is synchronized to frame sync
CFAIL = 1 The internal clock is not synchronized to frame sync

The CFAIL bit is universal for the QSLAC device and is independent of the channel addressed.

IOD1–IOD5

Programmable I/O direction control (CD1, CD2, C3, C4, C5 pins)
*0 = Pin is set as an input port
1 = Pin is set as an output port

*Power Up and Hardware Reset ($\overline{RST}$) Value = 00h

SOP 9.Write/Read Operating Mode **GCI Command**

(4A/4Bh)

Operating Mode (Configuration Register 5, CR5)

Bit	7	6	5	4	3	2	1	0
	RSVD		VMODE	LPM	RSVD			

RSVD: Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

VOUT Mode

VMODE = 0* VOUT = VREF through a resistor when channel is deactivated
VMODE = 1 VOUT high impedance when channel is deactivated.

Low Power Mode

LPM = 0* Low Power mode off
LPM = 1 Low Power mode on while all channels are inactive

Power Up and Hardware Reset ($\overline{RST}$) Value = 0Fh

SOP 10.Read SLIC Input/Output RegisterGCI Command

(53h)

Bit	7	6	5	4	3	2	1	0
	C7	C6	CD1B	C5	C4	C3	CD2	CD1

The logic states present on the CD1, CD2, C3, C4, and C5 pins of the QSLAC device for the addressed channel are read using this command, independent of their programmed direction (see SLIC I/O Direction Register). CD1B is the multiplexed CD1 bit and is valid only if the E1 multiplexing mode is enabled (EE = 1). If CD1, CD2, C3, C4, and C5 are programmed as inputs, then the logic states reported are determined by the external driving signal. In addition, CDA (the debounced state of CD1) and CDB (the debounced state of CD2, non-E1 multiplexed mode) or CD1B (E1 multiplexed mode), and the logic state present on the C3 pin of the device are sent directly upstream on the C/I bits of the upstream SC channel. If the CD1, CD2, C3, C4, and C5 pins are programmed as outputs then the logic states of these pins are controlled directly by the bits present in the C/I portion of the downstream SC channel and are not sent directly upstream in the SC channel. This command is normally used only to read the bit status via Command 53h. It is also possible although not recommended, if the CD1, CD2, and C3–C7 pins are programmed as outputs, to write the output state as Command 52h. The register is programmed upon execution of Command 52h but the status is overwritten when the next C/I portion of the downstream SC channel is received.

SOP 11.Write/Read Debounce Time Register* GCI Command (C8/C9h)

Bit	7	6	5	4	3	2	1	0
	EE1	E1P	DSH3	DSH2	DSH1	DSH0	RSVD	ECH

Enable E1

EE1 = 0* E1 Multiplexing is turned off
EE1 = 1 E1 Multiplexing is turned on

E1 Polarity

E1P = 0* E1 is a high-going pulse
E1P = 1 E1 is a low-going pulse

Debounce for Switchhook

DSH = 0–15 Debounce period in ms
DSH contains the debouncing time in ms of the CD1 data (usually switchhook) entering the CD1B bit of the read SLIC Input/Output register and the CD1B transmitted on the C/I bit of the upstream SC channel. The input data on CD1 must remain stable for the debounce time in order for the state of CD1B to change.

RSVD Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

Enable Chopper

ECH = 0* Chopper clock output is turned off.
ECH = 1 Chopper clock output is turned on.

Power Up and Hardware Reset ($\overline{RST}$) Value = 20h

Note: ** This command applies for all four channels of the device.*

SOP 12.Write/Read Ground Key Filter Sampling IntervalGCI Command (E8/E9h)

R/W = 0: Write

R/W = 1: Read

Bit	7	6	5	4	3	2	1	0
Command	1	1	1	0	1	0	0	R/W
I/O Data	RSVD	RSVD	RSVD	RSVD	GK3	GK2	GK1	GK0

Filter Ground Key

GK = 0–15 Filter sampling period in ms
GK contains the filter sampling time (in ms) of the CD1B data (usually Ground Key) or CD2 entering the upstream C/I channel described earlier.

RSVD Reserved for future use. Always write as 0, but 0 is not guaranteed when read.

Power Up and Hardware Reset ($\overline{RST}$) Value = 00h.

SOP 13.Read Real-Time Data Register **GCI Command**

(4D/4Fh)

C = 0: Do not clear interrupt

C = 1: Clear interrupt

This register writes/reads real-time data with or without closing the interrupt.

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	0	0	1	1	C	1
I/O Data	CDB4	CDA4	CDB3	CDA3	CDB2	CDA2	CDB1	CDA1

Real Time Data

CDA1	Debounced data bit 1 on Channel 1
CDB1	Data bit 2 or multiplexed data bit 1 on Channel 1
CDA2	Debounced data bit 1 on Channel 2
CDB2	Data bit 2 or multiplexed data bit 1 on Channel 2
CDB3	Debounced data bit 1 on Channel 3
CDA3	Data bit 1 on Channel 3
CDB4	Debounced data bit 1 on Channel 4
CDA4	Data bit 2 or multiplexed data bit 1 on Channel 4

This data is also available in the C/I field of the upstream SC channel.

SOP 14.Write/Read Interrupt Mask Register **GCI Command**

(6C/6Dh)

R/W = 0: Write

R/W = 1: Read

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	1	0	1	1	0	R/W
I/O Data	MCDB4	MCDA4	MCDB3	MCDA3	MCDB2	MCDA2	MCDB1	MCDA1

Mask CD Interrupt

MCDxy = 0	CDxy bit is NOT MASKED
MCDxy = 1*	CDxy bit is MASKED
x	Bit number (A or B)
y	Channel number (1 through 4)
Masked	A change does not cause the Interrupt Pin to go Low.

*Power Up and Hardware Reset ($\overline{RST}$) Value = FFh

COP (Coefficient Operation) Command GCI Command

The COP command writes or reads data related to filter coefficients. Filter coefficient data is used by the voice processors within the QSLAC device to configure the various filters in the voice channel. In this case, 1 to 14 coefficient bytes follow the command byte. The QSLAC device interprets the bytes as canonic signed digital (CSD) data and sets the coefficients accordingly.

The QSLAC device responds to the read coefficient command by sending up to 14 CSD bytes upstream. These bytes contain the coefficients requested by the upstream controller. For diagnostic purposes, various RAM locations containing data to which the QSLAC device has access can also be read back by this command.

The generic transmission sequence for the COP command is shown in Table 7.

Table 7. Generic Transmission Sequence for COP Command

Downstream	Upstream
ADDRESS Command byte, COP write Data1 • • $Data_m$ Control byte, COP read $m \leq 14$	 $Data_1$ • • $Data_n$ $n \leq 14$

The following tables show the format of the COP bytes that follow a downstream address byte.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
COMMAND	CMD	CMD	CMD	CMD	CMD	CMD	CMD	CMD
DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
•								
•								
DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA

The format in the upstream direction is the same except that the command byte is omitted.

Details of COP, CSD Data Commands

This section describes in detail each of the monitor channel COP commands. Each of the commands is shown along with the format of any additional data bytes that follow. For details of the filter coefficients of the form $C_{xy}m_{xy}$, please refer to the *Description of Coefficients* section.

COP 1.Write/Read AISN Coefficients and Analog Gains **GCI Command**

(50/51h)

R/W = 0: Write

R/W = 1: Read

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	0	0	W/R
Data	RSVD	AX	AR	AISN4	ASIN3	AISN2	AISN1	AISN0

RSVD: Reserved for future use. Reset to 0. Always write as 0, but 0 is not guaranteed when read.

Transmit analog gain

AX = 0*: 0 dB gain
AX = 1: 6.02 dB gain

Receive Analog Loss

AR = 0*: 0 dB loss
AR = 1: 6.02 dB loss

AISN coefficient

AISN = 0*–31 See below (Default value = 0)

The Analog Impedance Scaling Network (AISN) gain can be varied from –0.9375 to 0.9375 in multiples of 0.0625. The gain coefficient is decoded using the following equation:

$h_{AISN} = 0.0625\ ((AISN4 \bullet 2^4 + AISN3 \bullet 2^3 + AISN2 \bullet 2^2 + AISN1 \bullet 2^1 + AISN0 \bullet 2^0) - 16)$
where h_{AISN} is the gain of the AISN.

A value of AISN = '10000' turns on the Full Digital Loopback mode.

* Power Up and Hardware Reset ($\overline{RST}$) Value = 00h

COP 2.Write/Read GX Filter Coefficients **GCI Command**

(80/81h)

R/W = 0: Write

R/W = 1: Read

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Command	1	0	0	0	0	0	0	W/R
Coefficient Byte 1	C40	m40			C30	m30		
Coefficient Byte 2	C20	m20			C10	m10		

The coefficient for the GX filter is defined as:

$$H_{GX} = (1 + (C10 \bullet 2^{-m10}(1 + C20 \bullet 2^{-m20}(1 + C30 \bullet 2^{-m30}(1 + C40 \bullet 2^{-m40})))))$$

Power Up and Hardware Reset ($\overline{RST}$) Value = A9F0h, (H_{GX} = 1.995, or +6 dB)

COP 3.Write/Read GR Filter Coefficients **GCI Command**

(82/83h)

R/W = 0: Write

R/W = 1: Read

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Command	1	0	0	0	0	0	1	W/R
Coefficient Byte 1	C40	m40			C30	m30		
Coefficient Byte 2	C20	m20			C10	m10		

The coefficient for the GR filter is defined as:

$$H_{GR} = (C10 \bullet 2^{-m10}(1 + C20 \bullet 2^{-m20}(1 + C30 \bullet 2^{-m30}(1 + C40 \bullet 2^{-m40}))))$$

Power Up and Hardware Reset ($\overline{RST}$) Value = 23A1h, (H_{GR} = 0.35547, or –8.984 dB)

COP 4.Write/Read Z Filter FIR Coefficients **GCI Command**

(98/99h)

R/W = 1: Read

R/W = 0: Write

This command writes and reads only the FIR portion of the Z filter without affecting the IIR.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Command	1	0	0	1	1	0	0	R/W
I/O Data Byte 1	C40	m40			C30	m30		
I/O Data Byte 2	C20	m20			C10	m10		
I/O Data Byte 3	C41	m41			C31	m31		
I/O Data Byte 4	C21	m21			C11	m11		
I/O Data Byte 5	C42	m42			C32	m32		
I/O Data Byte 6	C22	m22			C12	m12		
I/O Data Byte 7	C43	m43			C33	m33		
I/O Data Byte 8	C23	m23			C13	m13		
I/O Data Byte 9	C44	m44			C34	m34		
I/O Data Byte 10	C24	m24			C14	m14		

The Z-transform equation for the Z filter is defined as:

$$H_z(z) = z_0 + z_1 \bullet z^{-1} + z_2 \bullet z^{-2} + z_3 \bullet z^{-3} + z_4 \bullet z^{-4} + \frac{z_5 \bullet z_6 \bullet z_7 \bullet z^{-1}}{1 - z_7 \bullet z^{-1}}$$

Sample rate = 32 kHz
For i = 0–5 and 7

$$z_i = C1i \bullet 2^{-m1i}\{1 + C2i \bullet 2^{-m2i}[1 + C3i \bullet 2^{-m3i}(1 + C4i \bullet 2^{-m4i})]\}$$

$$z_6 = C16 \bullet 2^{-m16}\{1 + C26 \bullet 2^{-m26}\}$$

Power Up and Hardware Reset ($\overline{RST}$) Values = 0190 0190 0190 0190 0190 0190 01 0190 (Hex)

($H_z(z) = 0$)

Note: *Z6 is used for IIR filter scaling only. Its value is typically greater than zero but less than or equal to one. The input to the IIR filter section is first increased by a gain of 1/Z6, improving dynamic range and avoiding truncation limitations through processing within this filter. The IIR filter output is then multiplied by Z6 to normalize the overall gain. Z5 is the actual IIR filter gain value defined by the programmed coefficients, but it also includes the initial 1/Z6 gain. The theoretical effective IIR gain, without the Z6 gain and normalization, is actually Z5/Z6.*

COP 5.Write/Read B1 Filter Coefficients 1–14 (86/87h)

GCI Command

R/W = 1: Read

R/W = 0: Write

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Command	1	0	0	1	1	0	0	R/W
I/O Data Byte 1	C32	m32			C22	m22		
I/O Data Byte 2	C12	m12			C33	m33		
I/O Data Byte 3	C23	m23			C13	m13		
I/O Data Byte 4	C34	m34			C24	m24		
I/O Data Byte 5	C14	m14			C35	m35		
I/O Data Byte 6	C25	m25			C15	m15		
I/O Data Byte 7	C36	m36			C26	m26		
I/O Data Byte 8	C16	m16			C37	m37		
I/O Data Byte 9	C27	m27			C17	m17		
I/O Data Byte 10	C38	m38			C28	m28		
I/O Data Byte 11	C18	m18			C39	m39		
I/O Data Byte 12	C29	m29			C19	m19		
I/O Data Byte 13	C310	m310			C210	m210		
I/O Data Byte 14	C110	m110			RSVD			

* ignored

The Z-transform equation for the B filter is defined as:

$$H_B(z) = B_2 \bullet z^{-2} + \ldots + B_9 \bullet z^{-9} + \frac{B_{10} \bullet z^{-10}}{1 - B_{11} \bullet z^{-1}}$$

Sample rate = 16 kHz

The coefficients for the FIR B section and the gain of the IIR B section are defined as:

For i = 2 to 10, $B_i = C1i \bullet 2^{-m1i}[1 + C2i \bullet 2^{-m2i}(1 + C3i \bullet 2^{-m3i})]$

The feedback coefficient of the IIR B section is defined as:

$$B_{11} = C111 \bullet 2^{-m111}\{1 + C211 \bullet 2^{-m211}[1 + C311 \bullet 2^{-m311}(1 + C411 \bullet 2^{-m411})]\}$$

Refer to Command COP8 for programming the B_{11} coefficients.

Power Up and Hardware Reset ($\overline{\text{RST}}$) Values = 36 AB B8 22 93 AB 2B 6C 46 2C 63 B6 9F 60 (Hex)

$$(H_B(z) = -0.254 \bullet z^{-2} - 0.891 \bullet z^{-3} - 0.656 \bullet z^{-4} - 0.090 \bullet z^{-5} + 0.013 \bullet z^{-6} + 0.017 \bullet z^{-7}$$
$$+ 0.014 \bullet z^{-8} + 0.013 \bullet z^{-9} + \frac{0.016 \bullet z^{-10}}{1 - 0.97656 \bullet z^{-1}})$$

RSVD: Reserved for future use. Reset to 0. Always write as 0, but 0 is not guaranteed when read.

COP 6.Write/Read X Filter Coefficients **GCI Command**

(88/89h)

R/W = 1: Read

R/W = 0: Write

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Command	1	0	0	0	1	0	0	W/R
Coefficient Byte 1	C40	m40			C30	m30		
Coefficient Byte 2	C20	m20			C10	m10		
Coefficient Byte 3	C41	m41			C31	m31		
Coefficient Byte 4	C21	m21			C11	m11		
Coefficient Byte 5	C42	m42			C32	m32		
Coefficient Byte 6	C22	m22			C12	m12		
Coefficient Byte 7	C43	m43			C33	m33		
Coefficient Byte 8	C23	m23			C13	m13		
Coefficient Byte 9	C44	m44			C34	m34		
Coefficient Byte 10	C24	m24			C14	m14		
Coefficient Byte 11	C45	m45			C35	m35		
Coefficient Byte 12	C25	m25			C15	m15		

The Z-transform equation for the X filter is defined as:

$$H_x(z) = X_0 + X_1 z^{-1} + X_2 z^{-2} + X_3 z^{-3} + X_4 z^{-4} + X_5 z^{-5}$$

Sample rate = 16 kHz

For i = 0 to 5, the coefficients for the X filter are defined as:

$$Xi = C1i \bullet 2^{-m1i}(1 + C2i \bullet 2^{-m2i}(1 + C3i \bullet 2^{-m3i}(1 + C4i \bullet 2^{-m4i})))$$

Power Up and Hardware Reset ($\overline{\text{RST}}$) Values = 0111 0190 0190 0190 0190 0190h

$H_x(z) = 1$

COP 7.Write/Read R Filter Coefficients GCI Command

(8A/8Bh)

R/W = 1: Read

R/W = 0: Write

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Command	1	0	0	0	1	0	1	W/R
Coefficient Byte 1	C46	m46			C36	m36		
Coefficient Byte 2	C26	m26			C16	m16		
Coefficient Byte 3	C40	m40			C30	m30		
Coefficient Byte 4	C20	m20			C10	m10		
Coefficient Byte 5	C41	m41			C31	m31		
Coefficient Byte 6	C21	m21			C11	m11		
Coefficient Byte 7	C42	m42			C32	m32		
Coefficient Byte 8	C22	m22			C12	m12		
Coefficient Byte 9	C43	m43			C33	m33		
Coefficient Byte 10	C23	C23			C13	m13		
Coefficient Byte 11	C44	m44			C34	m34		
Coefficient Byte 12	C24	m24			C14	m14		
Coefficient Byte 13	C45	m45			C35	m35		
Coefficient Byte 14	C25	m25			C15	m15		

$$HR = H_{IIR} \bullet H_{FIR}$$

The Z-transform equation for the IIR filter is defined as:

$$H_{IIR} = \frac{1 - z^{-1}}{1 - (R_6 \bullet z^{-1})}$$

Sample rate = 8 kHz

The coefficient for the IIR filter is defined as:

$$R_6 = C16 \bullet 2^{-m16}\{1 + C26 \bullet 2^{-m26}[1 + C36 \bullet 2^{-m36}(1 + C46 \bullet 2^{-m46})]\}$$

The Z-transform equation for the FIR filter is defined as:

$$H_{FIR}(z) = R_0 + R_1 z^{-1} + R_2 z^{-2} + R_3 z^{-3} + R_4 z^{-4} + R_5 z^{-5}$$

Sample rate = 16 kHz

For i = 0 to 5, the coefficients for the R2 filter are defined as:

$$R_i = C1i \bullet 2^{-m1i}\{1 + C2i \bullet 2^{-m2i}[1 + C3i \bullet 2^{-m3i}(1 + C4i \bullet 2^{-m4i})]\}$$

Power Up and Hardware Reset ($\overline{RST}$) Values = 2E01 0111 0190 0190 0190 0190 0190 (Hex)

(H_{FIR} (z) = 1, R_6 = 0.9902)

COP 8.Write/Read B2 Filter Coefficients 15–16 (96/97h) — GCI Command

R/W = 1: Read

R/W = 0: Write

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Command	1	0	0	1	0	1	1	W/R
Coefficient Byte 15	C411	m411			C311	m311		
Coefficient Byte 16	C211	m211			C111	m111		

This function is described in *Write B1 Filter Coefficients* on page 81.

Power Up and Hardware Reset ($\overline{RST}$) Value = AC01h

(B_{11} = 0.97656)

COP 9.Write/Read IIR Z Filter Coefficients (9A/9B) — GCI Command

R/W = 0: Write

R/W = 1: Read

This command writes and reads only the IIR portion of the Z filter without affecting the FIR.

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	1	1	0	1	R/W
I/O Data Byte 1	C45	m45			C35	m35		
I/O Data Byte 2	C25	m25			C15	m15		
I/O Data Byte 3	C26	m26			C16	m16		
I/O Data Byte 4	C47	m47			C37	m37		
I/O Data Byte 5	C27	m27			C17	m17		

The Z-transform equation for the Z filter is defined as:

$$H_z(z) = z_0 + z_1 \bullet z^{-1} + z_2 \bullet z^{-2} + z_3 \bullet z^{-3} + z_4 \bullet z^{-4} + \frac{z_5 \bullet z_6 \bullet z_7 \bullet z^{-1}}{1 - z_7 \bullet z^{-1}}$$

Sample rate = 32 kHz

For i = 0–5 and 7

$$z_i = C1i \bullet 2^{-m1i}\{1 + C2i \bullet 2^{-m2i}[1 + C3i \bullet 2^{-m3i}(1 + C4i \bullet 2^{-m4i})]\}$$

$$z_6 = C16 \bullet 2^{-m16}\{1 + C26 \bullet 2^{-m26}\}$$

Power Up and Hardware Reset ($\overline{RST}$) Values = 0190 0190 0190 0190 0190 0190 01 0190 (Hex)

($H_z(z) = 0$)

Note: *Z6 is used for IIR filter scaling only. Its value is typically greater than zero but less than or equal to one. The input to the IIR filter section is first increased by a gain of 1/Z6, improving dynamic range and avoiding truncation limitations through processing within this filter. The IIR filter output is then multiplied by Z6 to normalize the overall gain. Z5 is the actual IIR filter gain value defined by the programmed coefficients, but it also includes the initial 1/Z6 gain. The theoretical effective IIR gain, without the Z6 gain and normalization, is actually Z5/Z6.*

PROGRAMMABLE FILTERS

General Description of CSD Coefficients

The filter functions are performed by a series of multiplications and accumulations. A multiplication is accomplished by repeatedly shifting the multiplicand and summing the result with the previous value at that summation node. The method used in the QSLAC device is known as Canonic Signed Digit (CSD) multiplication and splits each coefficient into a series of CSD coefficients.

Each programmable FIR filter section has the following general transfer function:

$$HF(z) = h_0 + h_1 z^{-1} + h_2 z^{-2} + \ldots + h_n z^{-n} \qquad \text{Equation 1}$$

where the number of taps in the filter = n + 1.

The transfer function for the IIR part of Z and B filters is:

$$HI(z) = \frac{1}{1 - h_{(n+1)} z^{-1}} \qquad \text{Equation 2}$$

The transfer function of the IIR part of the R filter is:

$$HI(z) = \frac{1 - z^{-1}}{1 - h_{(n+1)} z^{-1}} \qquad \text{Equation 3}$$

The values of the user-defined coefficients (h_i) are assigned via the MPI. Each of the coefficients (h_i) is defined in the following general equation:

$$h_i = B_1 2^{-M_1} + B_2 2^{-M_2} + \ldots + B_N 2^{-M_N} \qquad \text{Equation 4}$$

where:

M_i = the number of shifts = $M_i \le M_i + 1$

B_i = sign = ±1

N = number of CSD coefficients

The value of h_i in Equation 4 represents a decimal number that is broken down into a sum of successive values of:

±1.0 multiplied by 2^{-0}, or 2^{-1}, or 2^{-2} … 2^{-7} …

or

±1.0 multiplied by 1, or 1/2, or 1/4 … 1/128 …

The limit on the negative powers of two is determined by the length of the registers in the ALU.

The coefficient h_i in Equation 4 can be considered to be a value made up of N binary 1s in a binary register where the left part represents whole numbers, the right part represents decimal fractions, and a decimal point separates them. The first binary 1 is shifted M_1 bits to the right of the decimal point; the second binary 1 is shifted M_2 bits to the right of the decimal point; the third binary 1 is shifted M_3 bits to the right of the decimal point, and so on.

When M_1 is 0, the resulting value is a binary 1 in front of the decimal point, that is, no shift. If M_2 is also 0, the result is another binary 1 in front of the decimal point, giving a total value of binary 10 in front of the decimal point (that is, a decimal value of 2.0). The value of N, therefore, determines the range of values the coefficient h_i can take (for example, if N = 3 the maximum and minimum values are ±3, and if N = 4 the values are between ±4).

Detailed Description of QSLAC Device Coefficients

The CSD coding scheme in the QSLAC device uses a value called mi, where m1 represents the distance shifted right of the decimal point for the first binary 1. m2 represents the distance shifted to the right of the previous binary 1, and m3 represents the number of shifts to the right of the second binary 1. Note that the range of values determined by N is unchanged. Equation 4 is now modified (in the case of N = 4) to:

$$h_i = B_1 2^{-M_1} + B_2 2^{-M_2} + B_3 2^{-M_3} + B_4 2^{-M_4} \qquad \text{Equation 5}$$

$$h_i = C1 \bullet 2^{-m1} + C1 \bullet C2 \bullet 2^{-(m1+m2)} + C1 \bullet C2 \bullet C3 \bullet 2^{-(m1+m2+m3)} + C1 \bullet C2 \bullet C3 \bullet C4 \bullet 2^{-(m1+m2+m3+m4)} \qquad \text{Equation 6}$$

$$h_i = C1 \bullet 2^{-m1}\{1 + C2 \bullet 2^{-m2}[1 + C3 \bullet 2^{-m3}(1 + C4 \bullet 2^{-m4})]\} \qquad \text{Equation 7}$$

where:

M_1 = m1	B_1 = C1
M_2 = m1 + m2	B_2 = C1 • C2
M_3 = m1 + m2 + m3	B_3 = C1 • C2 • C3
M_4 = m1 + m2 + m3 + m4	B_4 = C1 • C2 • C3 • C4

In the QSLAC device, a coefficient, h_i, consists of N CSD coefficients, each being made up of 4 bits and formatted as Cxy mxy, where Cxy is 1 bit (MSB) and mxy is 3 bits. Each CSD coefficient is broken down as follows:

Cxy is the sign bit (0 = positive, 1 = negative).

mxy is the 3-bit shift code. It is encoded as a binary number as follows:

000: 0 shifts

001: 1 shifts

010: 2 shifts

011: 3 shifts

100: 4 shifts

101: 5 shifts

110: 6 shifts

111: 7 shifts

y is the coefficient number (the i in h_i).

x is the position of this CSD coefficient within the h_i coefficient. The most significant binary 1 is represented by x = 1. The next most significant binary 1 is represented by x = 2, and so on.

Thus, C13 m13 represents the sign and the relative shift position for the first (most significant) binary 1 in the fourth (h_3) coefficient.

The number of CSD coefficients, N, is limited to four in the GR, GX, R, X, and Z filters; four in the IIR part of the B filter; three in the FIR part of the B filter; and two in the post-gain factor of the Z-IIR filter. Note also that the GX filter coefficient equation is slightly different from the other filters.

$$h_{iGX} = 1 + h_i \qquad \text{Equation 8}$$

Please refer to the Summary of MPI Commands section for complete details on programming the coefficients.

User Test Modes and Operating Conditions

The QSLAC device supports testing by providing test modes and special operating conditions as shown in Figure 12 (see Operating Conditions Register).

Cutoff Transmit Path (CTP): When CTP = 1, DX and $\overline{\text{TSC}}$ are High impedance and the transmit time slot does not exist. This mode takes precedence over the TSA Loopback (TLB) and Full Digital Loopback (FDL) modes.

Cutoff Receive Path (CRP): When CRP = 1, the receive signal is forced to 0 just ahead of the low pass filter (LPF) block. This mode also blocks Full Digital Loopback (FDL), the 1 kHz receive tone, and the B-filter path.

High Pass Filter Disable (HPF): When HPF = 1, all of the High pass and notch filters in the transmit path are disabled.

Lower Receive Gain (LRG): When LRG = 1, an extra 6.02 dB of loss is inserted into the receive path.

Arm Transmit Interrupt (ATI) and Read Transmit PCM Data (PCM/MPI mode only): The read transmit PCM data command, Command 47, can be used to read transmit PCM data through the microprocessor interface. If the ATI bit is set, an interrupt is generated whenever new transmit data appears in the channel and is cleared when the data is read. When combined with Tone Generation and Loopback modes, this allows the microprocessor to test channel integrity.

Interface Loopback (ILB): When ILB = 1, data from the receive/downstream path is looped back to the transmit/ Upstream path. Any other data in the transmit path is overwritten.

Full Digital Loopback (FDL): When FDL = 1, the VOUT output is turned off and the analog output voltage is routed to the input of the receive path, replacing the voltage from VIN. The AISN path is temporarily turned off. This test mode can also be entered by writing the code 10000 into the AISN register.

1 kHz Receive Tone (TON): When TON = 1, a 1 kHz digital mW is injected into the receive path, replacing any receive or downstream signal.

A-Law and µ-Law Companding

Table 8 and Table 9 show the companding definitions used for A-law and µ-law PCM encoding.

Table 8. A-Law: Positive Input Values

1	2	3	4	5	6	7	8
Segment Number	# Intervals x Interval Size	Value at Segment End Points	Decision Value Number *n*	Decision Value x_n (*See Note 1*)	Character Signal pre Inversion of Even Bits Bit No. 1 2 3 4 5 6 7 8	Quantized Value (at Decoder Output) y_n	Decoder Output Value No.
		4096	(128)	(4096)			
					1 1 1 1 1 1 1 1	4032	128
7	16 x 128		127	3968			
			⋮	⋮	*See Note 2*	⋮	⋮
			113	2176			
					1 1 1 1 0 0 0 0	2112	113
		2048	112	2048			
6	16 x 64		⋮	⋮	*See Note 2*	⋮	⋮
			97	1088			
					1 1 1 0 0 0 0 0	1056	97
		1024	96	1024			
5	16 x 32		⋮	⋮	*See Note 2*	⋮	⋮
			81	544			
					1 1 0 1 0 0 0 0	528	81
		512	80	512			
4	16 x 16		⋮	⋮	*See Note 2*	⋮	⋮
			65	272			
					1 1 0 0 0 0 0 0	264	65
		256	64	256			
3	16 x 8		⋮	⋮	*See Note 2*	⋮	⋮
			49	136			
					1 0 1 1 0 0 0 0	132	49
		128	48	128			
2	16 x 4		⋮	⋮	*See Note 2*	⋮	⋮
			33	68			
					1 0 1 0 0 0 0 0	66	33
		64	32	64			
1	32 x 2		⋮	⋮	*See Note 2*	⋮	⋮
			1	2			
↓					1 0 0 0 0 0 0 0	1	1
			0	0			

Notes:

1. *4096 normalized value units correspond to TMAX = 3.14 dBm0.*
2. *The character signals are obtained by inverting the even bits of the signals of column 6. Before this inversion, the character signal corresponding to positive input values between two successive decision values numbered n and n+1 (see column 4) is 128+n, expressed as a binary number.*
3. *The value at the decoder output is* $y_n = \frac{x_{n-1} + x_n}{2}$ *, for n = 1,...127, 128.*
4. x_{128} *is a virtual decision value.*
5. *Bit 1 is a 0 for negative input values.*

Table 9. μ-Law: Positive Input Values

1	2	3	4	5	6	7	8
Segment Number	# Intervals x Interval Size	Value at Segment End Points	Decision Value Number n	Decision Value x_n (*See Note 1*)	Character Signal pre Inversion of Even Bits Bit No. 1 2 3 4 5 6 7 8	Quantized Value (at Decoder Output) y_n	Decoder Output Value No.
		8159	(128)	(8159)			
8	16 x 256		127	7903	1 0 0 0 0 0 0 0	8031	127
			⋮	⋮	*See Note 2*	⋮	⋮
			113	4319			
		4063	112	4063	1 0 0 0 1 1 1 1	2112	112
7	16 x 128		⋮	⋮	*See Note 2*	⋮	⋮
			97	2143			
		2015	96	2015	1 0 0 1 1 1 1 1	1056	96
6	16 x 64		⋮	⋮	*See Note 2*	⋮	⋮
			81	1055			
		991	80	991	1 0 1 0 1 1 1 1	528	80
5	16 x 32		⋮	⋮	*See Note 2*	⋮	⋮
			65	511			
		479	64	479	1 0 1 1 1 1 1 1	264	64
4	16 x 16		⋮	⋮	*See Note 2*	⋮	⋮
			49	239			
		223	48	223	1 1 0 0 1 1 1 1	132	48
3	16 x 8		⋮	⋮	*See Note 2*	⋮	⋮
			33	103			
		95	32	95	1 1 0 1 1 1 1 1	99	32
2	16 x 4		⋮	⋮	*See Note 2*	⋮	⋮
			17	35			
		31	16	31	1 1 1 0 1 1 1 1	33	16
1	15 x 2		⋮	⋮	*See Note 2*	⋮	⋮
			2	3			
↓			1	1	1 1 1 1 1 1 1 0	2	1
	1 x 1				1 1 1 1 1 1 1 1	0	0
			0	0			

Notes:

1. *8159 normalized value units correspond to TMAX = 3.17 dBm0.*
2. *The character signal corresponding to positive input values between two successive decision values numbered n and n+1 (see column 4) is 255-n, expressed as a binary number.*
3. *The value at the decoder is* $y_0 = x_0 = 0$ *for n = 0, and* $y_n = \frac{x_{n+1} + x_n}{2}$ *, for n = 1, 2,...127.*
4. x_{128} *is a virtual decision value.*
5. *Bit 1 is a 0 for negative input values.*

APPLICATIONS

The QSLAC device performs a programmable codec/filter function for four telephone lines. It interfaces to the telephone lines through an AMD SLIC device or a transformer with external buffering. The QSLAC device provides latched digital I/O to control and monitor four SLICs and provides access to time-critical information, such as off/on-hook and ring trip, for all four channels via a single read operation or via the upstream C/I bits in the GCI SC channel. When various country or transmission requirements must be met, the QSLAC device enables a single SLIC design for multiple applications. The line characteristics (such as apparent impedance, attenuation, and hybrid balance) can be modified by programming each QSLAC device channel's coefficients to meet desired performance. The QSLAC device may require an external buffer to drive transformer SLICs.

In PCM/MPI mode, connection to a PCM back plane is implemented by means of a simple buffer chip. Several QSLAC devices can be tied together in one bus interfacing the back plane through a single buffer. An intelligent bus interface chip is not required because each QSLAC device provides its own buffer control (TSXA/B). The QSLAC device is controlled through the microprocessor interface, either by a microprocessor on the linecard or by a central processor.

In GCI mode, the QSLAC device decodes the S0 and S1 inputs and determines the DCL frequency, 2.048 MHz or 4.096 MHz automatically. The QSLAC device transmits and receives the GCI channel information in accordance with S0, S1 and DCL, synchronized by Frame Sync. (FSC). Up to four QSLAC devices can be bussed together forming one bidirectional 16 channel GCI bus. A simple inexpensive buffer should be used between the GCI bus and the backplane of the system.

Controlling the SLIC

The Am79Q061 QSLAC device has five TTL-compatible I/O pins (CD1, CD2, C3, C4 and C5) for each channel. The Am79Q031 QSLAC device has only CD1 and CD2 available. The outputs are programmed using MPI Command 19 or the downstream C/I bits in the GCI SC channel. The logic states are read back using MPI Command 21 or GCI Command SOP 10. In GCI mode CD1 (debounced), CD2, and C3 are also present on the upstream C/I bits in the GCI SC channel. In PCM/MPI mode, CD1 and CD2 for all four channels can be read back using MPI Command 16. The direction of the I/O pins (input or output) is specified by programming the SLIC I/O direction register (MPI Commands 22, GCI Command SOP 9).

Default Filter Coefficients

The default filter coefficients were calculated assuming an Am7920 SLIC with 50 Ω protection resistors, a 178 kΩ transversal impedance (Z_T), and a 90.5 kΩ receive impedance (Z_{RX}). This SLIC has a transmit gain of 0.5 (G_{TX}) and a current gain of 500 (K1). The transmit relative level was set to +0.28 dBr, and the receive relative level was set to –4.39 dBr. The equalization filters (X and R) were not optimized. The balance filter was designed to give acceptable balance into a variety of impedances. The nominal input impedance was set to 815 Ω. If the SLIC circuit differs significantly from this design, the default filters cannot be used and must be replaced by programmed coefficients.

Calculating Coefficients with WinSLAC Software

WinSLAC software is a program that models the QSLAC device, the line conditions, the SLIC, and the linecard components to obtain the coefficients of the programmable filters of the QSLAC device and some of the transmission performance plots.

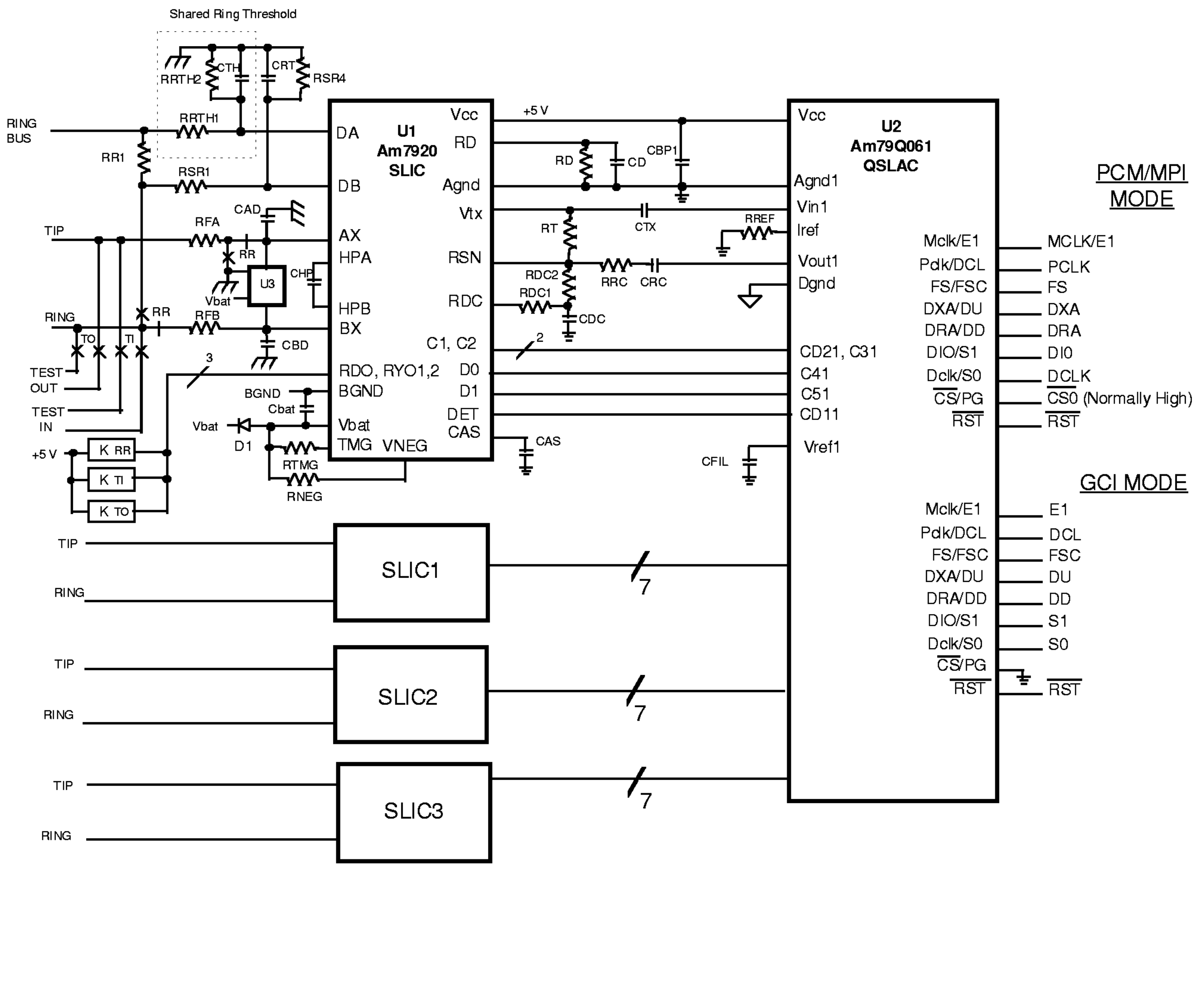
The following parameters relating to the desired line conditions and the components/circuits used in the linecard are to be provided as input to the program:

1. Line impedance or the balance impedance of the line is specified by the local PTT.
2. Desired two-wire impedance that is to appear at the linecard terminals of the exchange.
3. Tabular data for templates describing the frequency response and attenuation distortion of the design.
4. Relative analog signal levels for both the transmit and receive two-wire signals.
5. Component values and SLIC device selection for the analog portion of the line circuits.
6. Two-wire return loss template is usually specified by the local PTT.
7. Four-wire return loss template is usually specified by the local PTT.

The output from the WinSLAC software includes the coefficients of the GR, GX, Z, R, X, and B filters as well as transmission performance plots of two-wire return loss, receive and transmit path frequency responses, and four-wire return loss.

The software supports the use of the AMD SLICs or allows entry of a SPICE netlist describing the behavior of any type of SLIC circuit.

Am7920 SLIC/QSLAC APPLICATION CIRCUIT



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REVISION SUMMARY

Revision B to C

- “Frame sync” information was added to the first paragraph on page 36.