

*Advance Information*

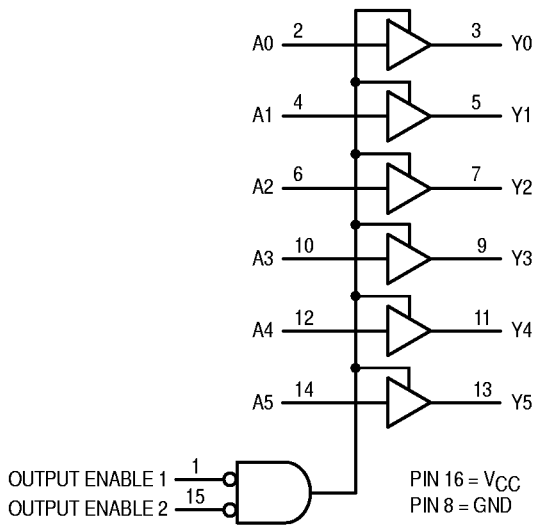
**Hex 3-State Noninverting Buffer with Common Enables**  
**High-Performance Silicon-Gate CMOS**

The MC74HC365A is identical in pinout to the LS365. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

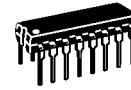
This device is a high-speed hex buffer with 3-state outputs and two common active-low Output Enables. When either of the enables is high, the buffer outputs are placed into high-impedance states. The HC365A has noninverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 90 FETs or 22.5 Equivalent Gates

**LOGIC DIAGRAM**



**MC74HC365A**



**N SUFFIX**  
PLASTIC PACKAGE  
16-LEAD  
CASE 648-08



**D SUFFIX**  
SOIC PACKAGE  
16-LEAD  
CASE 751B-05

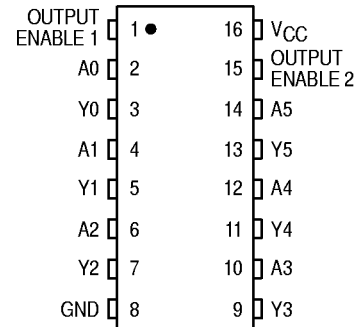


**DT SUFFIX**  
TSSOP PACKAGE  
16-LEAD  
CASE 948F-01

**ORDERING INFORMATION**

MC74HCXXXAN	Plastic
MC74HCXXXAD	SOIC
MC74HCXXXADT	TSSOP

**PIN ASSIGNMENT**



**FUNCTION TABLE**

Inputs			Output
Enable 1	Enable 2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

X = don't care  
Z = high impedance

This document contains information on a new product. Specifications and information herein are subject to change without notice.



**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	- 0.5 to V <sub>CC</sub> + 0.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	- 0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	± 20	mA
I <sub>out</sub>	DC Output Current, per Pin	± 25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	- 55	+ 125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.50	0.50	0.50	V
			3.0	0.90	0.90	0.90	
			4.5	1.35	1.35	1.35	
			6.0	1.80	1.80	1.80	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤ 3.6 mA  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	3.0	2.48	2.34	2.20	
			4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	

**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IL</sub>  I <sub>out</sub>   ≤ 3.6 mA  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	3.0	0.26	0.33	0.40	
			4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	± 0.5	± 5.0	± 10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**AC ELECTRICAL CHARACTERISTICS** (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0	120	150	180	ns
		3.0	60	75	90	
		4.5	24	30	36	
		6.0	20	26	31	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0	220	275	330	ns
		3.0	110	140	170	
		4.5	44	55	66	
		6.0	37	47	56	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0	220	275	330	ns
		3.0	110	140	170	
		4.5	44	55	66	
		6.0	37	47	56	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	60	75	90	ns
		3.0	22	28	34	
		4.5	12	15	18	
		6.0	10	13	15	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

## NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).
- Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

C <sub>PD</sub>	Power Dissipation Capacitance (Per Buffer)*	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	
			35

\* Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ . For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**SWITCHING WAVEFORMS**

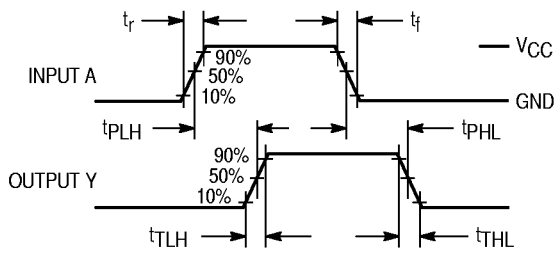


Figure 1.

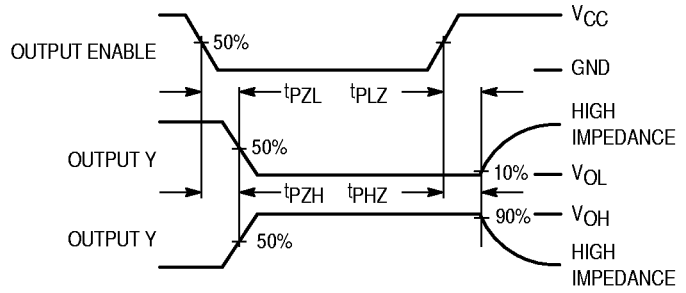
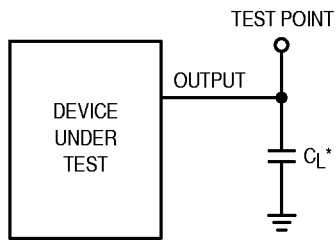


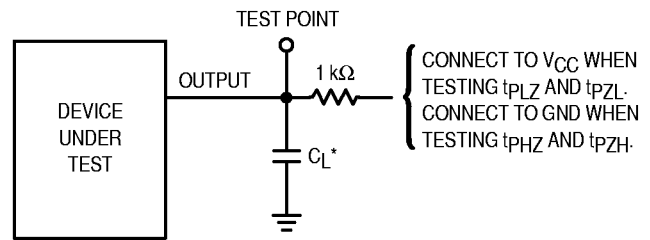
Figure 2.

**TEST CIRCUITS**



\* Includes all probe and jig capacitance

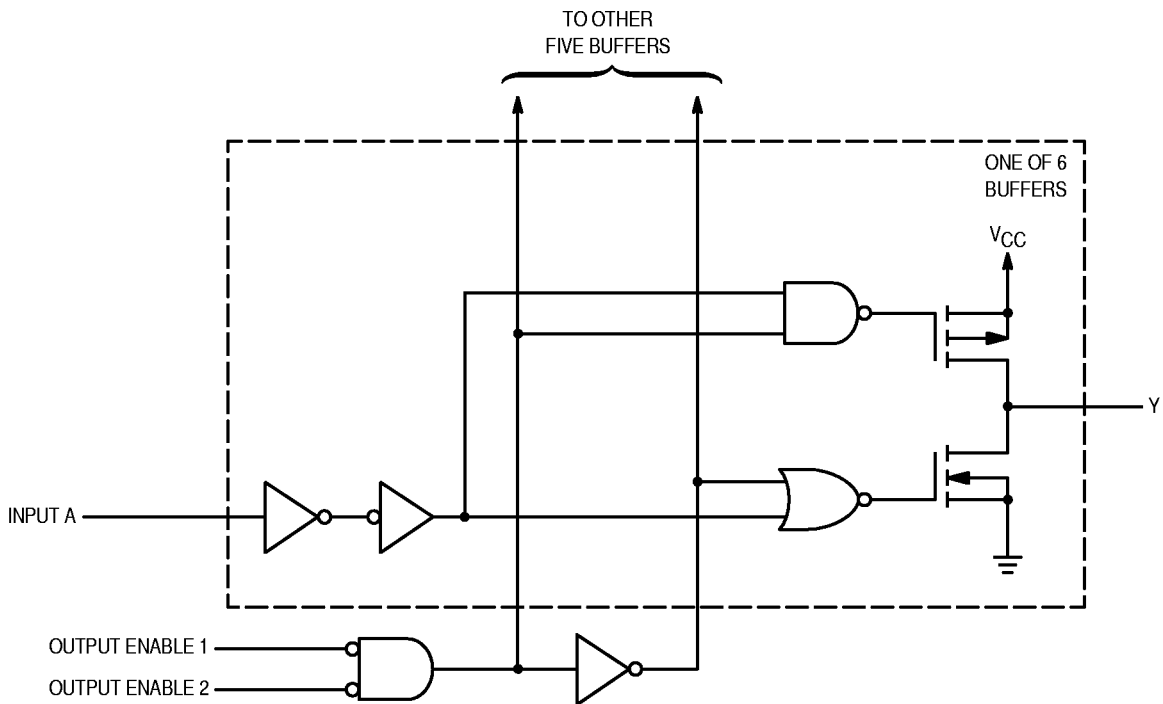
Figure 3.



\* Includes all probe and jig capacitance

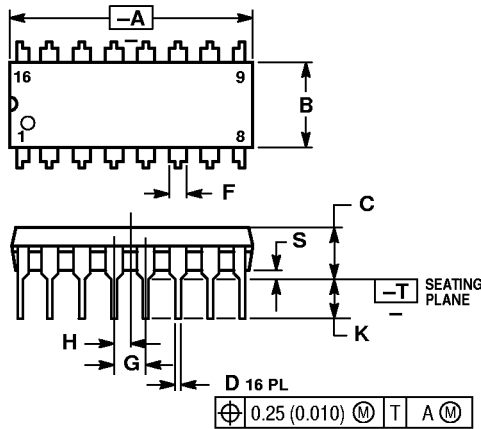
Figure 4.

**LOGIC DETAIL**



OUTLINE DIMENSIONS

**N SUFFIX**  
**PLASTIC PACKAGE**  
**CASE 648-08**  
**ISSUE R**

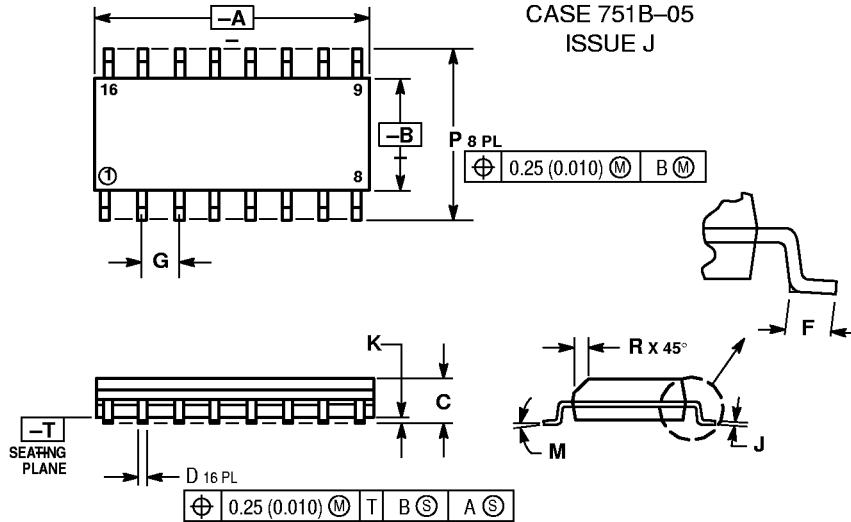


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

**D SUFFIX**  
**PLASTIC SOIC PACKAGE**  
**CASE 751B-05**  
**ISSUE J**



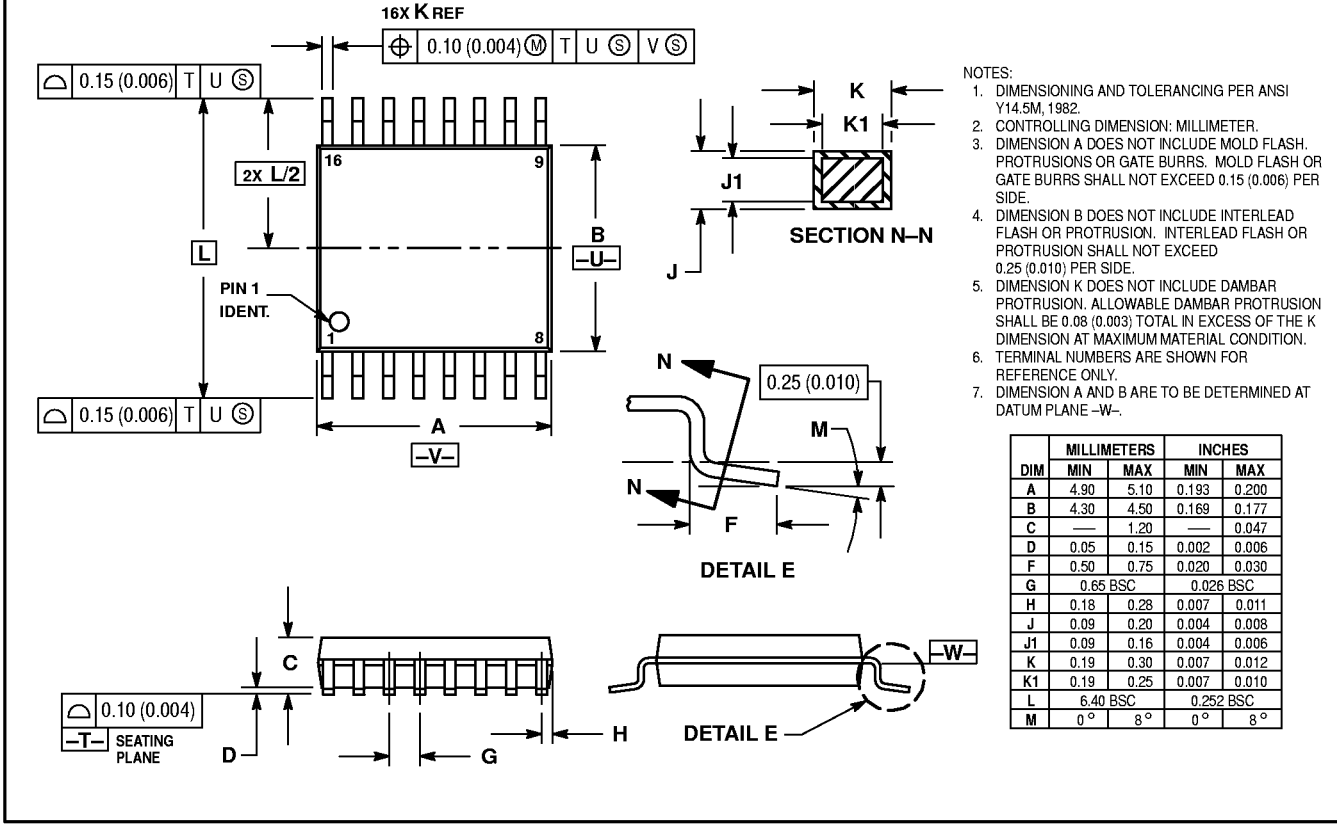
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

OUTLINE DIMENSIONS

DT SUFFIX  
 PLASTIC TSSOP PACKAGE  
 CASE 948F-01  
 ISSUE O



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