002645

SL-5-4016
SL-7-4016

J-2645

Quad 16-Bit Static Shift Registers

FEATURES

- TTL/DTL Compatible Clock Input
- TTL/DTL Compatible Data—
  No external interfacing components required on data inputs or outputs.
- DC-2MHz Operation
- Full Static Operation—
  Data is stored independently of the clock logic level.
- Temperature Range:
  0°C to +70°C
- Zener Protected Inputs
- Glass Passivation Protection

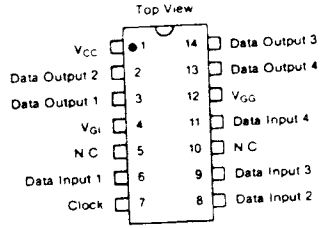
DESCRIPTION

The SL-5-4016 and SL-7-4016 are quad 16-bit static shift registers with clock and data inputs and outputs that interface directly with TTL/DTL logic arrays without the use of any special interface components. This device contains four independent common clock 16-bit DC to 2MHz shift registers constructed on a single monolithic chip utilizing MTNS P-Channel enhancement mode transistors. Each shift register bit is implemented with a cross coupled flip-flop, so that data is stored indefinitely regardles of the logic level of the clock. A single phase clock input is provided for all registers. Data on the input is sampled while the clock is at a "0" level and the register shifts on a "0" to "1" transition.

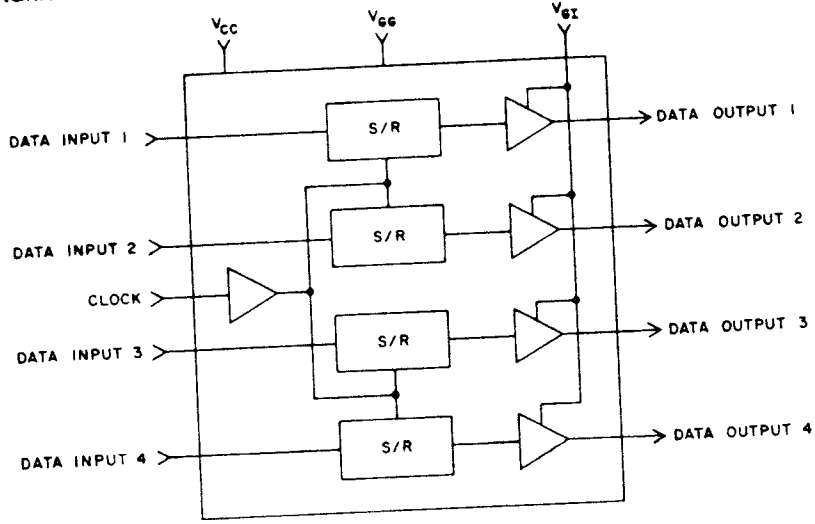
*Available only in Europe (14 Lead Plastic DIP)

PIN CONFIGURATION

14 LEAD DUAL IN-LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GG} and V_{GL} with respect to V_{CC} ..... -20V to +0.3V
Clock and Data Inputs with respect to V_{CC} ..... -15V to +0.3V
Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

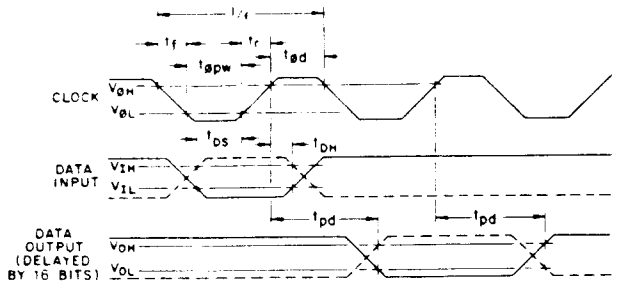
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±0.5 Volts (V_{CC} is the substrate voltage)
V_{GG} = +12 Volts ±1 Volt
V_{GL} = GND
Operating Temperature (T_A) = 0°C to +70°C
One TTL load (C_L total = 10 pF)

Characteristic	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Input						
Logic 1 Level	$V_{\phi H}$	V_{CC}-1.5	—	—	Volts	
Logic 0 Level	$V_{\phi L}$	—	—	+0.8	Volts	
Leakage	$I_{\phi L}$	—	—	10	µA	$V_{\phi} = V_{CC}$ -10V
Data Input						
Logic 1 Level	V_{IH}	V_{CC}-1.5	—	—	Volts	
Logic 0 Level	V_{IL}	—	—	+0.8	Volts	
Leakage	I_{IL}	—	—	10	µA	$V_{IN} = V_{CC}$ -10V
Data Output						
Logic 1 Level	V_{OH}	V_{CC}-1.0	—	—	Volts	I_{OH} = 100µA
Logic 0 Level	V_{OL}	—	—	+0.4	Volts	I_{OL} = 1.6mA
Power	—	—	450	—	mW	
AC CHARACTERISTICS						
Clock Input						
Frequency	f	DC	—	2.0	MHz	
Pulse Width	$t_{\phi PW}$	200	—	—	ns	$t_{\phi PW} = t_{\phi D}$
Pulse Delay	$t_{\phi D}$	450	—	—	ns	$t_{\phi D} \geq 1$ µsec
Rise and Fall Times	t_r, t_f	—	—	1000	ns	
Capacitance	C_ϕ	—	15	—	pF	1MHz, T_A = +25°C
Data Input						
Set Up Time	t_{DS}	150	—	—	ns	
Hold Time	t_{DH}	25	0	—	ns	
Capacitance	C_{IN}	—	5	—	pF	1MHz, T_A = +25°C
Data Output						
Propagation Delay	t_{pd}	—	250	—	ns	

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAM



MEMORY