

SN54AS885, SN74AS885 8-BIT MAGNITUDE COMPARATORS

SDAS236A – DECEMBER 1982 – REVISED JANUARY 1995

- Latchable P-Input Ports With Power-Up Clear
- Choice of Logical or Arithmetic (Two's Complement) Comparison
- Data and PLE Inputs Utilize pnp Input Transistors to Reduce dc Loading Effects
- Approximately 35% Improvement in ac Performance Over Schottky TTL While Performing More Functions
- Cascadable to n Bits While Maintaining High Performance
- 10% Less Power Than STTL for an 8-Bit Comparison
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

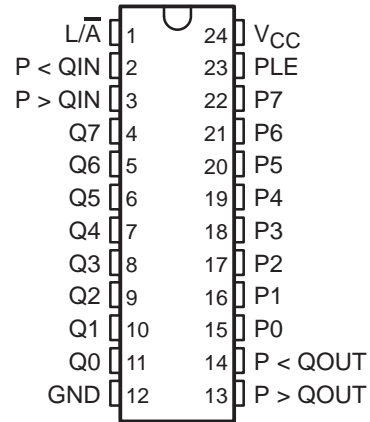
description

These advanced Schottky devices are capable of performing high-speed arithmetic or logic comparisons on two 8-bit binary or two's complement words. Two fully decoded decisions about words P and Q are externally available at two outputs. These devices are fully expandable to any number of bits without external gates. To compare words of longer lengths, the P > QOUT and P < QOUT outputs of a stage handling less significant bits can be connected to the P > QIN and P < QIN inputs of the next stage handling more significant bits. The cascading paths are implemented with only a two-gate-level delay to reduce overall comparison times for long words. Two alternative methods of cascading are shown in *application information*.

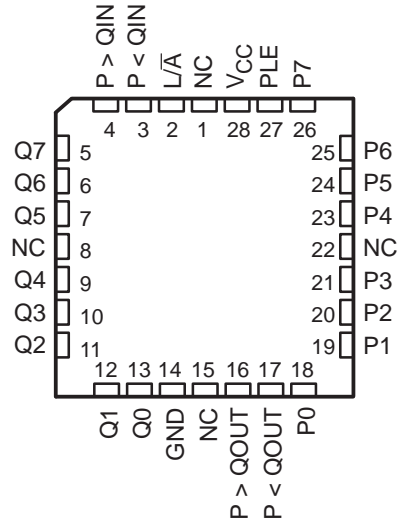
The latch is transparent when P latch-enable (PLE) input is high; the P-input port is latched when PLE is low. This provides the designer with temporary storage for the P-data word. The enable circuitry is implemented with minimal delay times to enhance performance when cascaded for longer words. The PLE, P, and Q data inputs utilize pnp input transistors to reduce the low-level current input requirement to typically -0.25 mA, which minimizes dc loading effects.

The SN54AS885 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74AS885 is characterized for operation from 0°C to 70°C.

SN54AS885 . . . JT PACKAGE
SN74AS885 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS885 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

SN54AS885, SN74AS885 8-BIT MAGNITUDE COMPARATORS

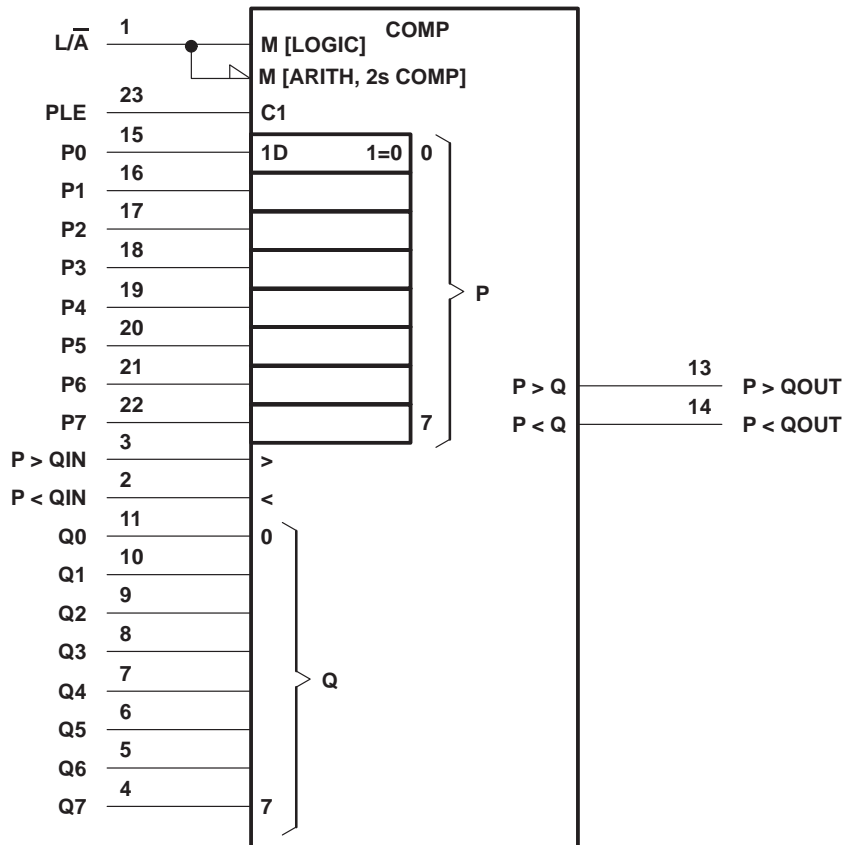
SDAS236A – DECEMBER 1982 – REVISED JANUARY 1995

FUNCTION TABLE

COMPARISON	INPUTS				OUTPUTS	
	$\overline{L/A}$	DATA P0–P7, Q0–Q7	P > QIN	P < QIN	P > QOUT	P < QOUT
Logical	H	P > Q	X	X	H	L
Logical	H	P < Q	X	X	L	H
Logical†	H	P = Q	H or L	H or L	H or L	H or L
Arithmetic	L	P AG Q	X	X	H	L
Arithmetic	L	Q AG P	X	X	L	H
Arithmetic†	L	P = Q	H or L	H or L	H or L	H or L

† In these cases, P > QOUT follows P > QIN and P < QOUT follows P < QIN.
AG = arithmetically greater than

logic symbol‡

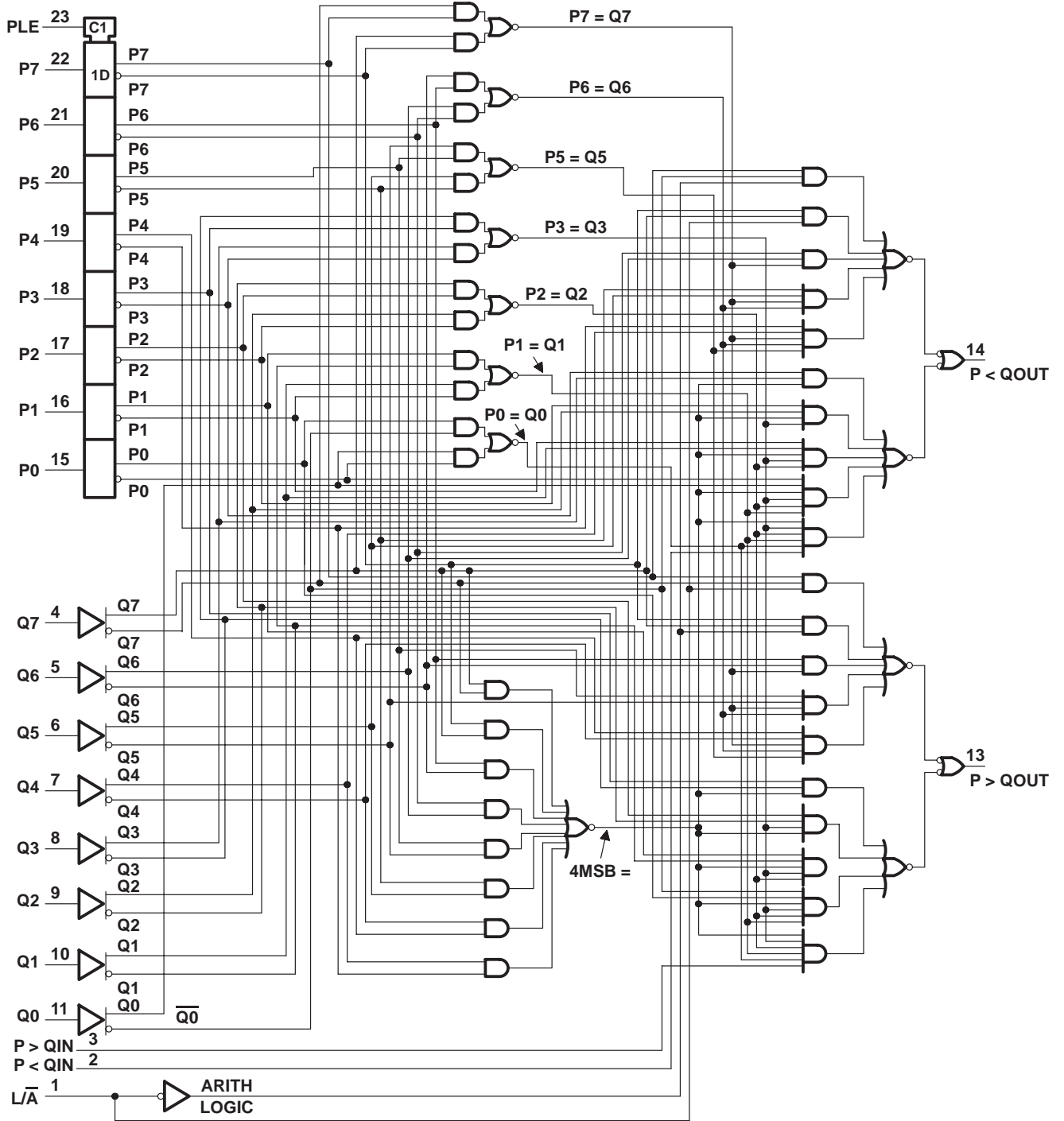


‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

SN54AS885, SN74AS885 8-BIT MAGNITUDE COMPARATORS

SDAS236A – DECEMBER 1982 – REVISED JANUARY 1995

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

SN54AS885, SN74AS885 8-BIT MAGNITUDE COMPARATORS

SDAS236A – DECEMBER 1982 – REVISED JANUARY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Operating free-air temperature range, T_A : SN54AS885	-55°C to 125°C
SN74AS885	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54AS885			SN74AS885			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-2			-2	mA
I_{OL}	Low-level output current			20			20	mA
t_{su}^*	Setup time, data before PLE↓	2			2			ns
t_h^*	Hold time, data after PLE↓	4.5			4			ns
T_A	Operating free-air temperature	-55		125	0		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS885			SN74AS885			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = 4.5 V$, $I_I = -18 mA$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5 V$ to $5.5 V$, $I_{OH} = -2 mA$	$V_{CC} - 2$			$V_{CC} - 2$			V
V_{OL}	$V_{CC} = 4.5 V$, $I_{OL} = 20 mA$	0.35	0.5		0.35	0.5		V
I_I	$V_{CC} = 5.5 V$, $V_I = 7 V$		0.1			0.1		mA
I_{IH}	L/\bar{A}		40			40		μA
	Others		20			20		
I_{IL}	L/\bar{A}		-4			-4		mA
	$P > QIN, P < QIN$		-2			-2		
	P, Q, PLE		-1			-1		
I_{O}^{\S}	$V_{CC} = 5.5 V$, $V_O = 2.25 V$	-20		-112	-20		-112	mA
I_{CC}	$V_{CC} = 5.5 V$, See Note 1		130	210		130	210	mA

‡ All typical values are at $V_{CC} = 5 V$, $T_A = 25^\circ C$.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

NOTE 1: I_{CC} is measured with all inputs high except L/\bar{A} , which is low.



switching characteristics (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX						UNIT
			SN54AS885			SN74AS885			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t _{PLH}	L/ \bar{A}	P < QOUT, P > QOUT	2	8.5	14	1	8.5	13	ns
t _{PHL}			2	7.5	14	1	7.5	13	
t _{PLH}	P < QIN, P > QIN	P < QOUT, P > QOUT	2	5	10	1	5	8	ns
t _{PHL}			2	5.5	10	1	5.5	8	
t _{PLH}	Any P or Q data input	P < QOUT, P > QOUT	2	13.5	21	1	13.5	17.5	ns
t _{PHL}			2	10	17	1	10	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

APPLICATION INFORMATION

The 'AS885 can be cascaded to compare words longer than eight bits. Figure 1 shows the comparison of two 32-bit words; however, the design is expandable to n bits. Figure 1 shows the optimum cascading arrangement for comparing words of 32 bits or greater. Typical delay times shown are at V_{CC} = 5 V, T_A = 25°C and use the standard advanced Schottky load of R_L = 500 Ω, C_L = 50 pF.

Figure 2 shows the fastest cascading arrangement for comparing 16-bit or 24-bit words. Typical delay times shown are at V_{CC} = 5 V, T_A = 25°C and use the standard advanced Schottky load of R_L = 500 Ω, C_L = 50 pF.

SN54AS885, SN74AS885 8-BIT MAGNITUDE COMPARATORS

SDAS236A – DECEMBER 1982 – REVISED JANUARY 1995

APPLICATION INFORMATION

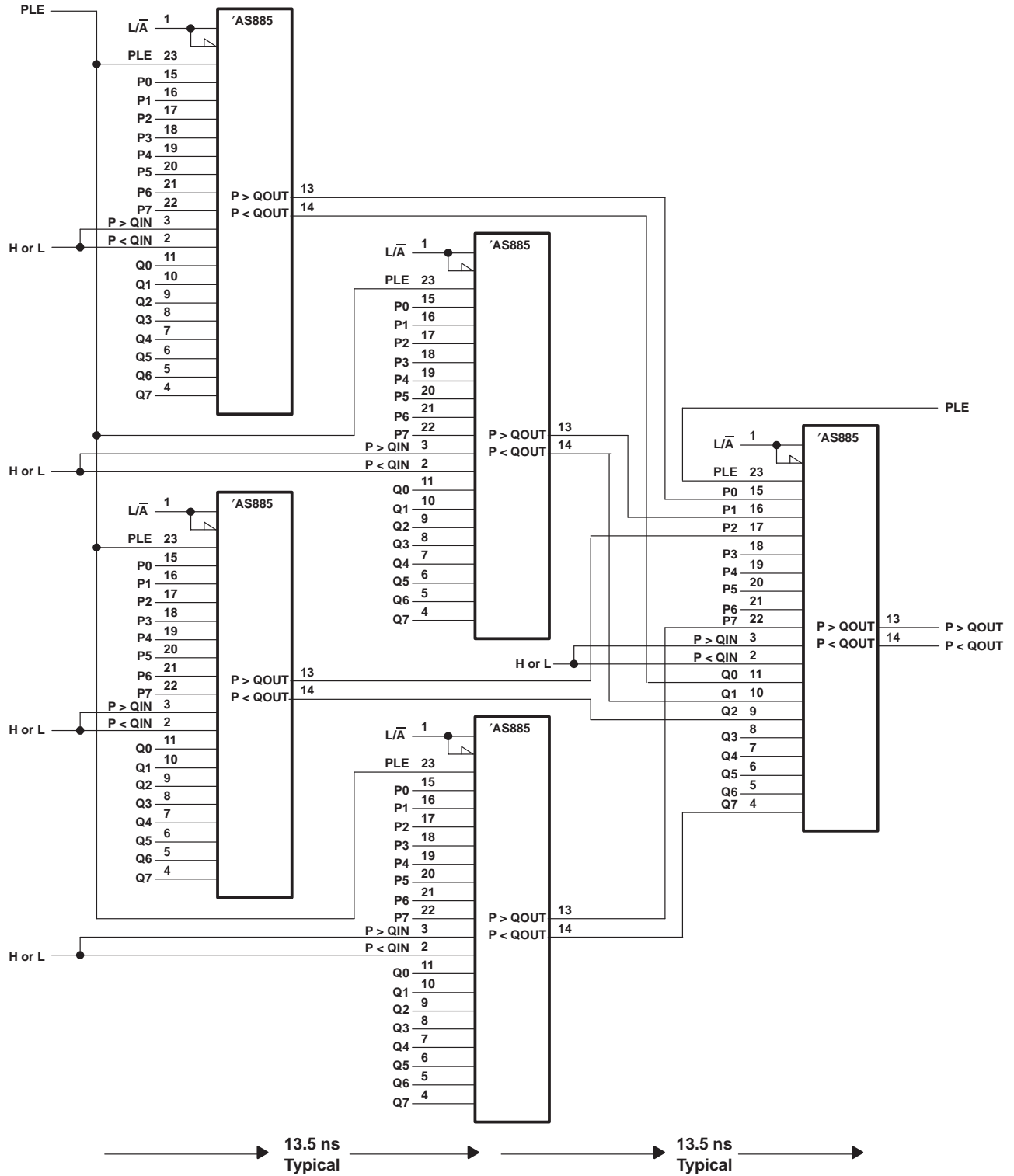


Figure 1. 32-Bit to 72 (n)-Bit Magnitude Comparator

APPLICATION INFORMATION

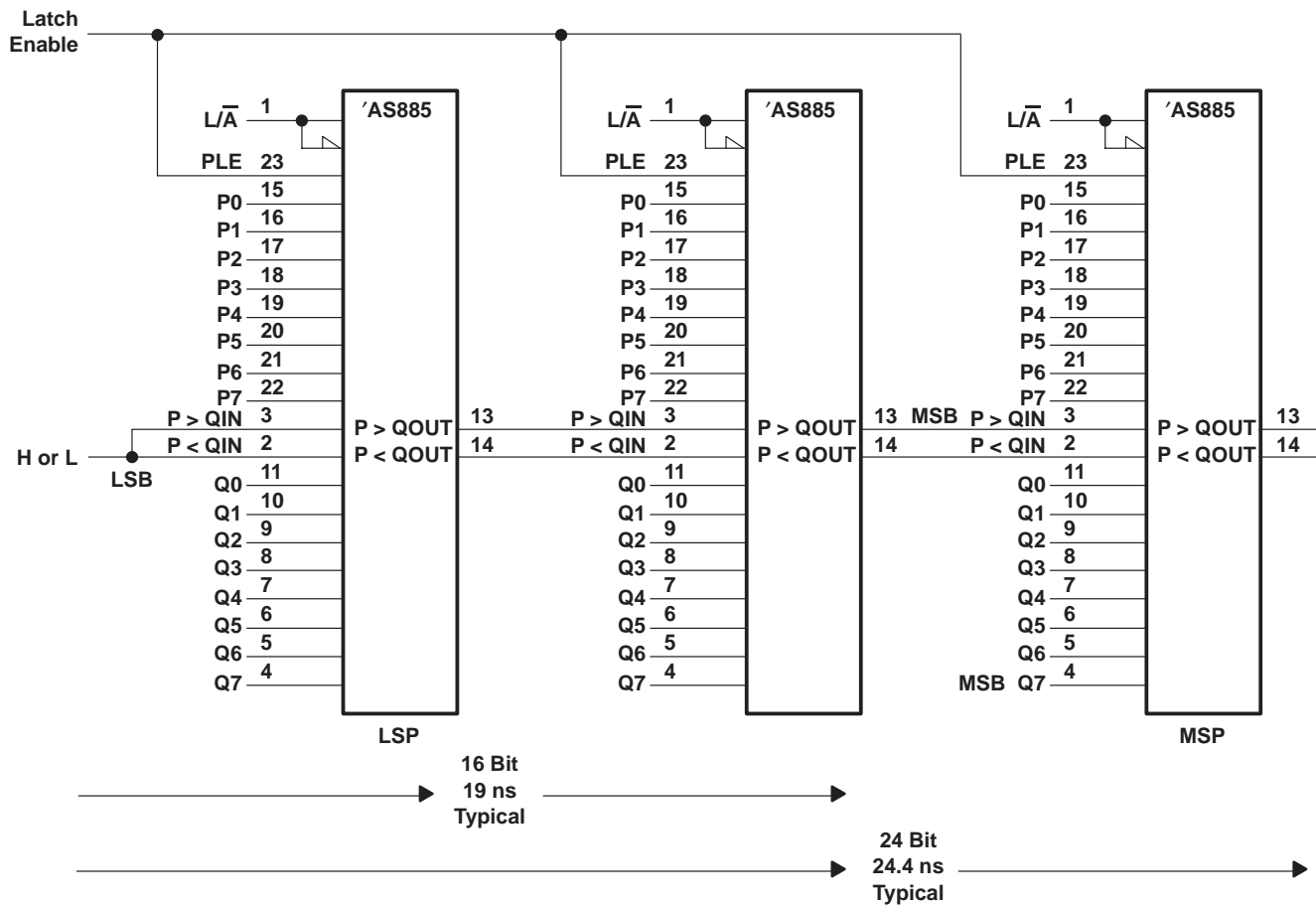
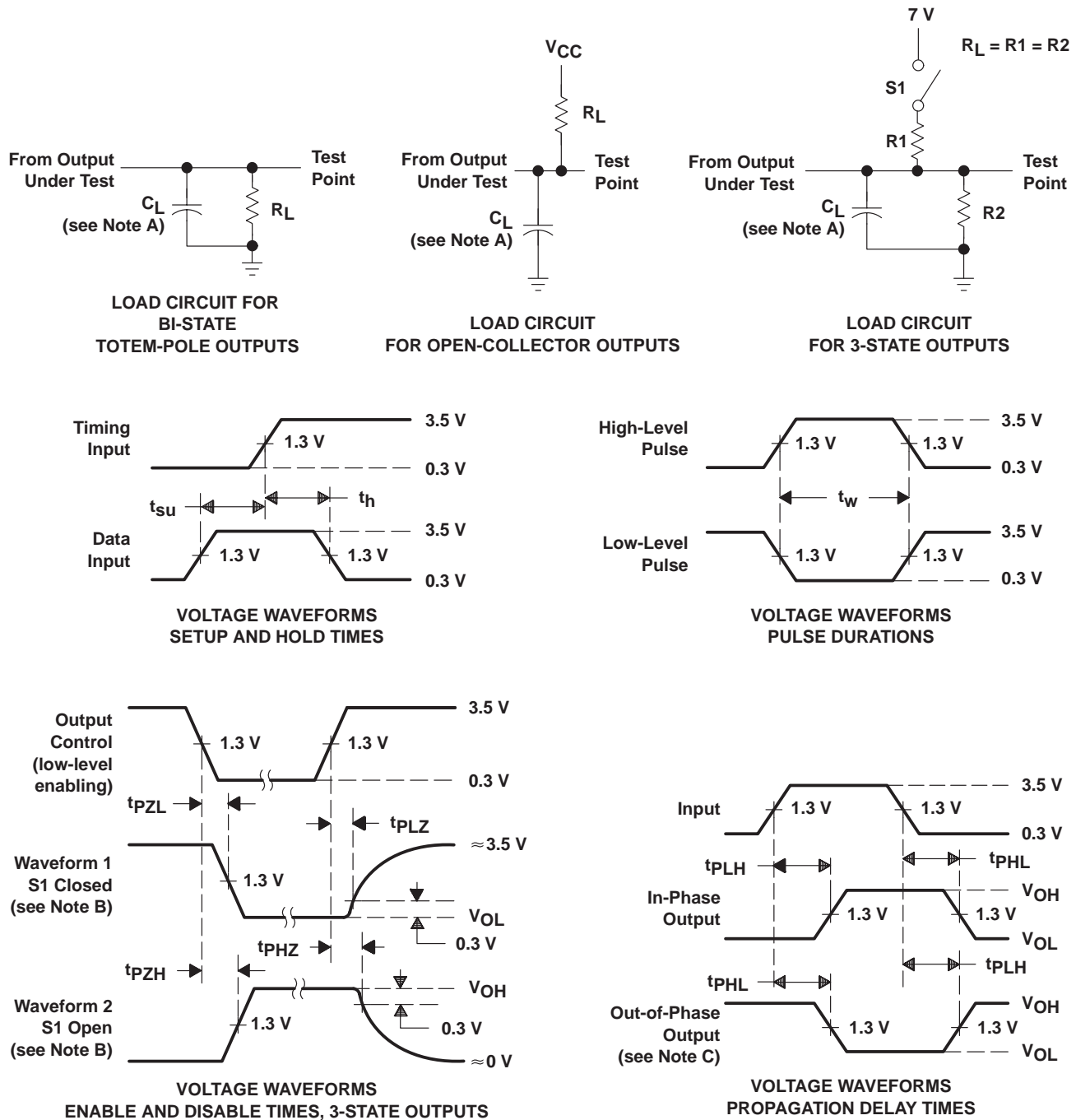


Figure 2. Fastest Cascading Arrangement for Comparing 16-Bit or 24-Bit Words

SN54AS885, SN74AS885 8-BIT MAGNITUDE COMPARATORS

SDAS236A – DECEMBER 1982 – REVISED JANUARY 1995

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 3. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-89757013A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-89757013A SNJ54AS 885FK	Samples
5962-8975701KA	NRND	CFP	W	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8975701KA SNJ54AS885W	
5962-8975701LA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8975701LA SNJ54AS885JT	Samples
SN54AS885JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54AS885JT	Samples
SN74AS885DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AS885	Samples
SN74AS885NT3	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		
SNJ54AS885FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-89757013A SNJ54AS 885FK	Samples
SNJ54AS885JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8975701LA SNJ54AS885JT	Samples
SNJ54AS885W	NRND	CFP	W	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8975701KA SNJ54AS885W	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AS885, SN74AS885 :

● Catalog: [SN74AS885](#)

● Military: [SN54AS885](#)

NOTE: Qualified Version Definitions:

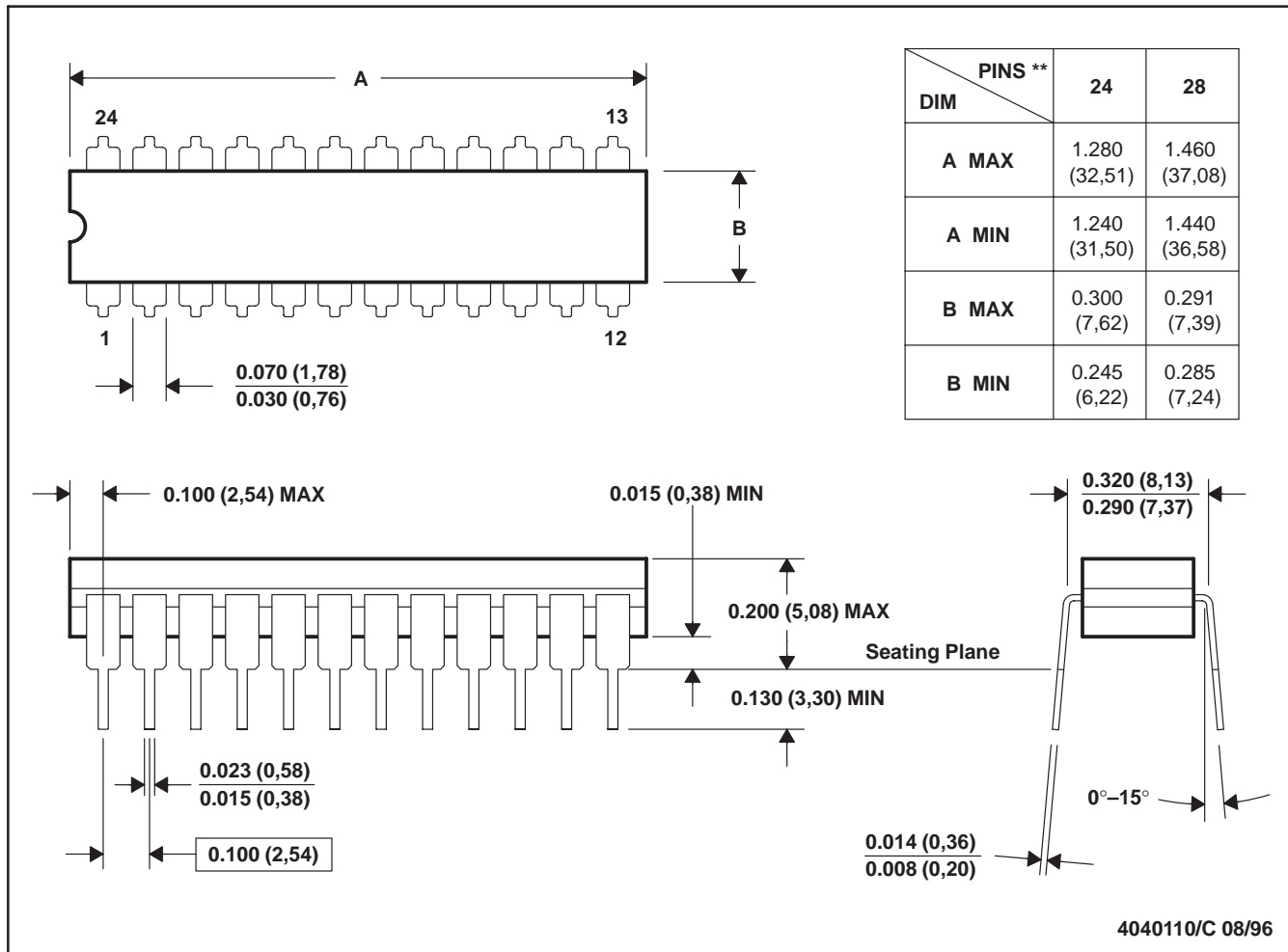
● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

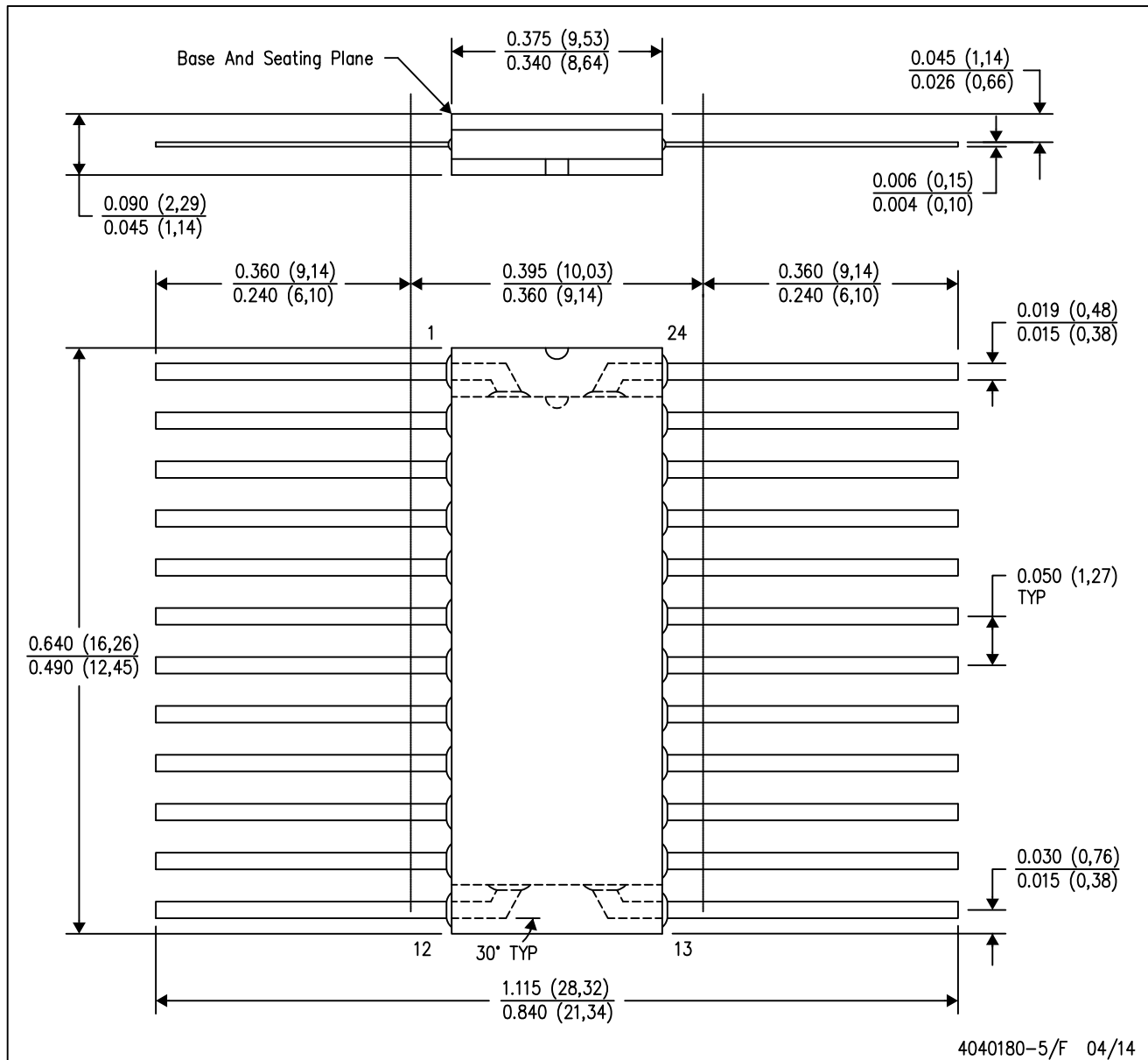
24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

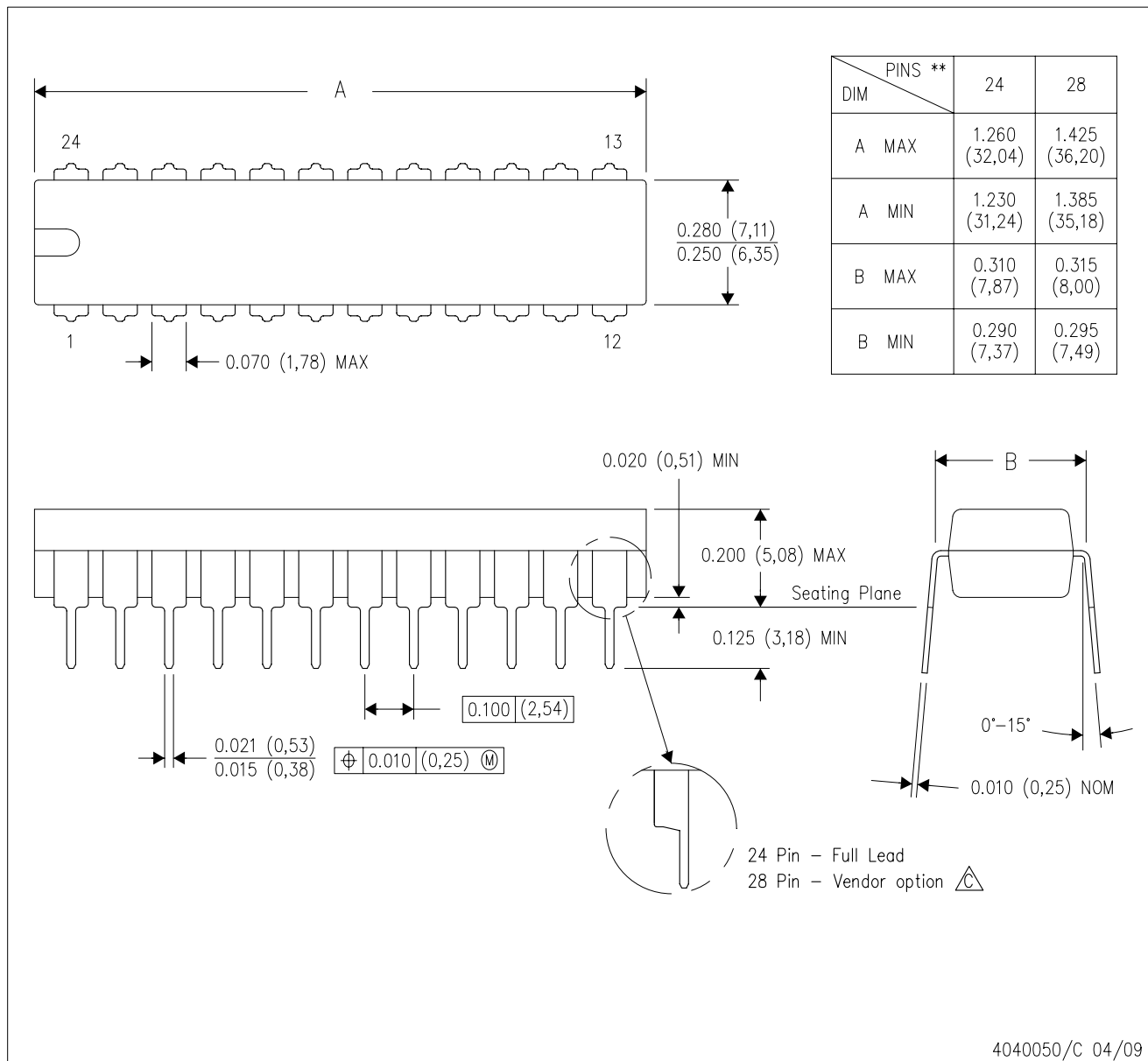
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004


MECHANICAL DATA

NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  The 28 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com