- **Complete Discrete Multitone-Based Asymmetric Digital Subscriber Line Coder/Decoder**
- **Supports Full Rate ADSL and G.Lite Application in Both Echo Cancellation or FDM Modes**
- **Integrated 14-Bit Converter for Transmitter/Receiver**
- **Integrated Transmit/Receive Channel Filters**
- **Integrated Transmit/Receive Attenuation/Gain**
- **Integrated Reference**
- **High-Speed Parallel Interface**
- **16-Bit 2s-Complement Data Format**
- **Selectable Parallel Data Transfer Rate**
- **Serial Configuration Port**
- **Eight General-Purpose Output Terminals**
- **Supports Multiple-Channel Configuration**
- **Single 3.3-V Supply**
- **Low Power Consumption, –450 mW at External Bias Mode**
- **–40°C to 85°C Operational Temperature**
- **Hardware/Software Power Down**
- **100-Terminal LQFP (PZ) Package**

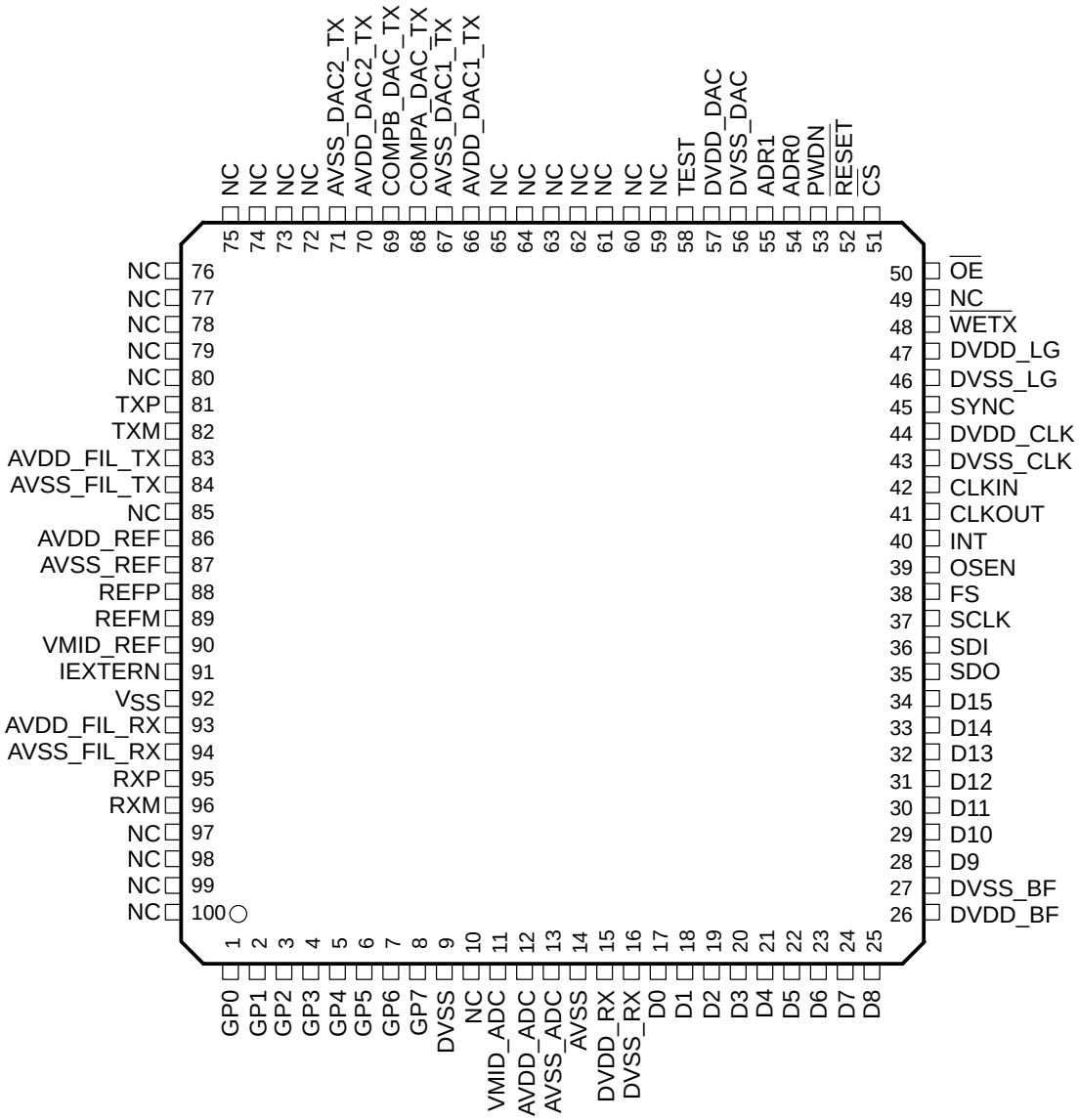
description

The TLV320AD16 is a high-speed coder/decoder (codec) for a central office-side (CO) discrete-multitone-based (DMT) asymmetric-digital subscriber line (ADSL) access that supports full rate ADSL, G.lite, and reduced-NEXT (near end cross talk) digital-filter FDM applications. The codec is a low-power device comprised of five functional blocks: transmitter (TX), receiver (RX), clock, reference, and host interface.

The transmit channel consists of selectable digital filters, a 14-bit, 8.832-MSPS DAC, a 1.104-MHz analog low-pass filter, and a transmit attenuator. The receiver channel consists of a three programmable-gain-amplifier stages (PGA), a 138-kHz analog low-pass filter (LPF), a 14-bit, 2.208-MSPS ADC, and a 138-kHz digital LPF. The sample phase and rate can be software selected. An onboard reference circuit generates 1.5-V reference voltage for the converters.

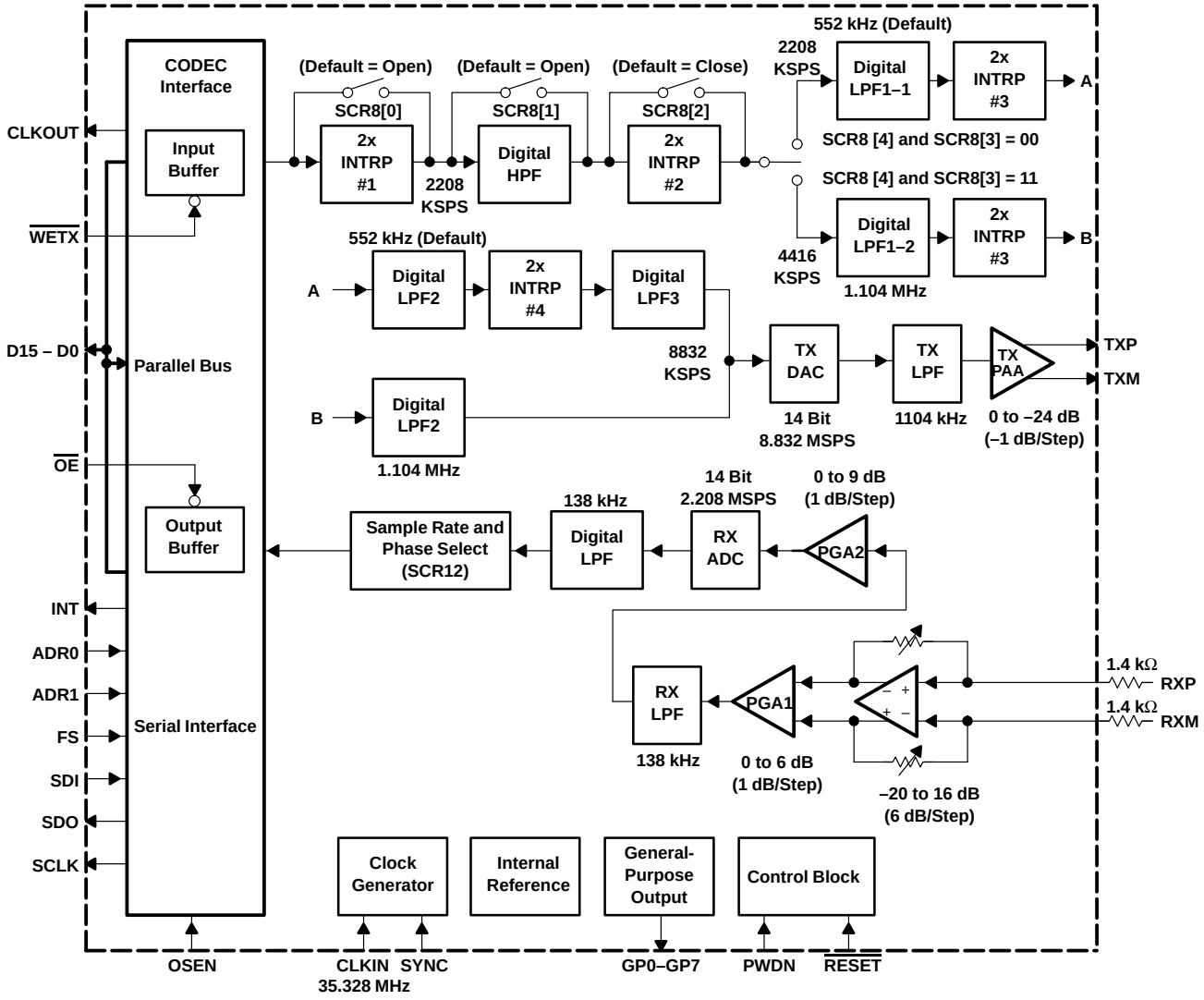
The codec has two interface ports: a parallel port for data transfer and a serial port for control. The parallel port is 16 bits wide, and is reserved for moving data between the codec and the host transceiver, such as the TMS320C6XX. Configuration is done via the serial port. A special interface scheme enables multichannel system design. The TLV320AD16 can be powered down via a dedicated terminal or through software control to reduce heat dissipation. Additionally, there is a general-purpose (GP) port consisting of eight output terminals for control of external circuitry.

PZ PACKAGE
(TOP VIEW)



NC – No internal connection

functional block diagram



NOTE: SCR8 and SCR12 are system control registers (see register programming for details).

Terminal Functions

TERMINAL		I/O†	DESCRIPTION
NAME	NO. PZ		
ADR0 ADR1	54 55	I	Serial-port chip ID address. ADR0 is the least significant bit. See multiple-channel configuration for detail.
AVDD_ADC	12	I	Analog-to-digital converter (ADC) analog power supply
AVDD_DAC1_TX	66	I	TX-channel analog power supply 1
AVDD_DAC2_TX	70	I	TX-channel analog power supply 2
AVDD_FIL_RX	93	I	RX-channel filter analog power supply
AVDD_FIL_TX	83	I	TX-channel filter analog power supply
AVDD_REF	86	I	Reference analog power supply
AVSS	14	I	Analog ground
AVSS_ADC	13	I	ADC analog ground
AVSS_DAC1_TX	67	I	TX-channel analog ground 1
AVSS_DAC2_TX	71	I	TX-channel analog ground 2
AVSS_FIL_RX	94	I	RX-channel filter analog ground
AVSS_FIL_TX	84	I	TX-channel filter analog ground
AVSS_REF	87	I	Reference analog ground
CLKIN	42	I	35.328-MHz external oscillator clock input
CLKOUT	41	0	RX channel digital interface data rate indicator of Rx internal buffer
COMPA_DAC_TX	68	I	TX-channel decoupling capacitor input A (add 500 pF X7R ceramic capacitor between this terminal and AVDD_DAC1_TX)
COMPB_DAC_TX	69	I	TX-channel decoupling capacitor input B (add 1-μF X7R ceramic capacitor between this terminal and AVDD_DAC1_TX)
$\overline{CS}$	51	I	Parallel-port chip select from host processor
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	34 33 32 31 30 29 28 25 24 23 22 21 20 19 18 17	I/0	(MSB) Parallel-port data. D0 is the least significant bit. (LSB)
DVDD_BF	26	I	Digital I/O buffer power supply
DVDD_CLK	44	I	Digital clock power supply
DVDD_DAC	57	I	Digital power supply for digital-to-analog converter (DAC)
DVDD_LG	47	I	Digital logic power supply
DVDD_RX	15	I	Digital power supply for RX channel
DVSS	9	I	Digital ground
DVSS_BF	27	I	Digital I/O buffer ground
DVSS_CLK	43	I	Digital clock ground

† I = input, O = output, I/O = 3-state input/output

Terminal Functions

TERMINAL		I/O†	DESCRIPTION
NAME	NO. PZ		
DVSS_DAC	56	I	Digital ground for DAC
DVSS_LG	46	I	Digital logic ground
DVSS_RX	16	I	Digital ground for RX channel
FS	38	I	Frame sync input for serial interface
GP7 GP6 GP5 GP4 GP3 GP2 GP1 GP0	8 7 6 5 4 3 2 1	0	General-purpose output port
IEXTERN	91	I	External bias current input. Used in external bias mode only. See *voltage reference* section for detail.
INT	40	0	Transmit channel digital interface data rate indicator. Indicates the update rate of the internal transmit buffer.
NC	10, 49, 59, 60, 61, 62, 63, 64, 65, 72, 73, 74, 75, 76, 77, 78, 79, 80, 85, 97, 98, 99, 100		No connection. All the NC terminals should be left open.
$\overline{OE}$	50	I	Parallel-port output enable for receive channel from host processor
OSEN	39	I	Hardware configuration: OSEN = 1 enables oversampling mode for the TX channel and the interface data rate needs to be doubled. The default state is low.
PWDN	53	I	Hardware power-down input. When PWDN = 1, the device is in the hardware power-down mode. The default state is low.
REFM	89	0	Decoupling reference voltage minus. Add 10-μF X5R and 0.1-μF X7R ceramic capacitors to AVSS_REF and REFP. The normal dc voltage at this terminal is 0.5 V. See Figure18 for the configuration.
REFP	88	0	Decoupling reference voltage plus. Add 10-μF X5R and 0.1-μF X7R ceramic capacitors to AVSS_REF and REFM. The normal dc voltage at this terminal is 2.5 V. See Figure18 for the configuration.
$\overline{RESET}$	52	I	Hardware system reset. A low level pulse will reset the device to its default state.
RXM	96	I	Analog input minus for the Rx channel. RXM is self-biased to AVDD_FIL_RX/2. A 1.4 kΩ series resister is needed for the input.
RXP	95	I	Analog input plus for the Rx channel. RXP is self-biased to AVDD_FIL_RX/2.A 1.4 kΩ series resister is needed for the input.
SCLK	37	0	Clock output for serial interface
SDI	36	I	Data input for serial interface
SDO	35	0	Data output for serial interface
SYNC	45	I	SYNC pulse for INT synchronization. A high pulse to this terminal synchronizes the clock operation. Refer to Figure 3 for detail.

Terminal Functions

TERMINAL NAME	TERMINAL NO. PZ	I/O†	DESCRIPTION
TEST	58	I	Extended system control register access bit. When the TEST pin is set to high, the part enters test mode and the extend system control registers can be accessed. The test terminal needs to be set to high for the external bias mode. The test terminal needs to be set to low for the normal mode.
TXM	82	0	Analog output minus for TX channel
TXP	81	0	Analog output plus for TX channel
VMID_ADC	11	0	Decoupling 1.5 V for ADC. Add 10-µF X5R and 0.1-µF X7R ceramic capacitors to AVSS_ADC.
VMID_REF	90	0	Decoupling 1.5 V reference voltage. Add 10-µF X5R and 0.1-µFX7R ceramic capacitors to AVSS_REF.
V_{SS}	92	I	Substrate. Connect V_{SS} to analog ground.
$\overline{WETX}$	48	I	Parallel-port write enable for transmit channel from host processor

† I = input, O = output, I/O = 3-state input/output

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, AV_{DD} to AGND, DVDD to DGND . . . . . –0.3 V to 4.5 V
Analog input voltage range to AGND . . . . . –0.3 V to AVDD + 0.3 V
Digital input voltage range to DGND . . . . . –0.3 V to DVDD+ 0.3 V
Operating virtual-junction temperature range, T_J . . . . . –40°C to 150°C
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

power supply

		MIN	NOM	MAX	UNIT
Supply voltage	All power supplies	3	3.3	3.6	V

digital inputs

		MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}	Input current = 0.75 mA	2			V
Low-level input voltage, V_{IL}	Input current = – 0.75 mA			0.8	V
Reset pulse width		80			ns
Input capacitance		5	10		nf

analog input

		MIN	NOM	MAX	UNIT
Analog input signal range	AVDD_FIL_RX = 3.3 V. The input signal is measured differentially and CPGA is set to –20 dB		30		Vp-p

clock

		MIN	NOM	MAX	UNIT
Input clock frequency	DVDD_CLK=3.3 V		35.328		MHz
Input clock duty cycle			50%		

electrical characteristics, typical at 25°C, analog power supply = 3.3 V, digital power supply = 3.3 V, f_{CLKIN} = 35.328 MHz (unless otherwise noted)

TX channel (measured differently, PAA=0 dB, unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Signal bandwidth	G.Lite mode		552		kHz
		Full rate with reduced NEXT (with 138 kHz DHPF)		1104		
		Full rate with EC		1104		
	Conversion rate			8.832		MHz
	Channel gain error	Test signal 43 kHz, full rate echo cancelled	–0.6		–0.2	dB
	PAA attenuation step error			–0.4	0.1	dB
PSRR	Power supply reject ratio	Apply 250 mVp-p multitone to TX power supply and measure 300 kHz at TX		–54	-45	dB
	Group delay	Relative delay		10		µs
	Output compliance voltage	Load=2000 Ω		3		Vp-p
AC Performance						
THD	Total harmonic distortion	Test signal 43 kHz, full rate echo cancelled Test signal 172 kHz, full rate and G.Lite reduced NEXT		–90	–76	dB
SNR	Signal to noise ratio		68	74		dB
SNDR	Signal-to-noise and harmonic distortion ratio		67	74		dB
MT	Missing tone test	Apply multitone with 120 kHz and 250 kHz missing		–65		dB

RX channel (measured differently, PGA1=0 dB, PGA2=0 dB, unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Channel bandwidth			138		kHz
	Clock rate			2208		kHz
	Channel gain error	CPGA = –2 dB, PGA1 =0dB, PGA2 =0dB, test signal = 10 kHz	–0.25		0.25	dB
	PGA gain step error	CPGA		0.10		dB
		PGA1		0.2		
		PGA2		0.1		
PSRR	Power supply reject ratio	Apply 250 mVp-p multitone to RX power supply and measure 60 kHz at RX		–65	–60	dB
	DC offset			0.09		mV
	Cross talk			73		dB
	Group delay	Relative delay		60		µs
CMRR	Common mode reject ratio			89		dB
	Analog input self-bias dc voltage		AVDD_FIL_RX/2			V
AC Performance						
THD	Total harmonic distortion	Test signal 43 kHz @ –3 dB		–90	–84	dB
SNR	Signal to noise ratio		70	75		dB
SNDR	Signal-to-noise and harmonic distortion ratio		68	75		dB
MT	Missing tone test	Apply multitone with 120 kHz missing		65		dB

electrical characteristics, typical at 25°C, analog power supply = 3.3 V, digital power supply = 3.3 V, f_{CLKIN} = 35.328 MHz (unless otherwise noted) (continued)

reference voltage

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFP	ADC positive reference	AVDD_REF=3.3V	2.4	2.5	2.6	V
REFM	ADC negative reference		0.4	0.5	0.6	V
VMID_REF			1.4	1.5	1.6	V
VMID_ADC	Receive channel mid-input voltage		1.4	1.5	1.6	V

power dissipation

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Power dissipation	Active mode	Internal reference		600		mW
		External reference		450		
Power dissipation	Power-down mode	Hardware power down		60	80	mW
		Software power down		60	80	

digital output

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	Output current = 0.5 mA	2.4			V
V_{OL}	Low-level output voltage	Output current = –0.5 mA			0.6	V

timing requirements over recommended ranges of supply voltage and operating free-air temperature with 10 pF load(unless otherwise noted)

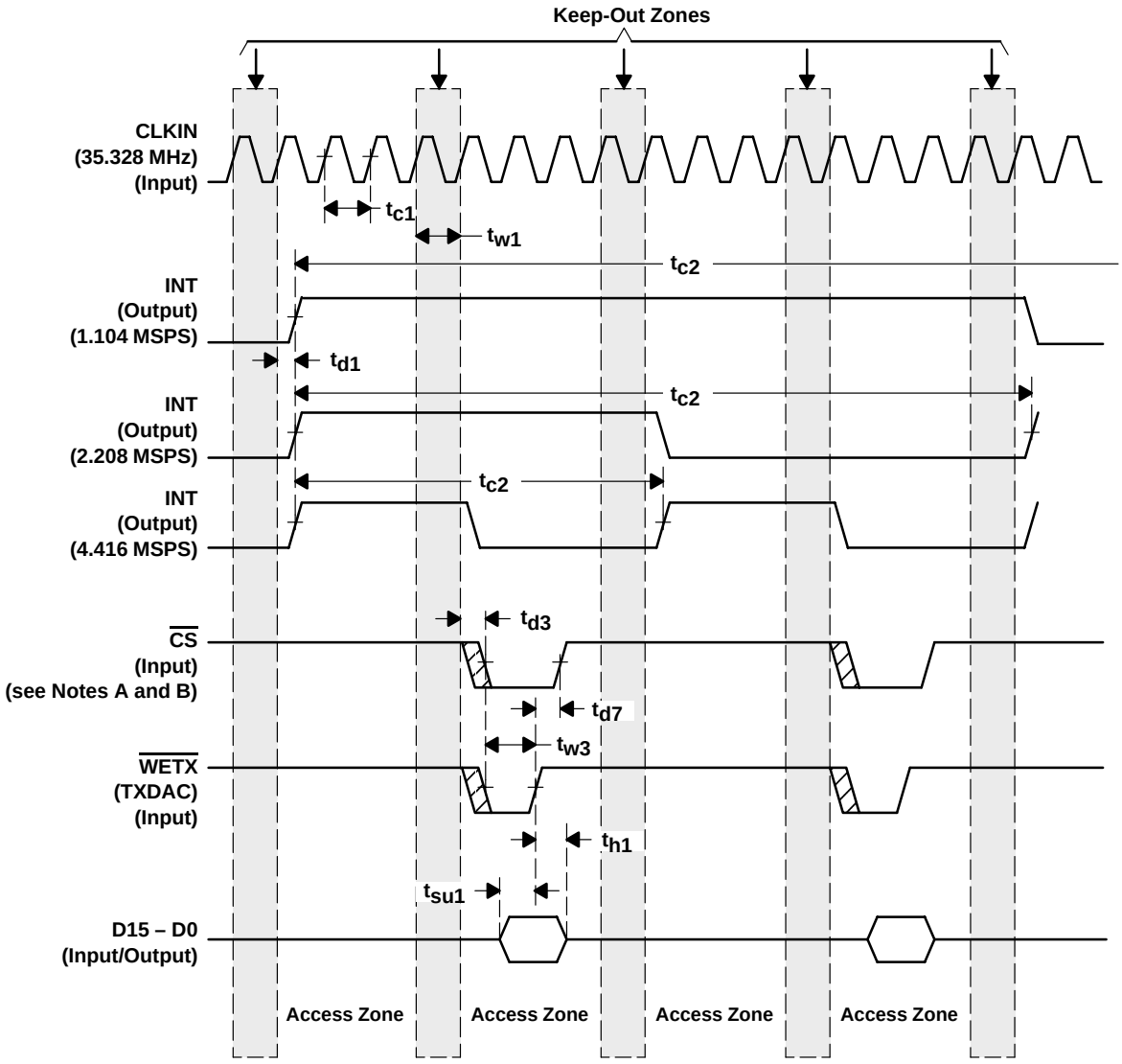
parallel port (see Figures 1, 2 and 3)

PARAMETER			MIN	TYP	MAX	UNIT
t_{c1}	Period, CLKIN			28.3		ns
t_{c2}	Cycle time, INT	OSEN/SCR8[4]=00		32		CLKIN
		OSEN/SCR8[4]=01/10		16		
		OSEN/SCR8[4]=11		8		
t_{c3}	Period, CLKOUT	SCR12[4:3]=00		16		
		SCR12[4:3]=01		32		
		SCR12[4:3]=10		64		
		SCR12[4:3]=11		128		
t_{d1}	Delay time, keep-out zone end to INT↑				16	ns
t_{w3}	Pulse width, $\overline{\text{WETX}}$		28			ns
t_{d4}	Delay time, data valid after $\overline{\text{OE}}$↓				15	ns
t_{d5}	Delay time, data valid (before change to high–Z) after $\overline{\text{OE}}$↑				5	ns
t_{d7}	Delay time, $\overline{\text{WETX}}$↑ to $\overline{\text{CS}}$↑		5			ns
t_{w2}	Pulse width, $\overline{\text{OE}}$		20			ns
t_{d2}	Delay time, keep out zone end (CLKIN↑) to $\overline{\text{CS}}$↓/$\overline{\text{OE}}$↓		0			ns
t_{d3}	Delay time, keep out zone end (CLKIN↑) to $\overline{\text{CS}}$↓/$\overline{\text{WETX}}$↓		0			ns
t_{su1}	Setup time, data valid before $\overline{\text{WETX}}$↑		15			ns
t_{h1}	Hold time, data valid after $\overline{\text{WETX}}$↑		5			ns
t_{w1}	Pulse width, keep-out zone time			1		CLKIN
t_{su2}	Setup time, SYNC keep high before CLKIN↑		10			ns
t_{h2}	Hold time, SYNC keep high after CLKIN↑		5			ns
t_{w4}	Pulse width, SYNC			28		ns

serial port (see Figure 4)

PARAMETER		MIN	TYP	MAX	UNIT
t_{su4}	Setup time, SDI valid before SCLK↓	20			ns
t_{h4}	Hold time, SDI valid after SCLK↓	5			ns
t_{su3}	FS become high before SCLK↓	20			ns
t_{h3}	FS keep high after SCLK↓	5			ns
t_{w5}	FS pulse width		28		ns
t_{c4}	Cycle time, SCLK		8		CLKIN
t_{c5}	Cycle time, FS	18			SCLK
t_{d6}	Delay time, SCLK rising edge to SOD valid			15	ns

PARAMETER MEASUREMENT INFORMATION

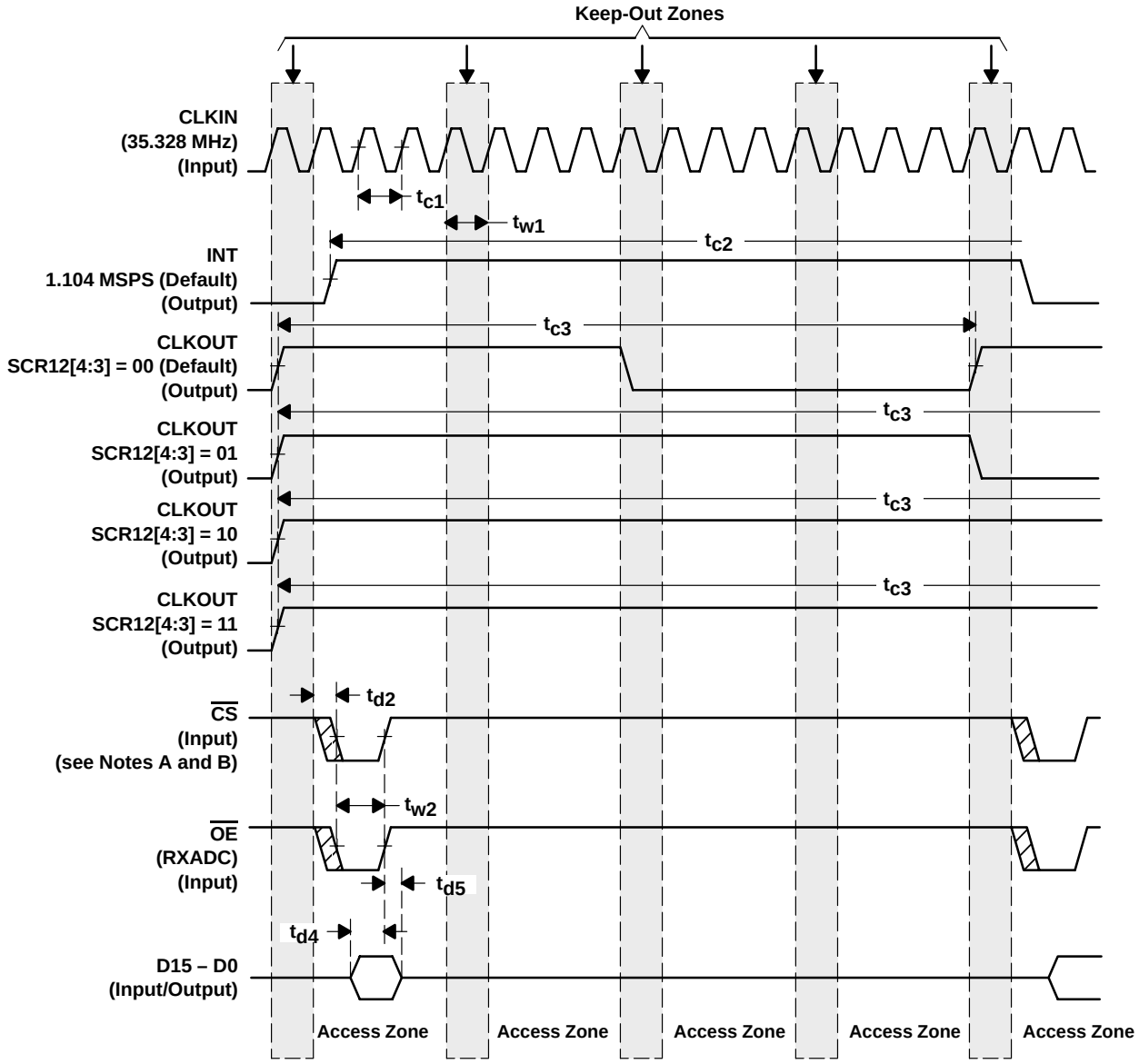


NOTES: A. $\overline{CS}$ and $\overline{WETX}$ may fall together or be skewed from each other, but the rising edge of $\overline{WETX}$ must occur prior to the rising edge of $\overline{CS}$.

B. The operation of $\overline{CS}$ and $\overline{WETX}$ shown above is under condition of OSEN/SCR8[4]=11, and is not a default function. *As long as the write operation does not conflict with read operation, the write operation can occur at any place except the keep-out-zone.*

Figure 1. Parallel Timing Diagram (TX)

PARAMETER MEASUREMENT INFORMATION

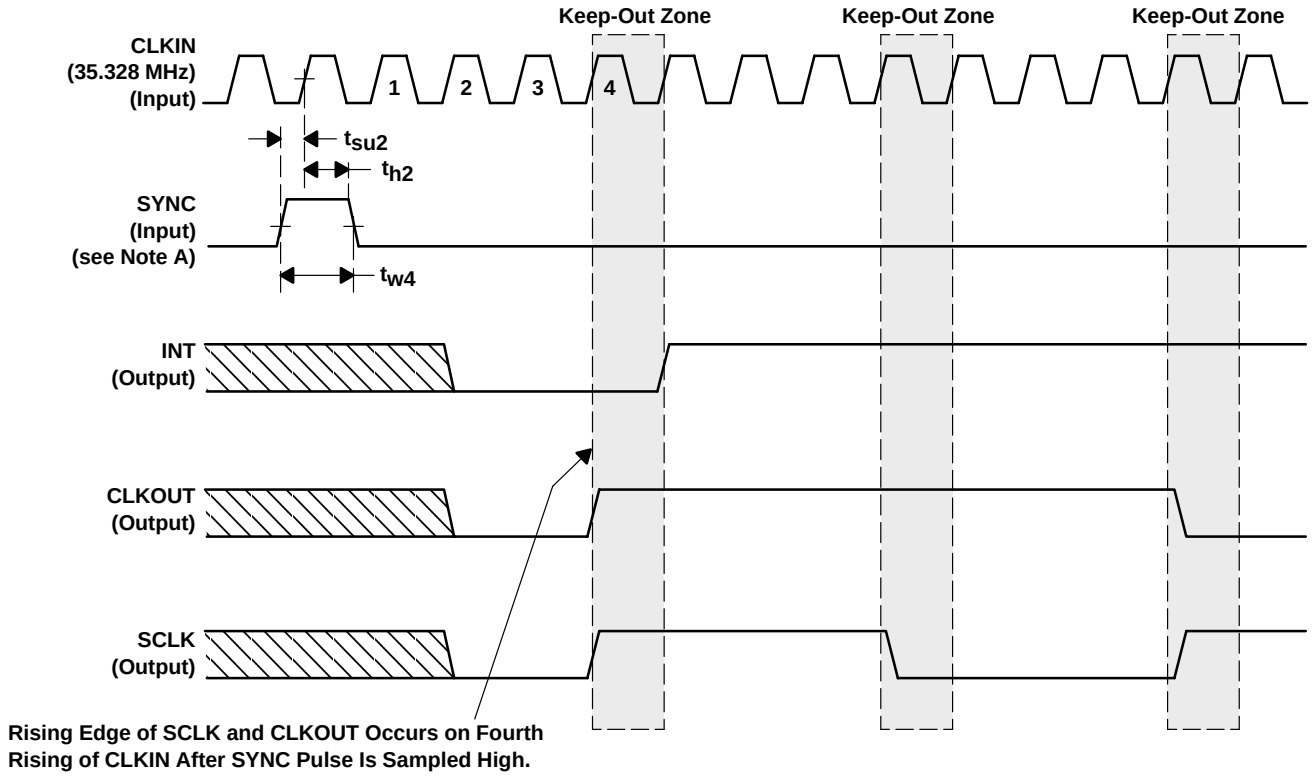


NOTES: A. $\overline{CS}$ and $\overline{OE}$ may fall/rise together or be skewed from each other. It does not matter which falls/rises first. However, t_{d4} is referenced from whichever falls last and t_{d5} is referenced from whichever rises first.

B. The operation of $\overline{CS}$ and $\overline{OE}$ shown above is for default condition (SCR8[4:3]=00). *As long as the read operation does not conflict with write operation, the read operation can occur at any place except the keep-out-zone.*

Figure 2. Parallel Timing Diagram (RX)

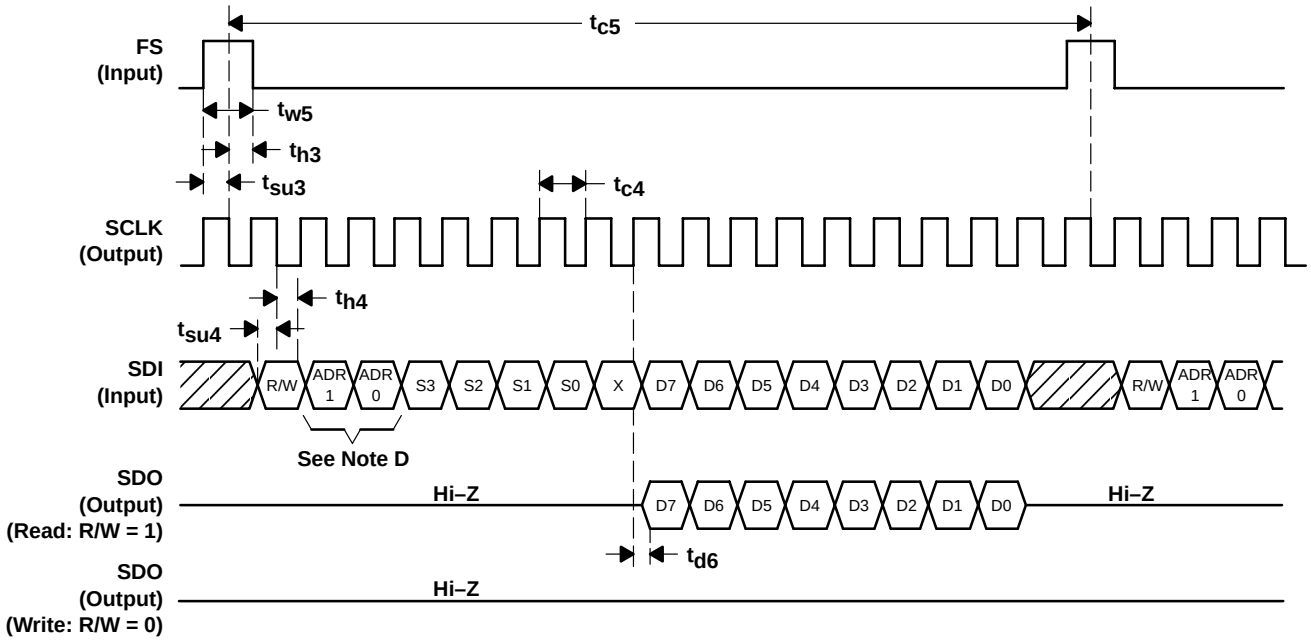
PARAMETER MEASUREMENT INFORMATION



NOTE A: SYNC is only used during multi-codec system to synchronous operation. The part can automatically meet the keep-out-zone requirement when used alone.

Figure 3. Sync Pulse Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. FS is sampled at the falling-edge of SCLK
B. Data is latched at the falling-edge of SCLK.
C. Data is sent out at the rising-edge of SCLK.
D. ADR0 and ADR1 are the configuration of pin ADR0 and ADR1.

Figure 4. Serial Port Timing

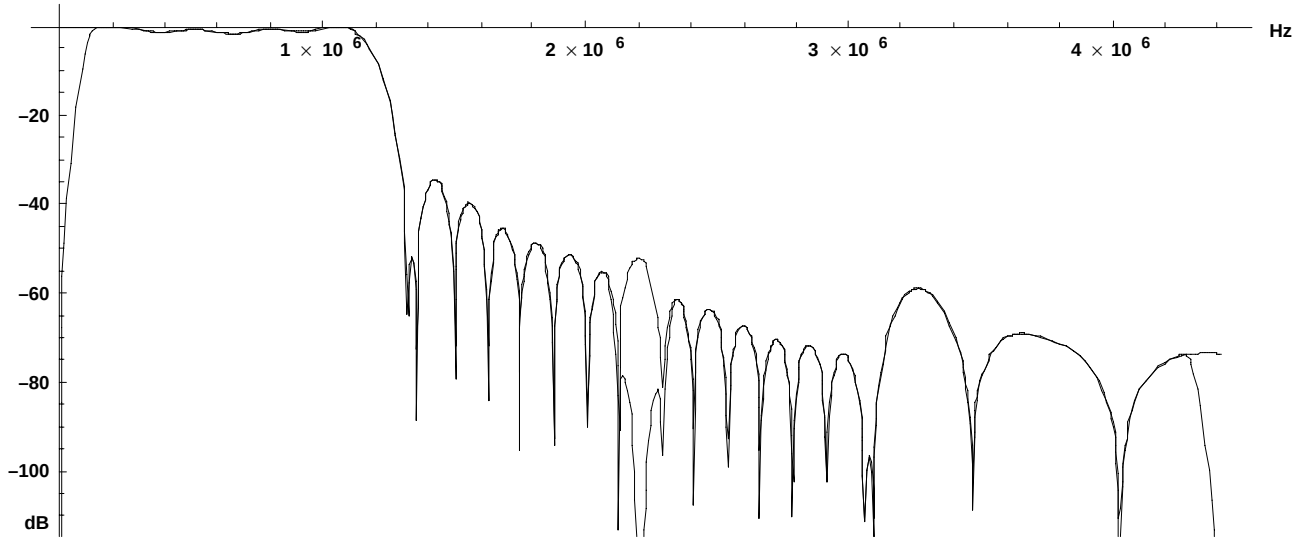


Figure 5. TLV320AD16 Transmitter Channel Frequency Response in Full Rate Mode With and Without Reduced Next High-Pass Over Frequency Range DC–4416 kHz

PARAMETER MEASUREMENT INFORMATION

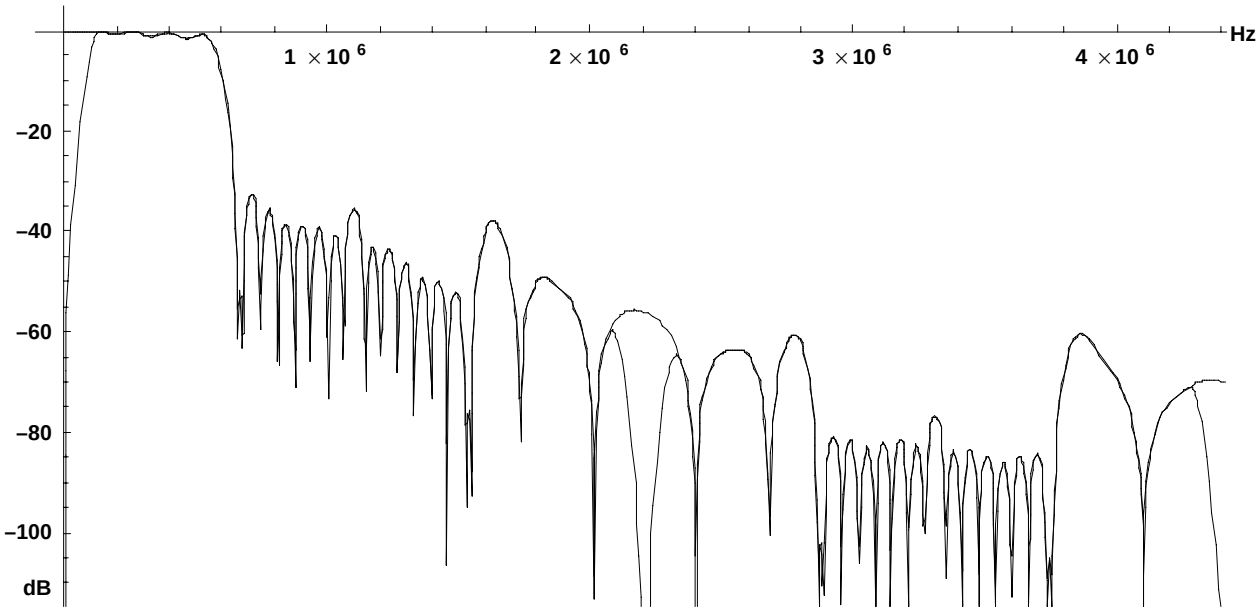


Figure 6. TLV320AD16 Transmitter Channel Frequency Response in G.lite Mode With and Without Reduced Next High-Pass Over Frequency Range DC–4416kHz.

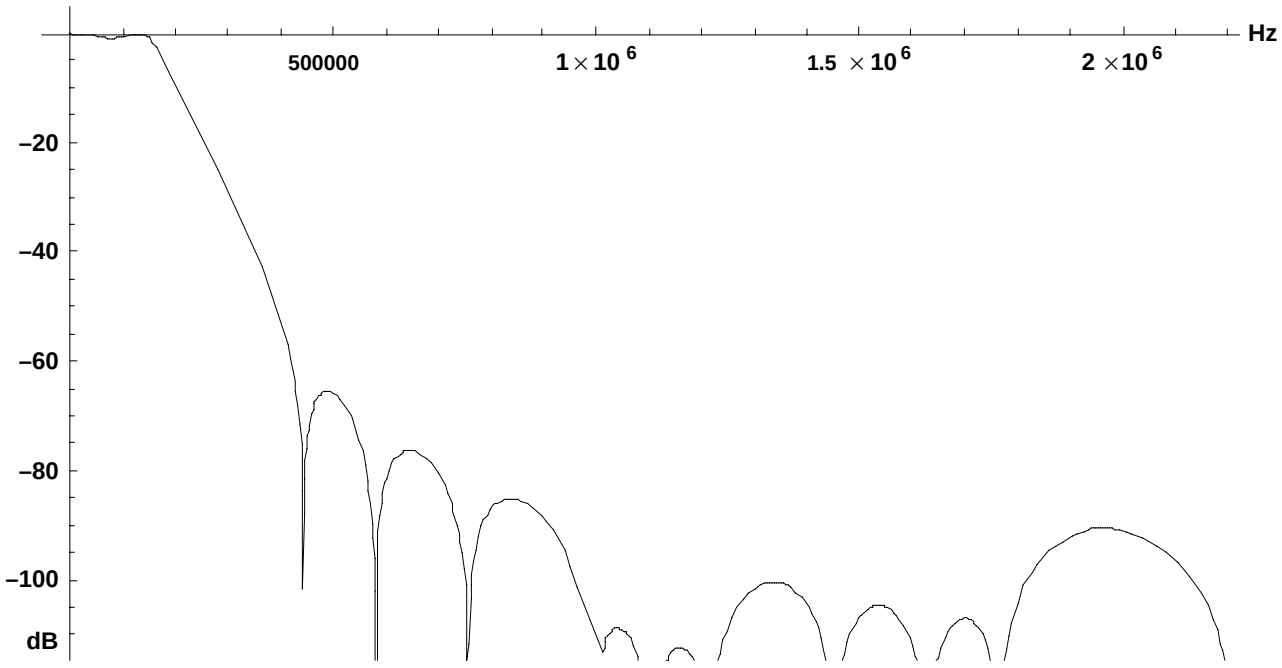


Figure 7. TLV320AD16 Receive Channel Frequency Response

THERMAL INFORMATION

thermal resistance characteristics (S-PQFP package)

NO			°C/W	AIR FLOW LFPM†
1	$R1_{JC}$	Junction-to-case	5.40	N/A
2	$R1_{JC}$	Junction-to-free air	30.4	0
3	$R1_{JC}$	Junction-to-free air	24.2	100
4	$R1_{JC}$	Junction-to-free air	22.3	250
5	$R1_{JC}$	Junction-to-free air	20	500

† LFPM - Linear feet per minute

PROGRAMMING INFORMATION

Table 1. System Control Register (SCR)

SYSTEM CONTROL REGISTER		MODE	DEFAULT VALUE	FUNCTION
NAME	ADDRESS			
	S3, S2, S1, S0			
SCR0	0000	R/W	00000000	D0: S/W RESET (self-clearing). D1 to D6: Reserved. D7: ESCR access enable
SCR1	0001	R/W	00000000	TX channel PAA attenuation select. D[4:0] = 00000 for 0 dB and D[4:0] = 11000 for –24 dB
SCR2	0010	R/W	00000000	RX channel PGA1 gain select. D[2:0] = 000 for 0 dB and D[2:0] = 110 for 6 dB
SCR3	0011	R/W	00000000	RX channel PGA2 gain select. D[3:0] = 0000 for 0 dB and D[3:0] = 1001 for 9 dB
SCR4	0100			Reserved
SCR5	0101			Reserved
SCR6	0110	R/W	00000000	D[7:0] = GP [7:0]
SCR7	0111	R/W	00000000	MISC.1. Control (set to 1 to enable) D0: Reserved D1: S/W power down RX channel with reference on D2: S/W power down TX channel with reference on D3: Analog loop back. TXP and TXM are internally connected to RXP and RXM. D4: Digital loop back. RX channel digital output is internally connected to TX channel digital input. D5: TX data read back mode. D6: Rx signal read back mode. D7: Reserved.
SCR8	1000	R/W	00000000	MISC.2. Control (set to 1 to enable) D0: TX INT1 BYP D1: TX HPF BYP D2: TX INT2 EN D3: TX DLPF BYP D4: MODE TX FULL D[7:5]: CPGA gain select. D[7:5]=000 for –20dB and D[7:5]=110 for +16dB.
SCR9	1001	R/W	00000000	RX offset word [7:0].
SCR10	1010	R/W	00000000	RX offset word [5:8]
SCR11	1011	R/W	00000000	D[7:4] = CTRL_DLPF1_GA[3:0] D[3:0] = CTRL_DLPF3_GA[3:0]
SCR12	1100	R/W	00000000	D[2:0] = CTRL–PHASE SEL[2:0] (see Figure 15) D[4:3] = CTRL_RATE SEL[1:0] (see Table 5)

NOTE 1: All reserved bits should be filled with 0 during operations. All registers are set to 0 after reset.

PROGRAMMING INFORMATION

Table 2. Extended System Control Register (ESCR)

SYSTEM CONTROL REGISTER		MODE	DEFAULT VALUE	FUNCTION
NAME	ADDRESS			
	S3, S2, S1, S0			
ESCR0	0000	R/W	00000000	D0: S/W RESET (self-cleaning) D7:ESCR access enable D1 to D6: Reserved
ESCR4	0100	R/W	00000000	D4:IREF_BYP D1 to D3 and D5 to D7: Reserved

NOTE 2: SCR0 and ESCR0 refer to the same register.

SCR0 – system control register Address:0000b contents at reset: 01000000b

D7	D6	D5	D4	D3	D2	D1	D0	REG. VALUE (HEX)	DESCRIPTION
0	1	0	0	0	0	0	1	41	D0=1:S/W reset (self clearing). All control registers are set to reset content.

SCR1 – system control register Address:0001b contents at reset: 00000000b

D7	D6	D5	D4	D3	D2	D1	D0	REG. VALUE (HEX)	DESCRIPTION
0	0	0	0	0	0	0	0	00	TX PAA attenuation = 0dB
0	0	0	0	0	0	0	1	01	TX PAA attenuation = 1dB
0	0	0	0	0	0	1	0	02	TX PAA attenuation = 2dB
0	0	0	0	0	0	1	1	03	TX PAA attenuation = 3dB
0	0	0	0	0	1	0	0	04	TX PAA attenuation = 4dB
0	0	0	0	0	1	0	1	05	TX PAA attenuation = 5dB
0	0	0	0	0	1	1	0	06	TX PAA attenuation = 6dB
0	0	0	0	0	1	1	1	07	TX PAA attenuation = 7dB
0	0	0	0	1	0	0	0	08	TX PAA attenuation = 8dB
0	0	0	0	1	0	0	1	09	TX PAA attenuation = 9dB
0	0	0	0	1	0	1	0	0A	TX PAA attenuation = 10dB
0	0	0	0	1	0	1	1	0B	TX PAA attenuation = 11dB
0	0	0	0	1	1	0	0	0C	TX PAA attenuation = 12dB
0	0	0	0	1	1	0	1	0D	TX PAA attenuation = 13dB
0	0	0	0	1	1	1	0	0E	TX PAA attenuation = 14dB
0	0	0	0	1	1	1	1	0F	TX PAA attenuation = 15dB
0	0	0	1	0	0	0	0	10	TX PAA attenuation = 16dB
0	0	0	1	0	0	0	1	11	TX PAA attenuation = 17dB
0	0	0	1	0	0	1	0	12	TX PAA attenuation = 18dB
0	0	0	1	0	0	1	1	13	TX PAA attenuation = 19dB
0	0	0	1	0	1	0	0	14	TX PAA attenuation = 20dB
0	0	0	1	0	1	0	1	15	TX PAA attenuation = 21dB
0	0	0	1	0	1	1	0	16	TX PAA attenuation = 22dB
0	0	0	1	0	1	1	1	17	TX PAA attenuation = 23dB
0	0	0	1	1	0	0	0	18	TX PAA attenuation = 24dB
–	–	–	–	–	–	–	–	19–FF	TX PAA attenuation = 24dB

PROGRAMMING INFORMATION

SCR2 – RX PGA1 control register Address:0010b contents at reset: 00000000b

D7	D6	D5	D4	D3	D2	D1	D0	REG. VALUE (HEX)	DESCRIPTION
0	0	0	0	0	0	0	0	00	RX PGA1= 0dB
0	0	0	0	0	0	0	1	01	RX PGA1= 1dB
0	0	0	0	0	0	1	0	02	RX PGA1= 2dB
0	0	0	0	0	0	1	1	03	RX PGA1= 3dB
0	0	0	0	0	1	0	0	04	RX PGA1= 4dB
0	0	0	0	0	1	0	1	05	RX PGA1= 5dB
0	0	0	0	0	1	1	0	06	RX PGA1= 6dB
–	–	–	–	–	–	–	–	06–FF	RX PGA1= 6dB

SCR3– RX PGA2 control register Address:0011b contents at reset: 00000000b

D7	D6	D5	D4	D3	D2	D1	D0	REG. VALUE (HEX)	DESCRIPTION
0	0	0	0	0	0	0	0	00	RX PGA2= 0 dB
0	0	0	0	0	0	0	1	01	RX PGA2= 1 dB
0	0	0	0	0	0	1	0	02	RX PGA2= 2 dB
0	0	0	0	0	0	1	1	03	RX PGA2= 3 dB
0	0	0	0	0	1	0	0	04	RX PGA2= 4 dB
0	0	0	0	0	1	0	1	05	RX PGA2= 5 dB
0	0	0	0	0	1	1	0	06	RX PGA2= 6 dB
0	0	0	0	0	1	1	1	07	RX PGA2= 7 dB
0	0	0	0	1	0	0	0	08	RX PGA2= 8 dB
0	0	0	0	1	0	0	1	09	RX PGA2= 9 dB
–	–	–	–	–	–	–	–	0A–FF	RX PGA2= 9 dB

SCR6– general-purpose output data register Address:0110b contents at reset: 00000000b

D7	D6	D5	D4	D3	D2	D1	D0	REG. VALUE (HEX)	DESCRIPTION
0/1	–	–	–	–	–	–	–		GP7 = low(0)/high(1)
–	0/1	–	–	–	–	–	–		GP6 = low(0)/high(1)
–	–	0/1	–	–	–	–	–		GP5 = low(0)/high(1)
–	–	–	0/1	–	–	–	–		GP4 = low(0)/high(1)
–	–	–	–	0/1	–	–	–		GP3 = low(0)/high(1)
–	–	–	–	–	0/1	–	–		GP2 = low(0)/high(1)
–	–	–	–	–	–	0/1	–		GP1 = low(0)/high(1)
–	–	–	–	–	–	–	0/1		GP0 = low(0)/high(1)

PROGRAMMING INFORMATION

SCR7 – Miscellaneous control register 1 Address:0111b contents at reset: 00000000b

D7	D6	D5	D4	D3	D2	D1	D0	REG. VALUE (HEX)	DESCRIPTION
–	–	–	–	–	–	–	0		Reserved
–	–	–	–	–	–	1	–		S/W power–down RX channel
–	–	–	–	–	1	–	–		S/W power–down TX channel
–	–	–	–	1	–	–	–		Analog loopback (see Note 3)
–	–	–	1	–	–	–	–		Digital loopback (see Note 4)
–	–	1	–	–	–	–	–		TX data read back mode (see Note 5)
–	1	–	–	–	–	–	–		RX analog input read back (see Note 6)
0	–	–	–	–	–	–	–		Reserved

NOTES: 3. Analog loopback: Analog output pins (TXP/TXM) are internally connected to RXP/RXM.
4. Digital loopback: RX digital output buffer (16-bit word) is internally connected to the TX digital input buffer.
5. The input digital data is read back from RX output buffer without going through DAC converter.
6. The input analog signal is read back from TX without going through ADC converter.

SCR8 – miscellaneous control register 2 (refer to block diagram for correspondent control pin) Address:1000b contents at reset: 00000000b

D7	D6	D5	D4	D3	D2	D1	D0	REG. VALUE (HEX)	DESCRIPTION
0	0	0	–	–	–	–	–		CPGA=–20dB
0	0	1	–	–	–	–	–		CPGA=–14 dB
0	1	0	–	–	–	–	–		CPGA=–8 dB
0	1	1	–	–	–	–	–		CPGA=–2 dB
1	0	0	–	–	–	–	–		CPGA=4 dB
1	0	1	–	–	–	–	–		CPGA=10 dB
1	1	0	–	–	–	–	–		CPGA=16 dB
1	1	1	–	–	–	–	–		Reserved
–	–	–	–	–	–	–	1		Bypass TX 2X interpolation 1 (see Note 7)
–	–	–	–	–	–	1	–		Bypass TX 138 kHz digital HPF (see Note 7)
–	–	–	–	–	1	–	–		Enable TX 2X interpolation 2 (see Note 7)
–	–	–	–	1	–	–	–		Bypass TX 552 kHz digital LPF 2 (see Note 7)
–	–	–	0	–	–	–	–		Select TX digital LPF1–1 (see Note 7)
–	–	–	1	–	–	–	–		Select TX digital LPF1–2 (see Note 7)

NOTE 7: [4:0] are restricted by the following setting. Performance of the codec for invalid combination of bits is not guaranteed and such combinations should not be used. Figures 8 to 14 show the data path for each combination.

TLV320AD16 Transmit

	D4	D3	D2	D1	D0	COMMENTS
OSEN =0 (default)	0	0	0	0	0	G.Lite with reduced next mode (refer to Figure 8)
	0	0	0	1	0	G.Lite with EC mode (refer to Figure 9)
	1	1	1	0	1	Full rate with reduced next mode (refer to Figure 10)
	1	1	1	1	1	Full rate with EC mode (refer to Figure 11)
OSEN =1	0	0	0	0	1	G.Lite with reduced next mode (refer to Figure 12)
	0	0	0	1	1	G.Lite with EC mode (refer to Figure 13)
	1	1	0	1	1	Full rate with EC mode (refer to Figure 14)

PROGRAMMING INFORMATION

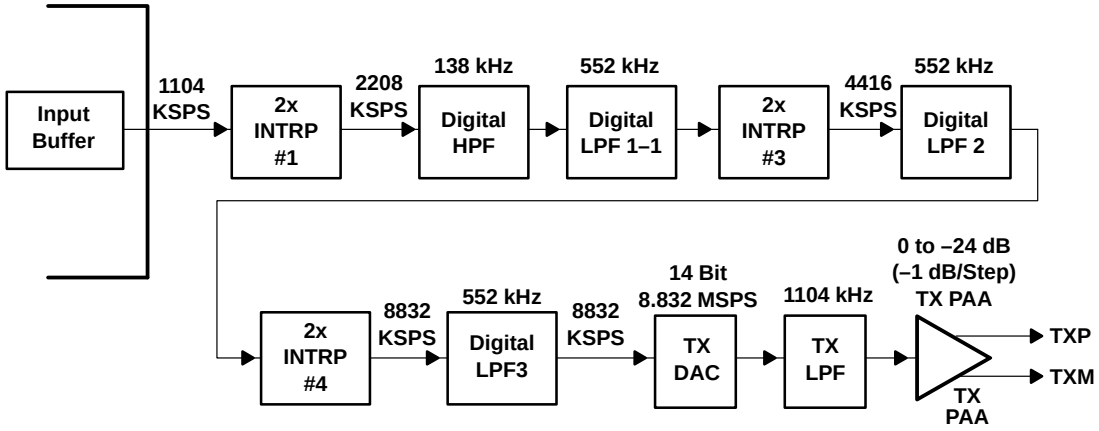


Figure 8. TLV320AD16 Transmit Block Diagram in G.Lite/Reduced NEXT Mode (SCR8[4:0]=00000 and OSEN=0, default)

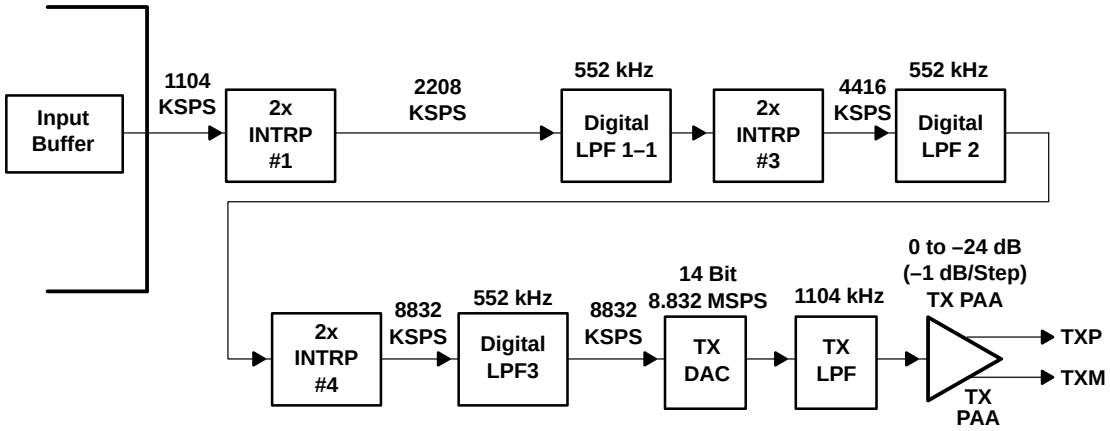


Figure 9. TLV320AD16 Transmit Block Diagram in G.Lite/EC Mode (SCR8[4:0]=00010 and OSEN=0)

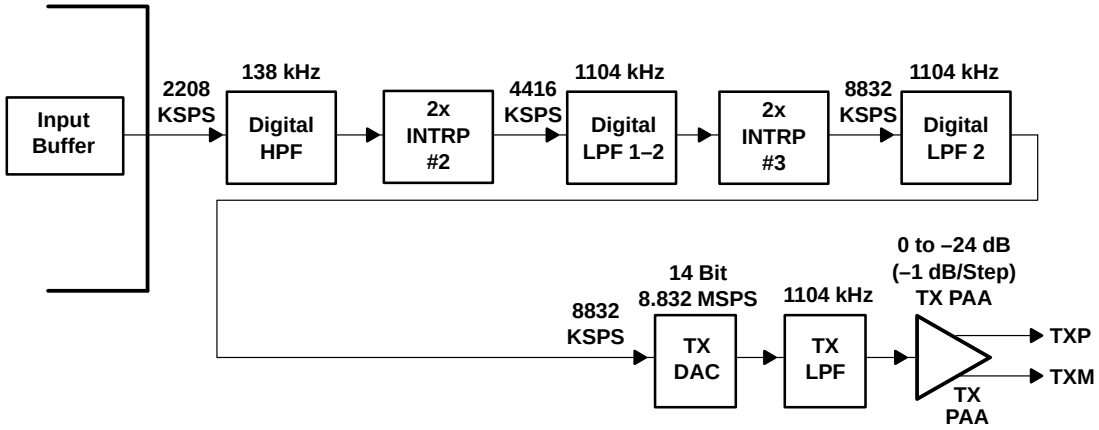


Figure 10. TLV320AD16 Transmit Block Diagram in Full/Reduced NEXT Mode (SCR8[4:0]=11101 and OSEN=0)

PROGRAMMING INFORMATION

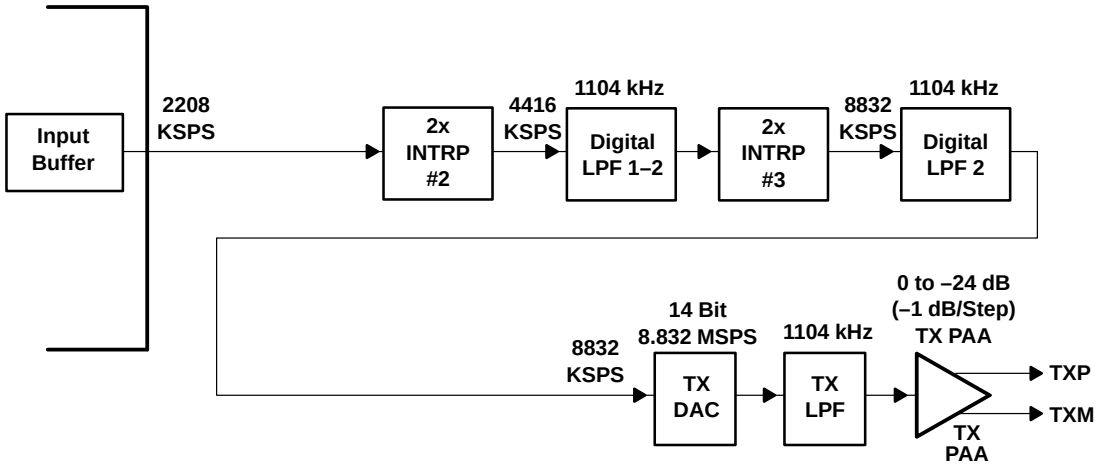


Figure 11. TLV320AD16 Transmit Block Diagram in Full/EC Mode (SCR8[4:0]=11111 and OSEN=0)

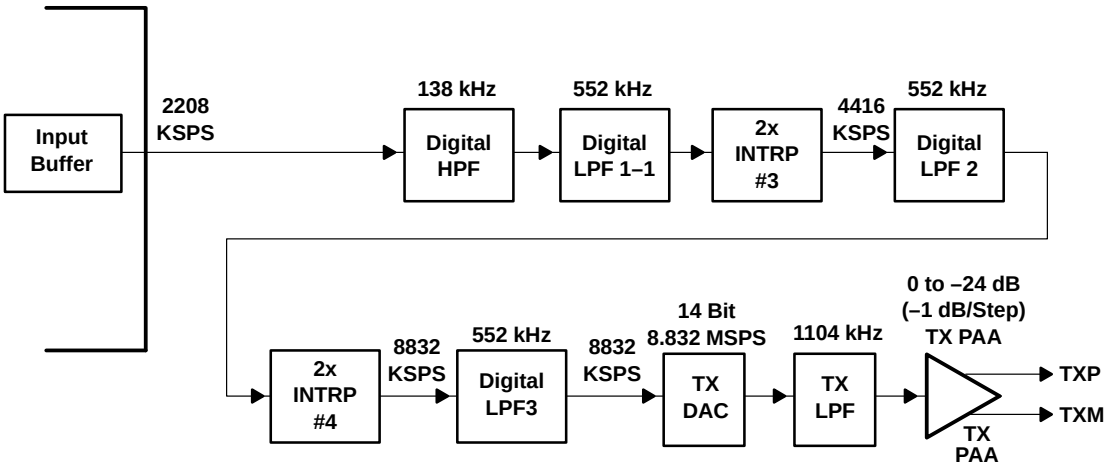


Figure 12. TLV320AD16 Transmit Block Diagram in G.Lite/Reduced NEXT Over-Sampling Mode (SCR8[4:0]=00001 and OSEN=1)

PROGRAMMING INFORMATION

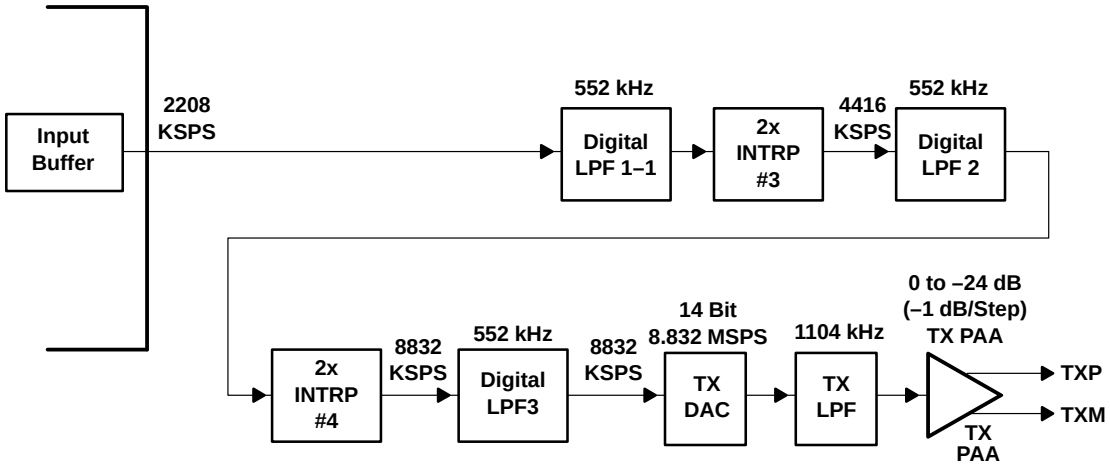


Figure 13. TLV320AD16 Transmit Block Diagram in G.Lite/EC Over-Sampling Mode (SCR8[4:0]=00011 and OSEN = 1)

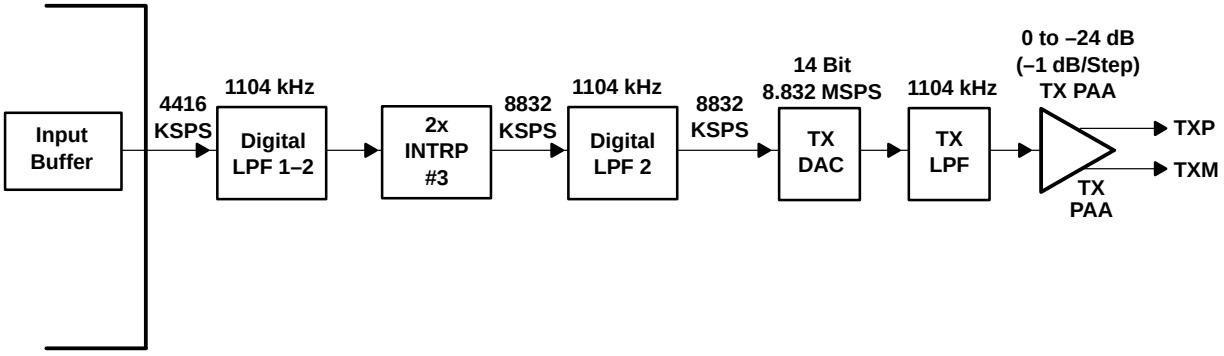


Figure 14. TLV320AD16 Transmit Block Diagram in Full/EC Over-Sampling Mode (SCR8[4:0]=11011 and OSEN=1)

PROGRAMMING INFORMATION

SCR9 – RX offset control register[7:0] Address:1001b contents at reset: 00000000b

SCR10 – RX offset control register [15:8] Address:1010b contents at reset: 00000000b

These two registers are concatenated to form a 16-bit word in 2s complement data format. The 16-bit word is used to adjust RX channel dc offset error. It adds to the 16-bit data from the RX digital filter before the data goes to RX output buffer.

SCR11 – TX gain adjustment register Address:1011b contents at reset: 00000000b

D7	D6	D5	D4	D3	D2	D1	D0	REG. VALUE (HEX)	DESCRIPTION
1	0	0	0	–	–	–	–		TX digital gain for DLPF1=–0.8 dB
1	0	0	1	–	–	–	–		TX digital gain for DLPF1=–0.7 dB
1	0	1	0	–	–	–	–		TX digital gain for DLPF1=–0.6 dB
1	0	1	1	–	–	–	–		TX digital gain for DLPF1=–0.5 dB
1	1	0	0	–	–	–	–		TX digital gain for DLPF1=–0.4 dB
1	1	0	1	–	–	–	–		TX digital gain for DLPF1=–0.3 dB
1	1	1	0	–	–	–	–		TX digital gain for DLPF1=–0.2 dB
1	1	1	1	–	–	–	–		TX digital gain for DLPF1=–0.1 dB
0	0	0	0	–	–	–	–		TX digital gain for DLPF1=0 dB (default)
0	0	0	1	–	–	–	–		TX digital gain for DLPF1=0.1 dB
0	0	1	0	–	–	–	–		TX digital gain for DLPF1=0.2 dB
0	0	1	1	–	–	–	–		TX digital gain for DLPF1=0.3 dB
0	1	0	0	–	–	–	–		TX digital gain for DLPF1=0.4 dB
0	1	0	1	–	–	–	–		TX digital gain for DLPF1=1.5 dB
0	1	1	0	–	–	–	–		TX digital gain for DLPF1=0.6 dB
0	1	1	1	–	–	–	–		TX digital gain for DLPF1=0.7 dB
–	–	–	–	1	0	0	1		TX digital gain for DLPF3=–1.4 dB
–	–	–	–	1	0	1	0		TX digital gain for DLPF3=–1.2 dB
–	–	–	–	1	0	1	1		TX digital gain for DLPF3=–1 dB
–	–	–	–	1	1	0	0		TX digital gain for DLPF3=–0.8 dB
–	–	–	–	1	1	0	1		TX digital gain for DLPF3=–0.6 dB
–	–	–	–	1	1	1	0		TX digital gain for DLPF3=–0.4 dB
–	–	–	–	1	1	1	1		TX digital gain for DLPF3=–0.2 dB
–	–	–	–	0	0	0	0		TX digital gain for DLPF3= 0 dB (default)
–	–	–	–	0	0	0	1		TX digital gain for DLPF3=0.2 dB
–	–	–	–	0	0	1	0		TX digital gain for DLPF3=0.4 dB
–	–	–	–	0	0	1	1		TX digital gain for DLPF3=0.6 dB
–	–	–	–	0	1	0	0		TX digital gain for DLPF3=0.8 dB
–	–	–	–	0	1	0	1		TX digital gain for DLPF3= 1 dB
–	–	–	–	0	1	1	0		TX digital gain for DLPF3=1.2 dB
–	–	–	–	0	1	1	1		TX digital gain for DLPF3=1.4 dB

NOTE: Digital gain is used to compensate the TX channel gain error.

PROGRAMMING INFORMATION

SCR12– RX data control register Address:1100b contents at reset: 00000000b

D7	D6	D5	D4	D3	D2	D1	D0	REG. VALUE (HEX)	DESCRIPTION (see figure15)
–	–	–	1	1	0	0	0		Sampling points A_1, A_2….. are used for RX data
–	–	–	1	1	0	0	1		Sampling points B_1, B_2….. are used for RX data
–	–	–	1	1	0	1	0		Sampling points C_1, C_2….. are used for RX data
–	–	–	1	1	0	1	1		Sampling points D_1, D_2….. are used for RX data
–	–	–	1	1	1	0	0		Sampling points E_1, E_2….. are used for RX data
–	–	–	1	1	1	0	1		Sampling points F_1, F_2….. are used for RX data
–	–	–	1	1	1	1	0		Sampling points G_1, G_2….. are used for RX data
–	–	–	1	1	1	1	1		Sampling points H_1, H_2….. are used for RX data
			1	0	–	0	0		Sampling points A_1, E_1, A_2, E_2….. are used for RX data
			1	0	–	0	1		Sampling points B_1, F_1, B_2, F_2….. are used for RX data
			1	0	–	1	0		Sampling points C_1, G_1, C_2, G_2….. are used for RX data
			1	0	–	1	1		Sampling points D_1, H_1, D_2, H_2….. are used for RX data
–	–	–	0	1	–	–	0		Sampling points A_1, C_1, E_1, G_1, A_2, C_2, E_2, G_2….. are used for RX data
–	–	–	0	1	–	–	1		Sampling points B_1, D_1, F_1, H_1, B_2, D_2, F_2, H_2….. are used for RX data
–	–	–	0	0	–	–	–		All sampling points (A_1, B_1, C_1, D_1, E_1, F_1, G_1, H_1, A_2, B_2, C_2, D_2 ,E_2, F_2, G_2, H_2…..) are used for RX data

NOTE: Performance of the codec for invalid combination of bits is not guaranteed and such combinations should not be used. The user should make no assumption that the code bits will saturate to a maximum or minimum value or wrap around to a valid combination.

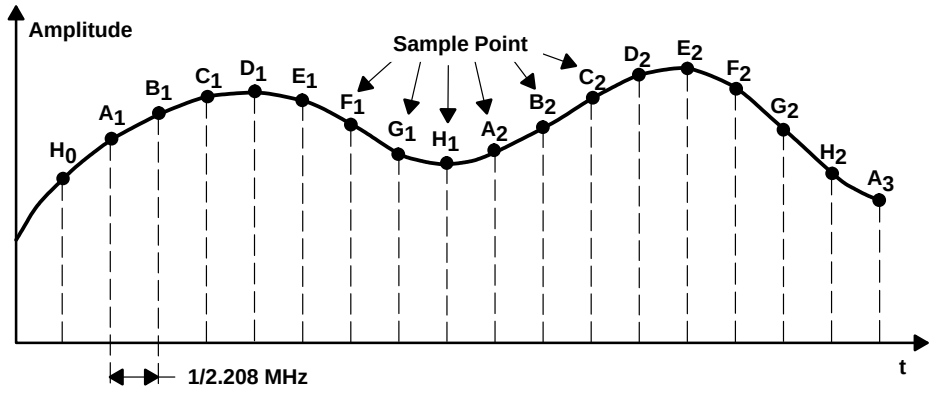


Figure 15. Input Signal Sampling

PROGRAMMING INFORMATION

ESCR0 – extended system control register
Address:0000b **Contents at reset: 00000000b**

D7	D6	D5	D4	D3	D2	D1	D0	REG. VALUE (HEX)	DESCRIPTION
0	0	0	0	0	0	0	1	01	S/W reset (self clearing) All control registers are set to reset content.
1	0	0	0	0	0	0	0	80	Extended system control register index bit. When TEST (terminal 58) is high, write 1 to SCR0[7] will enable access to ESCR. Write 0 to ESCR0[7] will enable access to SCR. (see Note 8)

NOTE 8: ESCR0 and ESCR4 will reset to the default state when the TEST terminal is set to low.

ESCR4 – loop control register (see functional block diagram)
Address:0100b **Contents at reset: 00000000b**

D7	D6	D5	D4	D3	D2	D1	D0	REG. VALUE (HEX)	DESCRIPTION
–	–	–	1	–	–	–	–		Internal bias is bypassed and external bias is enabled. A 12 μA to 15 μA dc current is needed for terminal IEXTERN.
0	0	0	–	0	0	0	0		Reserved

PRINCIPLES OF OPERATION

transmit channel

The transmit channel is powered by a high-performance DAC. This is an 8.832 MHz, 14-bit DAC that provides oversampling to reduce the DAC noise. Digital and analog low-pass filters limit the output signal bandwidth. The TX digital HPF can be bypassed by software control as shown in the functional block diagram. The programmable attenuator, with a range of 0 dB to 24 dB in –1-dB steps, drives the output into the external ADSL line driver.

receiver channel

The receiver channel has a course programmable gain amplifier (CPGA) and two high performance programmable gain amplifiers (PGA) to match the loop loss. This results in a reduction in dynamic range requirement of the 14-bit ADC. Two external series 1.4-kΩ resisters are required to implement the CPGA function (see functional block diagram). The range of the analog input signal is calculated by the following equation:

$$Vin = \frac{Vo}{10^{(A/20)}}$$

Where:

Vin = Different analog input signal range before ac-coupling to 1.4 kΩ serial resistors
Vo = Differential analog output of CPGA
A = CPGA gain setting

PRINCIPLES OF OPERATION

receiver channel (continued)

Table 3. Analog Input Range When Vo = 3 V p–p

CPGA Setting (dB)	Vin (V)
–20	30
–14	15.03
–8	7.53
–2	3.77
4	1.89
10	0.94
16	0.47

The internal ADC works at 2.280 MHz. The two LPFs (one analog and one digital) limit the input signal bandwidth to 138 kHz. The update rate of the output buffer is software programmable.

clock generation

The clock generator provides the necessary clock signals for the device. The external oscillator specifications are:

- 3.3-V supply
- 35.328 MHz, ±50 PPM
- 60/40 minimum duty cycle (50/50 is optimum)

There are three clocks generated on the device for the interface. The serial clock (SCLK) output (terminal 37), the 4.416-MHz clock (CLKOUT) output (terminal 41), and the interrupt (INT) output (terminal 40). The SCLK is used in the serial codec interface and has a fixed frequency of 4.416 MHz. The INT is used to indicate the minimum data rate requirement for the TX channel. The INT is controlled by the system control register 8 (SCR8) and the OSEN terminal. The CLKOUT is used to indicate the RX buffer update rate. The CLKOUT is controlled by the system control register 12 (SCR12) only. See Tables 4 and 5 for detail.

Table 4. Clock Description – INT (TX Data Rate)

SCR8[4]	OSEN	FREQUENCY (MHz)
0	0	1.104
0	1	2.208
1	0	2.208
1	1	4.416

Table 5. Clock Description – CLKOUT (RX Data Rate)

SCR8[4]	OSEN	FREQUENCY (MHz)
0	1	2.208
0	1	1.104
1	0	0.552
1	1	0.276

PRINCIPLES OF OPERATION

parallel interface

The device has a 16-bit parallel interface for transmitter and receiver data. The input and output buffer (see block diagram) are internally updated at a rate set by the register and hardware input terminals. The interface functions in a slave mode. The $\overline{OE}$ and $\overline{WETX}$ strobes are signal input terminals and are controlled by the external host controller. The $\overline{OE}$ is a level-triggered signal and the $\overline{WETX}$ is a edge-triggered signal. Incoming data is registered on the rising edge of $\overline{WETX}$. Output data from the codec is enabled after the $\overline{OE}$ strobe goes low and is disabled after the $\overline{OE}$ strobe goes to high. The INT and CLKOUT clocks can be used to synchronize the read and write operation, respectively.

For the 16-bit parallel data, D0 is the LSB and D15 is the MSB. The parallel TX and RX data contains 16 valid bits. All 16 bits are used in the digital filtering.

keep-out zones (for parallel interface only)

The last clock input (CLKIN) cycle before a transition of INT (works at 4.416 MHz) is defined as a keep-out zone (KOZ). This cycle lasts for one CLKIN period and has an 8.832 MHz clock rate. These zones are reserved for sampling of analog signals. The 16-bit parallel data bus should be quiet during these keep-out zones.

oversampling mode

The OSEN terminal selects a 2× oversampling mode for the TX channel. The actual TX update rate is controlled by the OSEN terminal and SCR8[4].

serial interface

The serial port is used for codec configuration and register reading. The word length is 16 bits. Two hardware-configuration terminals, ADR1 and ADR0, are used to configure the device identification (ID). Up to four codecs can be identified for each common serial port. The serial data to the SDI terminal has ADR0 and ADR1 information (see Figure 4). The codec that has the same configuration of ADR0 and ADR1 will respond to the serial data. The master codec (ADR[1:0] = 00) provides the SCLK to the host processor. The SCLK terminals on the other codecs are left unconnected. All the codecs in a multi-codec system should be synchronized by common SYNC signals so that their SCLK signals are in phase. This ensures that even though the individual codec SCLK signals are not being used the data is being latched into the codec properly. Refer to Figure 17 for details.

A host DSP can drive the FS (synchronized to the CLKOUT from codec) into the codec to initiate a 16-bit serial I/O frame.

general-purpose port (GP0 to GP7)

The GP port provides eight outputs for control of external circuitry such as LEDs, gain control, and power down. Each port can drive up to a 2-mA current. They are controlled by system control register 6 (SCR6).

PRINCIPLES OF OPERATION

voltage reference

The built-in reference provides the needed reference voltages and currents to individual analog blocks. Only decoupling capacitors are needed for each reference terminal when internal bias currents are used. See Figure 18 for detail.

The device can also use external bias current by setting D4 of the extended system control register-4 (ESCR4) to 1. In order to access ESCR4, complete the following:

- Set the TEST terminal to high
- Program the D7 of the SCR0 to 1
- Access and program the ESCR4[4] to 1

Extended system control register is programmed in the same format as the system control register. Write 0 to the ESCR0[7], this will take the device back to the normal system control register mode. Figure 16 shows a configuration using an on-chip reference voltage. A clean external current bias can improve the device performance and decrease the power consumption.

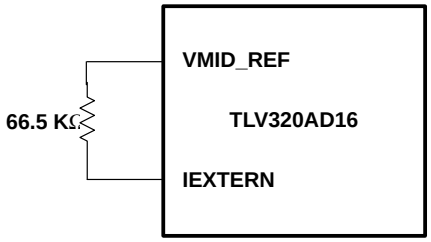


Figure 16. Bias Current Provided By On-Chip Voltage Reference

device initialization time

The TLV320AD16 will enter normal work mode 150 ms after 3 V of power has been reached or wake up from hardware power down mode. It takes 100 ms to recover from a TX or RX software shutdown. Two master clock periods (56 ns) are required to recover from hardware/software reset.

power-down mode

Both hardware and software power-down modes are provided. All of the digital interfaces and references are operative when the codec is in the software power-down mode. Only the digital interfaces are operative when the codec is in the hardware power-down mode. None of the system control registers are effected by either a hardware or software power-down. Power down of either or both the TX and RX channels can be invoked through software control. A logic 1 on the power-down (PWDN) terminal will hardware power-down the device.

multiple-channel configuration

The device is designed to have multiple-channel configuration capability. Up to four devices can be designed in a system. The parallel data bus is shared by the chip select ($\overline{CS}$) signal to each device. The serial bus is shared by the different configurations of ADR1 and ADR0 (see Figure 4) for each device. When the host device sends a control command signal through the serial bus, the ADR1 and ADR0 are decoded by each codec. Only the corresponding codec has control of the serial bus. All SYNC pins should be connected together. The host device will send a pulse to all codecs to synchronize the operation. The serial clock in the serial codec interface has a fixed frequency of 4.416 MHz. Refer to Figure 17 for the configuration.

PRINCIPLES OF OPERATION

power supply grouping recommendation

The following power supply grouping is recommended for the best performance of the device. Ferrite beads are used to separate group 1, group 2, and group 3 if the same 3.3-V analog power source is shared.

- Group1: AVDD_DAC1_TX, AVDD_DAC2_TX, AVDD_FIL_TX
- Group2: AVDD_FIL_RX, AVDD_ADC
- Group3: AVDD_REF
- Group4: DVDD_BF, DVDD_CLK, DVDD_DAC, DVDD_LG, DVDD_RX

PRINCIPLES OF OPERATION

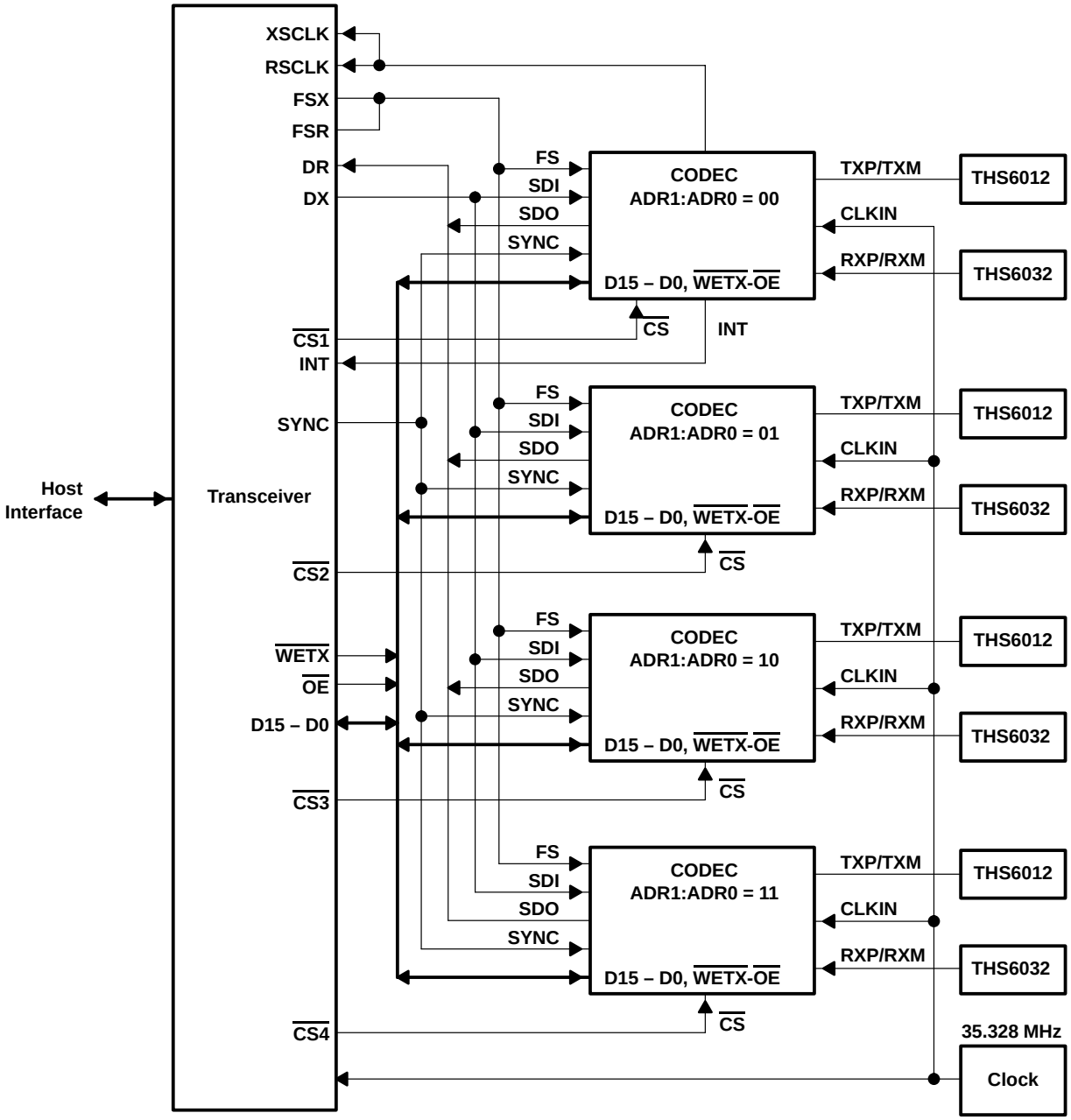
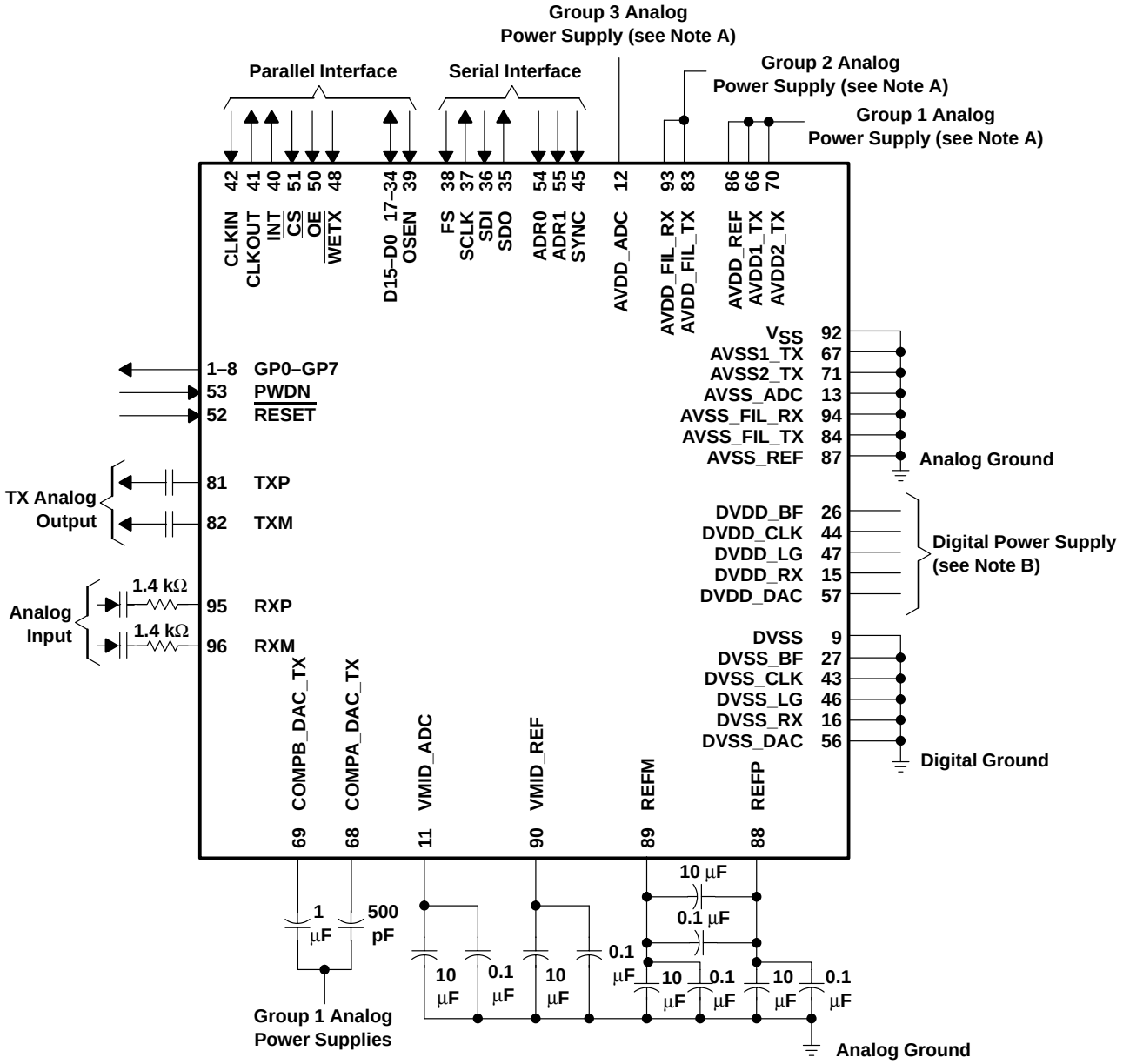


Figure 17. TLV320AD16 Multichannel Codec Configuration

PRINCIPLES OF OPERATION



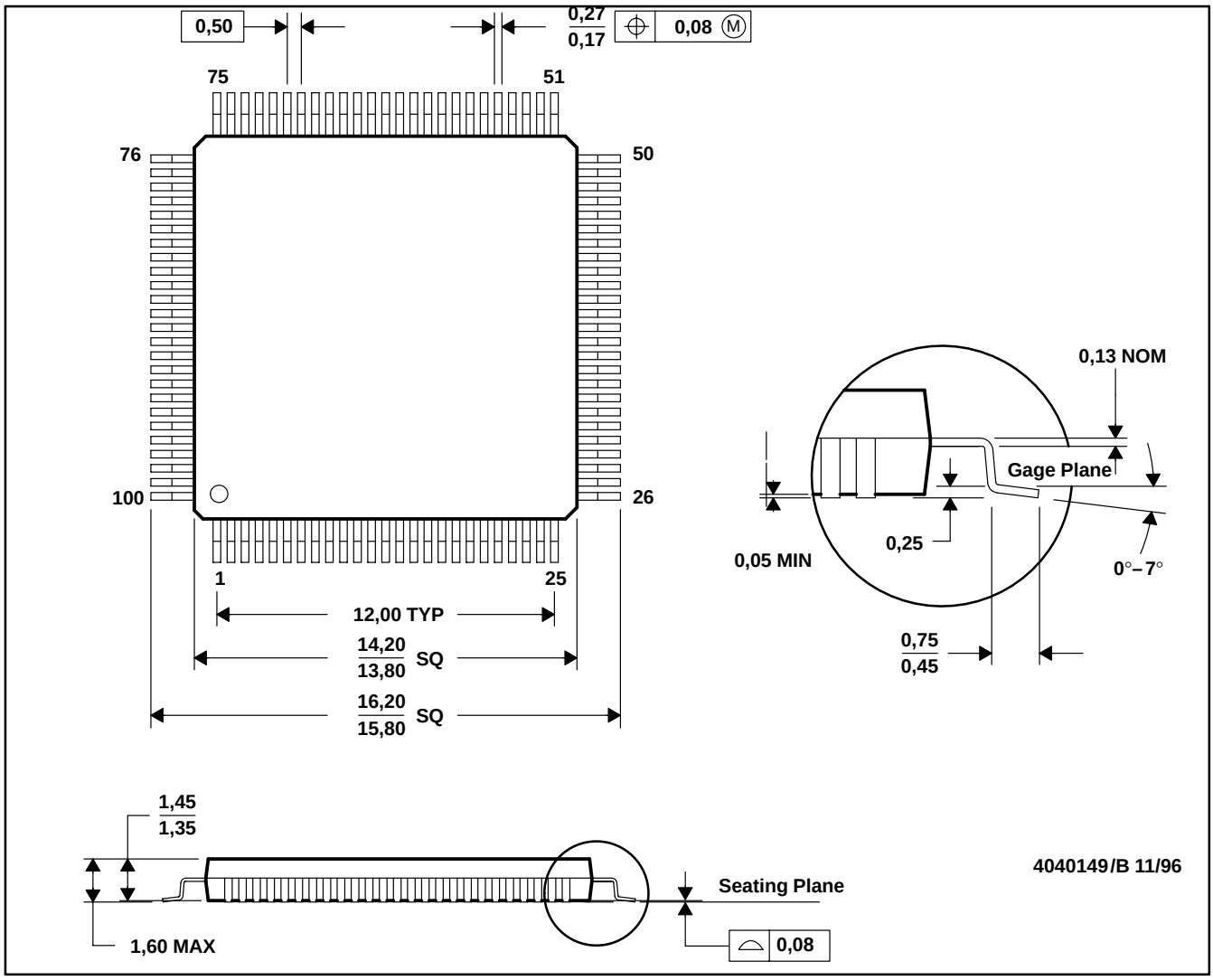
NOTES: A. A 10-µF type and a 0.1-µF X7R ceramic capacitor are needed for all analog power supplies. Each pair of bypass-capacitors are connected to the corresponding analog ground. Refer to the Terminal Functions table for detail.

B. A 10-µF type and a 0.1-µF X7R ceramic capacitor are needed for all analog power supplies. Each pair of bypass-capacitors are connected to the corresponding digital power supply. Refer to the Terminal Functions table for detail.

Figure 18. Typical Chip Configuration

MECHANICAL DATA

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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