National Semiconductor

PRELIMINARY

NMC41257 262,144 x 1-Bit Dynamic RAM

General Description

The NMC41257 is a 262,144 words by 1-bit new generation dynamic RAM. It is fabricated with National's proprietary N-channel triple-polysilicon technology which combines high performance and high density with improved reliability and excellent alpha radiation tolerance.

The NMC41257 is designed to operate with a single +5V power supply with ±10% tolerance. The use of a single transistor memory cell and advanced dynamic circuitry enable it to achieve high speeds with low power consumption.

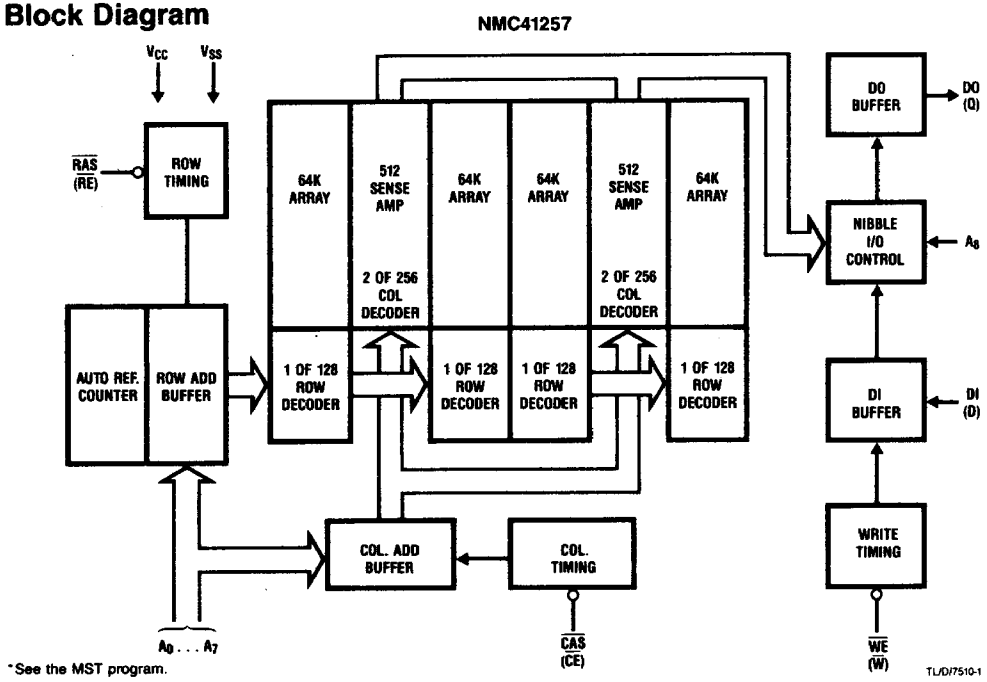
Multiplexed address inputs with separate row and column strobes allow the NMC41257 to be packaged in a standard 16-pin DIP. It is available in both plastic and cerdip packages.

The NMC41257 must be refreshed every 4 ms. This is accomplished by performing any cycle which brings the row address strobe ($\overline{RAS}$) active at each of the 256 row addresses. Thus any read, write, $\overline{RAS}$-only refresh or hidden refresh cycle refreshes all cells at the selected row address. The $\overline{RAS}$-only refresh mode permits the $\overline{RAS}$ to be cycled while the column address strobe ($\overline{CAS}$) is held high, i.e., inactive. In this mode, addresses A0–A7 select the row that is refreshed. In addition, a $\overline{CAS}$ before $\overline{RAS}$ automatic refresh is provided. When $\overline{RAS}$ goes low after $\overline{CAS}$ has been low (by t_{CSR}), the internal refresh counter is activated to generate the addresses to be refreshed. In this mode all address inputs are ignored by the device. A nibble mode is also provided allowing the serial access of 4 bits of data at a very high data rate. Nibble mode address is controlled by the addresses supplied to pin 1 (A8 — Row and Column).

Features

- High performance: 100, 120, 150 ns access time
- Single power supply: 5V ±10%
- Low power: 22 mW (max) standby
  412 mW (max) active
- Wide $\overline{RAS}$ to $\overline{CAS}$ delay windows
- Read, Write and Read-Modify-Write cycles
- Common I/O capability using Early Write cycle
- $\overline{RAS}$-only Refresh and Hidden Refresh capability
- Automatic $\overline{CAS}$ before $\overline{RAS}$ refresh mode
- 256 cycle, 4 ms refresh
- TTL compatible: all inputs and output
- Industry standard 16-pin configuration
- TRI-STATE® output
- Fast nibble mode on either read or write cycles
  — 20 ns access (41257-10)
  — 40 ns cycle (41257-10)
- MST™ screen available*

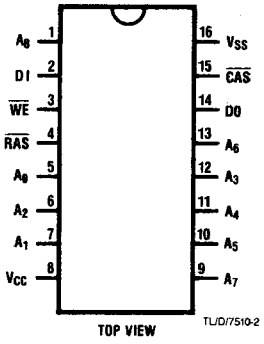
Block Diagram



*See the MST program.

Connection Diagram

Dual-In-Line Package



NS Package Number N16A

Pin Names

$\overline{RAS}$ ($\overline{RE}$) Row Address Strobe
$\overline{CAS}$ ($\overline{CE}$) Column Address Strobe
$\overline{WE}$ ($\overline{W}$) Write Enable
A_0–A_8 Address Inputs
DI (D) Data Input
DO (Q) Data Output
V_{CC} Power (5V)
V_{SS} Ground

Absolute Maximum Ratings (Note 1)

Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation	1 Watt
Voltage on Any Pin Relative to V_{SS}	−1.0V to +7V
Lead Temperature (Soldering, 10 seconds)	300°C

Device	NMC 41257-10	NMC 41257-12	NMC 41257-15
t_{RAC} (ns, Max)	100	120	150
t_{CAC} (ns, Max)	50	60	75
t_{RC} (ns, Min)	200	230	280
I_{CC1} (mA, Max)	75	75	75
I_{CC2} (mA, Max)	4	4	4

Recommended DC Operating Conditions

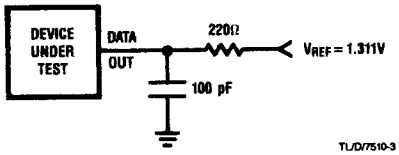
Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature	0	70	°C
V_{CC}	Supply Voltages (Notes 2 and 3)	4.5	5.5	V
V_{SS}	Supply Voltages (Notes 2 and 3)	0	0	V
V_{IH}	Input High Voltage, All Inputs (Note 2)	2.4	V_{CC} + 1.0	V
V_{IL}	Input Low Voltage, All Inputs (Note 2)	−1.0	0.8	V

DC Electrical Characteristics (at recommended operating conditions)

Symbol	Parameter	Min	Max	Units
I_{CC1}	Operating Current Average Power Supply Operating Current (Note 4) ($\overline{RAS}$, $\overline{CAS}$ Cycling, $t_{RC} = t_{RC\ MIN}$)		75	mA
I_{CC2}	Standby Current Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$, DO = High Impedance)		4	mA
I_{CC3}	Refresh Current (RAS only) Average Power Supply Current, Refresh Mode (Note 4) ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC\ MIN}$)		50	mA
I_{CC4}	Refresh Current (automatic $\overline{CAS}$ before $\overline{RAS}$) Average Power Supply Current, Refresh Mode (Note 4) $\overline{CAS} = V_{IL}$, $\overline{RAS}$ Cycling, $t_{RC} = t_{RC\ MIN}$)		50	mA
I_I	Input Leakage Input Leakage Current, Any Input (0V < V_{IN} < V_{CC}, All Other Pins not Under Test = 0V)	−10	10	μA
I_{OZ}	Output Leakage Output Leakage Current (D_0 is Disabled, 0V < V_{OUT} < V_{CC})	−10	10	μA
V_{OH} V_{OL}	Output Levels Output High Voltage (I_{OUT} = −5 mA) Output Low Voltage (I_{OUT} = 4.2 mA)	2.4 0	V_{CC} 0.4	V V

AC Testing Conditions

1. Data Out Load



2. Input Levels

V_{IL} (Max)	0.8V
V_{IH} (Min)	2.4V

3. Output Levels

V_{OL}	0.4V	I_{OL} = 4.2 mA
V_{OH}	2.4V	I_{OL} = −5.0 mA

4. Transition times are measured between 0.8V (V_{IL} Max) and 2.4V (V_{IH} Min). Rise and fall times are 5 ns.

Capacitance

Symbol	Parameter	Max	Units
CI	Input Capacitance, A0–A8, DI (Note 5)	5	pF
CC	Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ (Note 5)	10	pF
CO	Output Capacitance, DO (Note 5)	7	pF

AC Electrical Characteristics (at recommended operating conditions) (Notes 2, 6, 7, and 8)

Symbol	Parameter	NMC41257-10		NMC41257-12		NMC41257-15		Units
		Min	Max	Min	Max	Min	Max	
READ, WRITE CYCLES								
t_{RAC}	Access Time from $\overline{RAS}$ (Notes 11, 12)		100		120		150	ns
t_{CAC}	Access Time from $\overline{CAS}$ (Notes 11, 13)		50		60		75	ns
t_{RP}	$\overline{RAS}$ Precharge Time	90		100		120		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	100	10k	120	10k	150	10k	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	50		60		75		ns
t_{RC}	Random Read or Write Cycle Time	200		230		280		ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time (Note 9)	20	50	25	60	25	75	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10		10		ns
t_{RSH}	$\overline{RAS}$ Hold Time	50		60		75		ns
t_{CSH}	$\overline{CAS}$ Hold Time	100		120		150		ns
t_{ASR}	Row Address Set-Up Time	0		0		0		ns
t_{RAH}	Row Address Hold Time	15		20		20		ns
t_{ASC}	Column Address Set-Up Time	0		0		0		ns
t_{CAH}	Column Address Hold Time	25		30		30		ns
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	75		90		105		ns
t_{RCS}	Read Command Set-Up Time	0		0		0		ns
t_{RCH}	Read Command Hold Time (Note 10)	0		0		0		ns
t_{OFF}	Output Buffer Turn-Off Delay (Note 14)		20		25		25	ns
t_{WP}	Write Command Pulse Width	20		25		30		ns
t_{WCS}	$\overline{WE}$ to $\overline{CAS}$ Set-Up Time (Note 15)	0		0		0		ns
t_{WCH}	Write Command Hold Time	20		25		30		ns
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	95		100		120		ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	40		45		45		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	40		45		45		ns
t_{DS}	Data-In Set-Up Time	0		0		0		ns

AC Electrical Characteristics (Continued)

Symbol	Parameter	NMC41257-10		NMC41257-12		NMC41257-15		Units
		Min	Max	Min	Max	Min	Max	
t_{DH}	Data-In Hold Time	20		25		30		ns
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	85		100		120		ns
t_T	Transition Time (Rise and Fall) (Note 7)	3	50	3	50	3	50	ns
t_{REF}	Refresh Period		4		4		4	ms
READ-MODIFY-WRITE CYCLES								
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	100		120		150		ns
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay (Note 15)	50		60		75		ns
t_{RWC}	Read-Write-Cycle Time	245		280		330		ns
t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	145	10k	170	10k	205	10k	ns
t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	95		110		130		ns
REFRESH CYCLE								
t_{CSR}	Column Address Strobe Setup Time for Auto Refresh	10		10		10		ns
t_{CHR}	Column Address Strobe Hold Time for Auto Refresh	30		30		30		ns
t_{RPC}	Precharge to $\overline{CAS}$ Active Time	0		0		0		ns
NIBBLE MODE CYCLE								
t_{NC}	Nibble Mode Cycle Time	40		50		60		ns
t_{NAC}	Nibble Mode Access Time	20		25		30		ns
t_{NAS}	Nibble Mode Setup Time	20		25		30		ns
t_{NP}	Nibble Mode Precharge Time	10		15		20		ns
t_{NRSH}	Nibble Mode $\overline{RAS}$ Hold Time	20		25		30		ns
t_{NCWD}	Nibble Mode $\overline{CAS}$ to WRITE Delay	20		25		30		ns
t_{NCRW}	Nibble Mode RMW $\overline{CAS}$ Pulse Width	45		55		65		ns
t_{NCWL}	Nibble Mode WRITE to $\overline{CAS}$ Lead Time	20		25		30		ns
AUTO REFRESH COUNTER TEST MODE								
t_{RTC}	Refresh Counter Test Cycle Time (Note 16)	360		410		500		
t_{TRAS}	Refresh Counter Test $\overline{RAS}$ Pulse and Width (Note 16)	260	10k	300	10k	360	10k	
t_{CPT}	Refresh Counter Test $\overline{CAS}$ Precharge Time (Note 16)	50		60		70		

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the device should be operated at these limits. The table of "Recommended DC Operating Conditions" provides conditions for actual device operation.

Note 2: All voltages referenced to V_{SS}.

Note 3: When applying voltages to the device. V_{CC} should never be 1.0V more negative than V_{SS}.

Note 4: I_{CC1}, I_{CC3}, and I_{CC4} depend on cycle rate measured with output open.

Note 5: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\,\Delta t/\Delta V$ with the recommended DC operating conditions applied to the device. Capacitance is guaranteed by periodic testing.

Note 6: Any 8 cycles that perform refresh must be applied following either power on or periods of no row address strobe activity exceeding 4 ms.

Note 7: Transition times are assumed to be 5 ns.

Note 8: Timing reference points are V_{IH} (min) and V_{IL} (max).

Note 9: If t_{RCD} (min) $< t_{RCD} < t_{RCD}$ (max) the access time is t_{RAC} (row timing limited). If the t_{RCD} exceeds t_{RCD} (max) the access time is t_{RCD} plus t_{CAC} (column timing limited). If -10 ns $< t_{RCD} < t_{RCD}$ (min) the cycle is indeterminate.

Note 10: t_{RCH} is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.

Note 11: See AC Testing Conditions for output load.

Note 12: Assumes $t_{RCD} < t_{RCD}$ (max) (row limited timing).

Note 13: Assumes $t_{RCD} > t_{RCD}$ (max) (column limited timing).

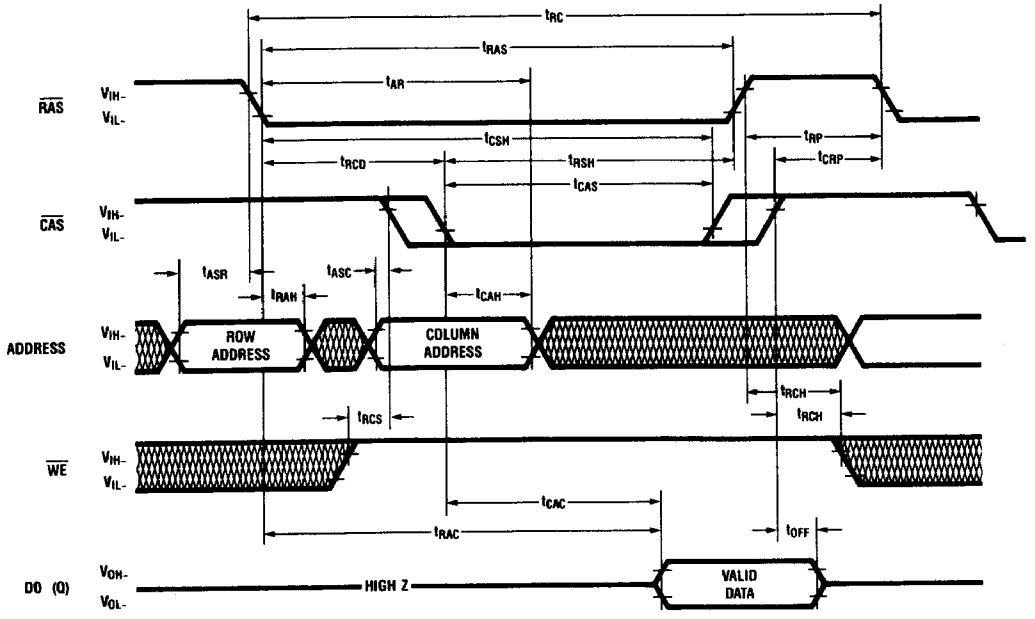
Note 14: t_{OFF} max defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Note 15: The placement of the negative going edge of $\overline{WE}$ with respect to the negative edge of $\overline{CAS}$ determines the type of write cycle. If t_{WCS} is greater than 0 ns (negative edge of $\overline{WE}$ before the negative edge of $\overline{CAS}$) the memory is in an early write cycle and data out is TRI-STATE. If t_{CWD} is greater than t_{CWD} (min) the memory is in a read-write or read-modify-write cycle and data out is the original contents of the selected cell. If $\overline{WE}$ goes low between these two times the cycle is a write cycle and data out is indeterminate.

Note 16: Read-modify-write cycle only.

Switching Time Waveforms

Read Cycle Timing



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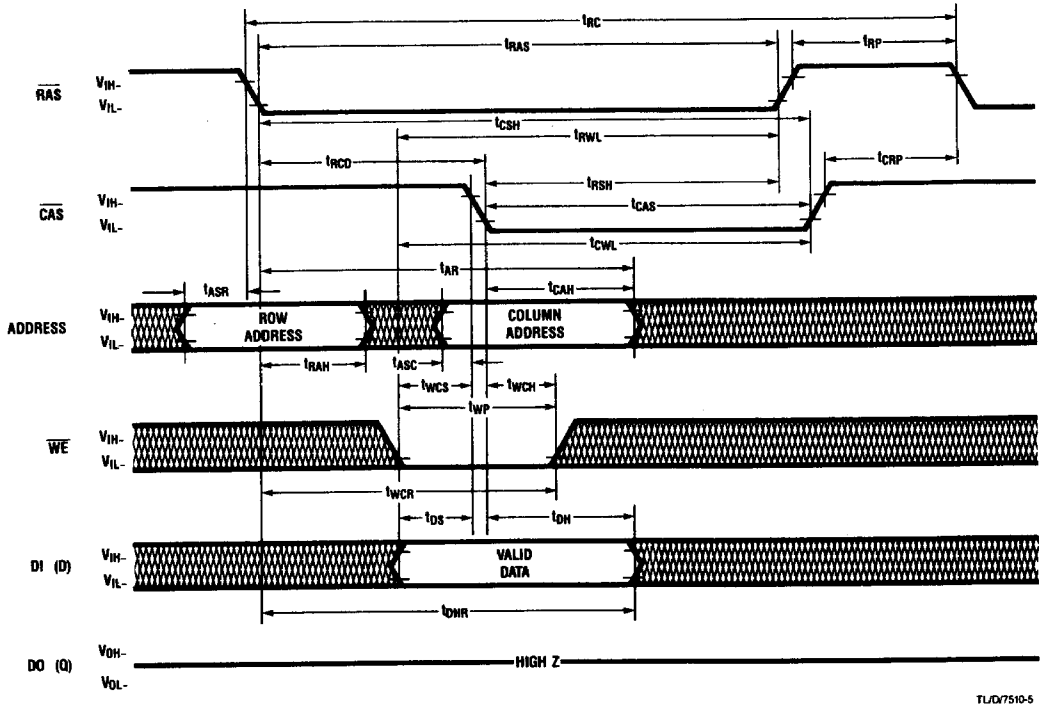
Early Write Cycle



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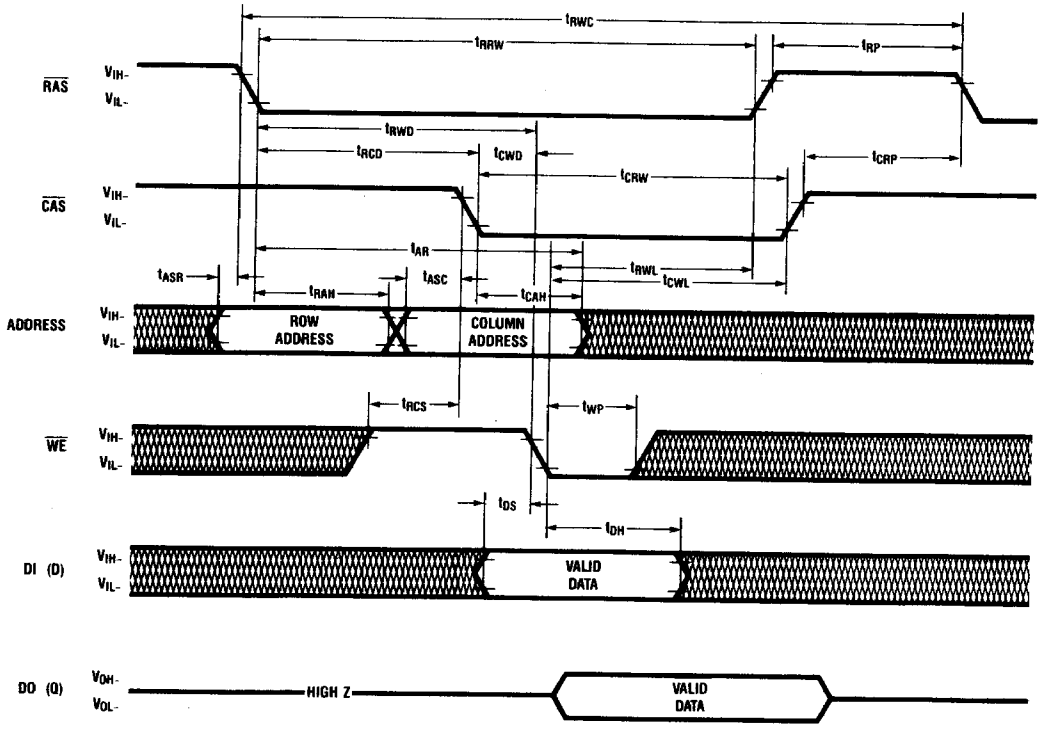
Switching Time Waveforms (Continued)

Read-Modify-Write or Late Write Cycle



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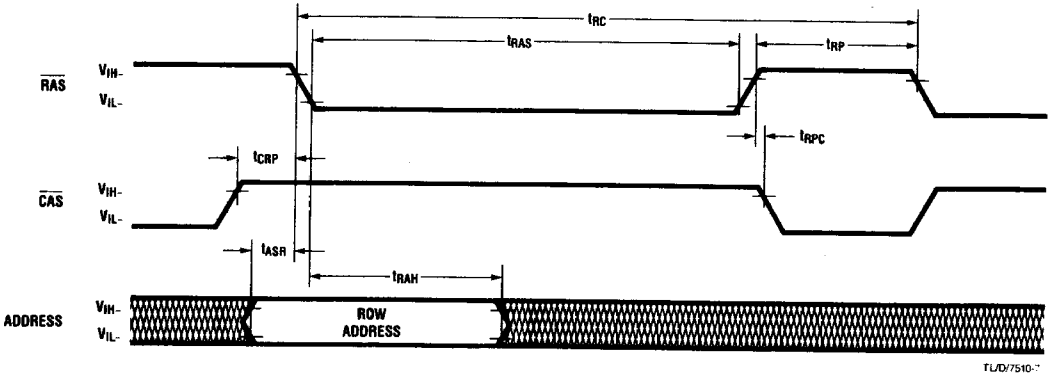
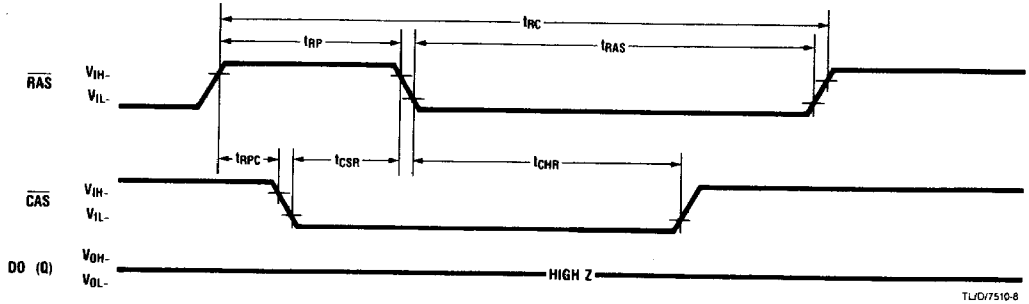
RAS Only Refresh Cycle (Data-in and Write are Don't Care)



TL/D/7510-7

Automatic (CAS Before RAS) Refresh Cycle



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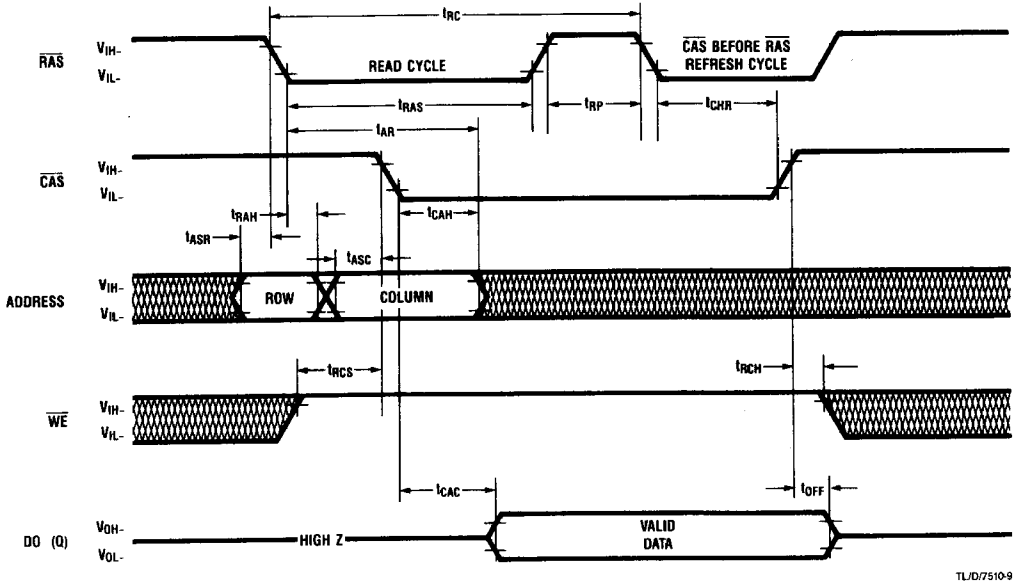
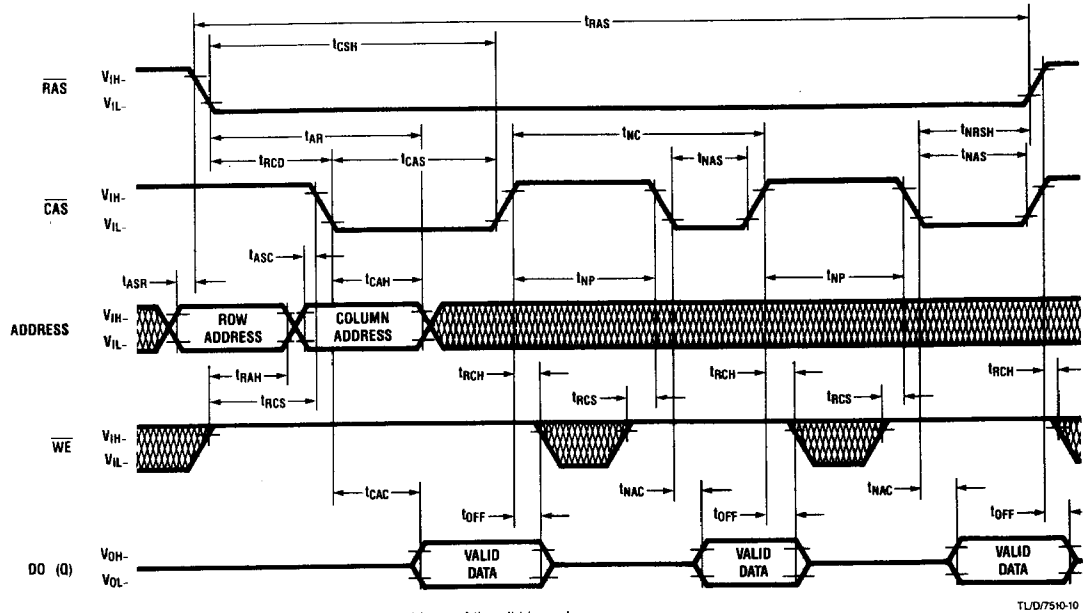
Switching Time Waveforms (Continued)

Hidden Refresh Cycle



TL/D/7510-9

Nibble Mode Read Cycle*



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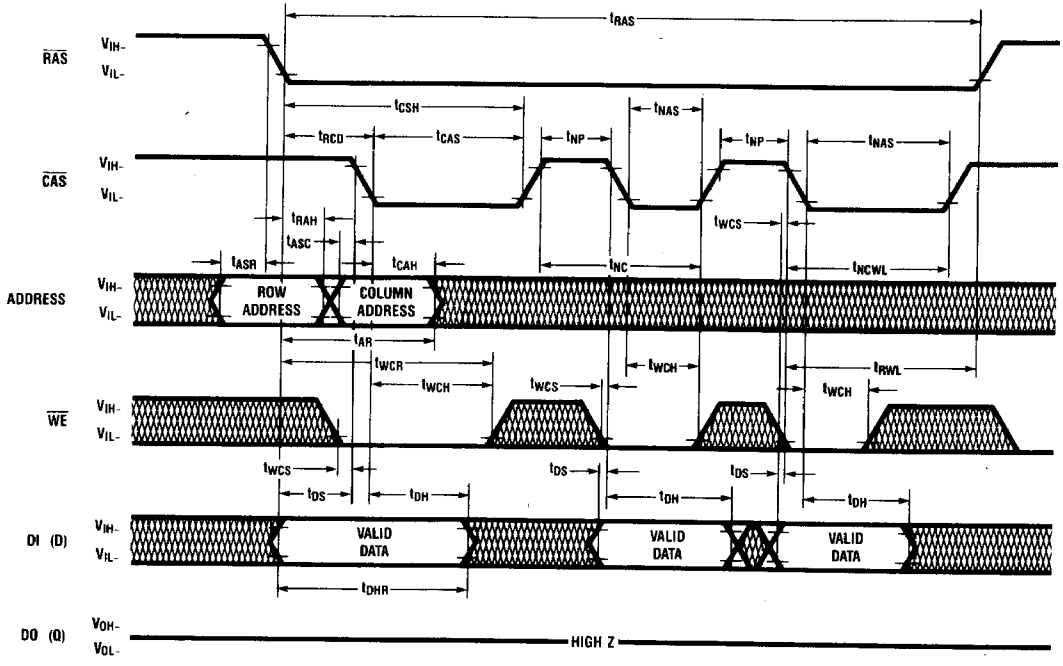
*Pin 1 at row time and column time determine the starting address of the nibble cycle.

Switching Time Waveforms (Continued)

Nibble Mode Write Cycle (Early Write)



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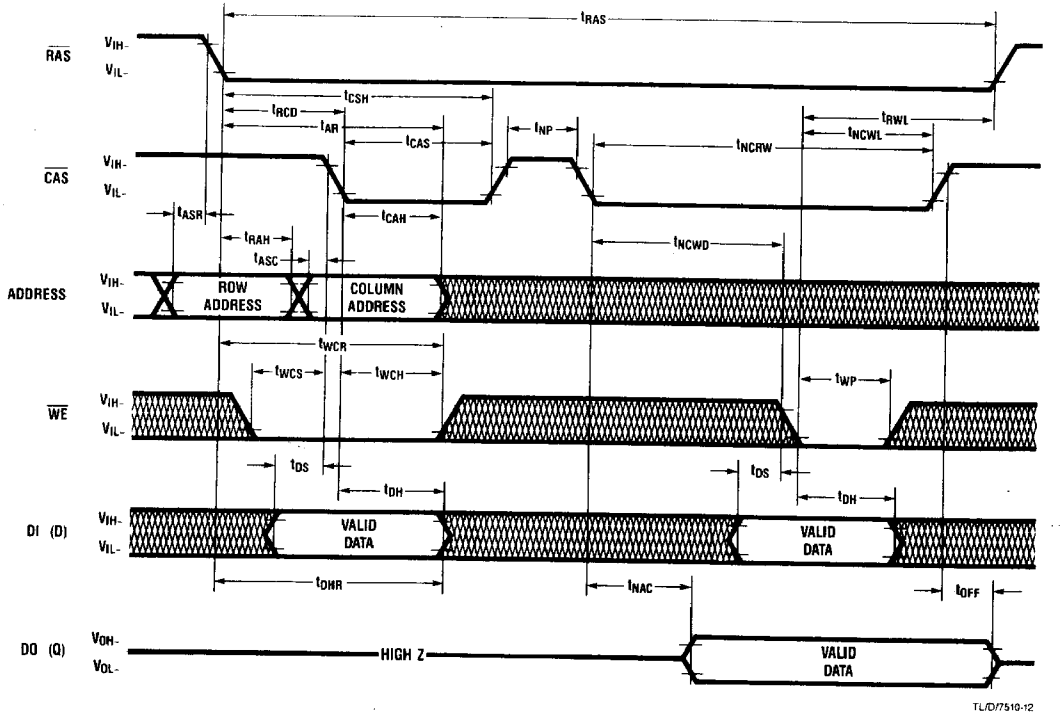
Nibble Mode Read-Modify-Write



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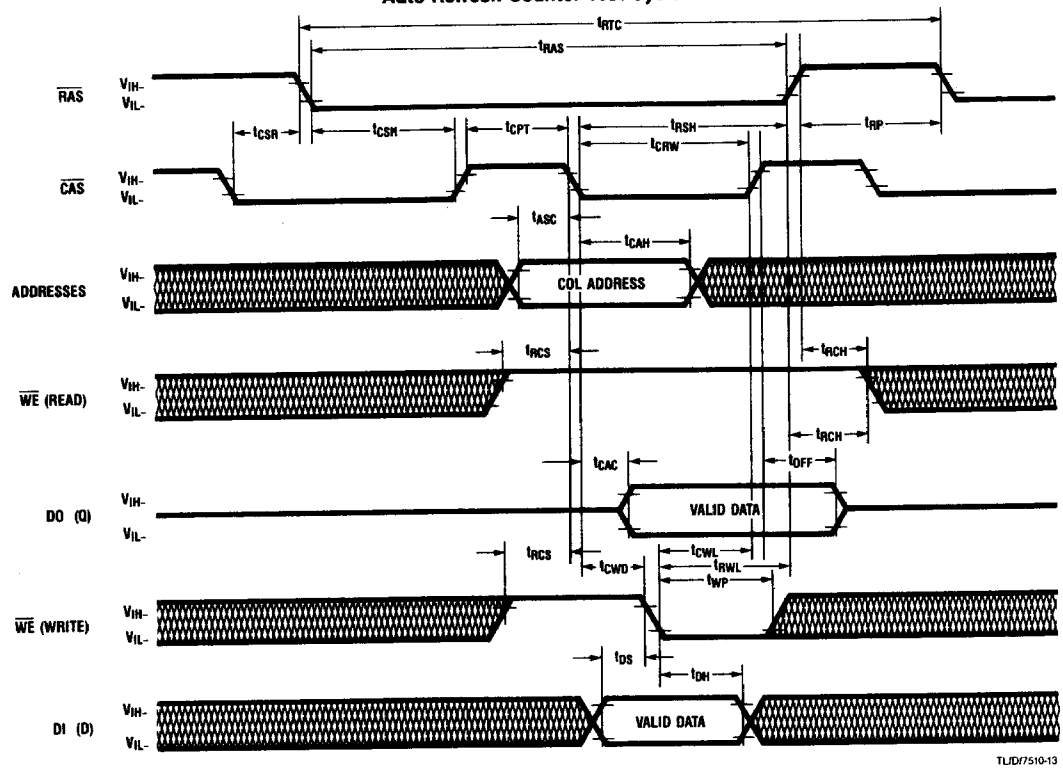
Switching Time Waveforms (Continued)

Auto Refresh Counter Test Cycle



TL/D/7510-13

Functional Description

Device Initialization: The 256K dynamic RAM requires a single +5V supply. After power up an initial 100 microsecond pause is required to allow an internal substrate pump to establish the correct substrate bias. After this pause a minimum of 8 cycles of Row Address Strobe ($\overline{RAS}$) clock must be given to the part to allow the internal dynamic circuitry to reach proper levels. Upon completion of the initialization sequence the part will be ready to operate in accordance with these specifications.

Address Inputs: Eighteen binary address inputs are required to address any one of 262,144 bits in this DRAM. These addresses are multiplexed and strobed into the part in two groups of 9 addresses by the negative going edge of the Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$) clocks. The delay interval between these two clocks (t_{RCD}) describes the minimum time at which the column addresses may follow the row addresses for good device performance and the maximum time at which the column addresses may follow the row addresses before the Access Time (t_{RAC}) will begin to increase beyond the specification.

Reading Data: A read cycle begins by presenting a valid row address to the address inputs and bringing the $\overline{RAS}$ input from V_{IH} to V_{IL}. This causes the row addresses to be latched into the part. This is followed by presenting a valid column address to the address inputs and bringing the $\overline{CAS}$ input from V_{IH} to V_{IL} at which time the column addresses are latched in. If the $\overline{CAS}$ input transition is made before the t_{RCD} maximum time then valid data will appear on data out in time to meet the t_{RAC} specification. If the $\overline{CAS}$ input transition is made after the t_{RCD} maximum time data out will be valid in time to meet the t_{CAC} specification. The external $\overline{CAS}$ signal may become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the TRI-STATE mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{WE}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

Writing Data: The write cycle is similar to the read cycle except the Write Enable ($\overline{WE}$) clock must be at V_{IL} during the time $\overline{CAS}$ is active. If the $\overline{WE}$ transition is done before the minimum t_{WCS} time, the cycle will be an early write cycle (data out remains in TRI-STATE). If $\overline{WE}$ makes a transition after t_{CWD} minimum time, the cycle will be a read-modify-

Functional Description (Continued)

write cycle. If $\overline{WE}$ makes a transition between t_{WCS} and t_{CWD} time, then the type of cycle is indeterminate.

Data is supplied to the data in input and is latched in with Write Enable ($\overline{WE}$) in the same manner as the addresses are with $\overline{RAS}$ and $\overline{CAS}$ provided the $\overline{WE}$ transition is made after the $\overline{CAS}$ transition. If the $\overline{WE}$ transition is made before the $\overline{CAS}$ transition, then the data is latched by the $\overline{CAS}$ transition.

The Read-Modify-Write Cycle: This type of cycle allows the user to both read and write a single bit in memory during the same cycle.

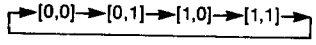
For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{WE}$) clock at the V_{IH} level until after the t_{CWD} time has elapsed. At this time the write ($\overline{WE}$) clock is asserted. The data in is set up and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Refreshing the DRAM: The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 4 ms. This is accomplished by sequentially cycling through the 256 row address locations every 4 ms. These row addresses are controlled by address inputs A0 through A7. A normal read or write operation to the RAM will serve to refresh all the bits (1024) associated with that particular row decoded.

For $\overline{RAS}$-Only Refresh type cycle the memory component is in standby. In this refresh method, the user must perform a $\overline{RAS}$-only cycle on all 256 row addresses every 4 ms. The row addresses (A0–A7) are latched with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and should be inactive or at a V_{IH} level to conserve power.

For a $\overline{CAS}$ before $\overline{RAS}$ refresh (auto refresh) type cycle $\overline{RAS}$ falls after $\overline{CAS}$ has been low by t_{CSR}. This activates the internal refresh counter which generates the address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by $\overline{CAS}$ in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as $\overline{CAS}$ is held active (hidden refresh).

The Nibble Mode Cycle: Nibble Mode Operation allows faster successive data operation on 4 bits. The first bit is accessed in the usual manner with read data coming out at t_{CAC} time. By keeping $\overline{RAS}$ low, $\overline{CAS}$ can be cycled up and then down, to read or write the next three bits at a high data rate (t_{NAC}). Row and column addresses need only be supplied for the first access of the cycle. From then on, the falling edge of $\overline{CAS}$ will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around method).



Pin one (A8) determines the starting point of the circular 4-bit nibble. Row A8 and Column A8 provide the two binary bits needed to select one of four bits. From then on, successive bits come out in a binary fashion; 00→01→10→11 with A8 row being the least significant address.

A nibble cycle can be a read, write, or late write cycle. Any combinations of reads and writes or late writes will be allowed. In addition, the circular wrap-around will continue for as long as $\overline{RAS}$ is kept low.