ML6686

Intelligent Token Ring Physical Interface

GENERAL DESCRIPTION

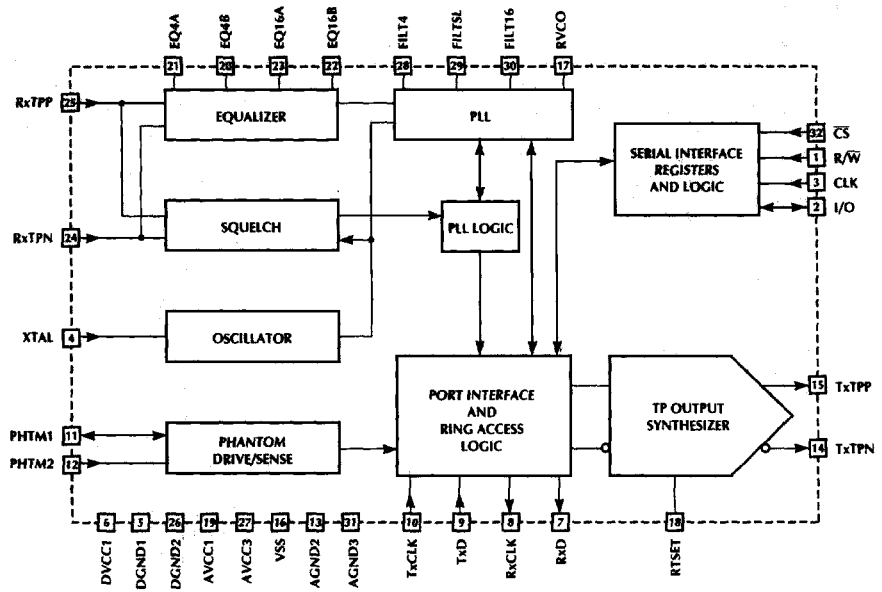
The ML6686 Token Ring Physical Interface Circuit is designed for ISO/IEC 8802-5 networks using unshielded twisted pair (UTP) or shielded twisted pair (STP) media. ML6686 is intended for hub/concentrator applications. The ML6686 includes a receiver equalizer, two PLLs, a FIFO with user selectable length between 0, 2, 4, or 8 UI, internal frequency/phase tracking select logic, and current driven twisted pair transmit driver and receiver. The first PLL uses a single edge constant-gain phase/frequency detector for enhanced clock tracking and low VCO output phase distortion and the second PLL filters jitter. The circuit also includes phantom wire fault detection and output drivers for use with an external phantom switching mechanism.

A 4-line serial interface, compatible with Intel MCS®-51 family of microcontrollers, is used to access all control and status bits. The control bits default to values that allow the ML6686 to operate without a MAC controller as Lobe ports. The defaults are set to 16Mbps data rate, with 2 PLL retiming, and a 8 UI FIFO.

FEATURES

- Supports dual PLL jitter attenuator and clock regeneration for each lobe port and Ring-In/Ring-Out ports for UTP/STP extended distance concentrators.
- 4-line serial microcontroller interface for management of control and status.
- Compatible with ISO/IEC 8802-5-1989 and the emerging 802.5q Standard for Token Ring.
- 16 and 4 Mbps data rates selectable through control bit.
- Supports dual ring fault tolerant Ring-In/ Ring-Out trunks.
- Fault isolation capability at each concentrator port available for network management.
- Provides dual phase-locked loops with single edge constant gain phase detector and selectable length FIFO for clock regeneration, jitter attenuation, and data recovery.
- Several programmable retiming options.
- Serial interface for Status and Control bits.
- On-chip receiver channel equalization switchable for both 4 and 16 Mbps.

BLOCK DIAGRAM

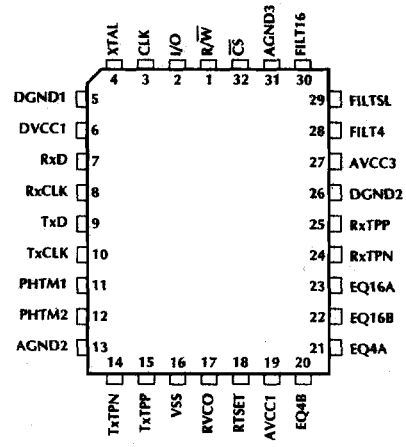


GENERAL DESCRIPTION (Continued)

External components are minimized by the use of internally-controlled station fault, receiver pulse width squelch, and internal 4/16 Mbps switching logic. In a concentrator application the ML6686 performs the switching function eliminating the need for relays. Isolation can be achieved optically. The circuit requires a single +5V power supply, and is fabricated in BiCMOS technology.

PIN CONFIGURATION

ML6686
32-Pin PLCC (Q32)



PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	R/$\overline{W}$	Read/write bar. The state of this input, while $\overline{CS}$ is low, allows either reading from the Status register, R/$\overline{W}$ = 1, or writing to the Control register, R/$\overline{W}$ = 0. This input should not change state until the read or write operation is completed. For $\overline{CS}$ = 1, R/$\overline{W}$ is a don't care.
2	I/O	Input to Control register or, output from Status register. When $\overline{CS}$ = 0 and R/$\overline{W}$ = 1, I/O is an output from the Status register. When $\overline{CS}$ = 0 and R/$\overline{W}$ = 0, I/O is an input to the control register. When $\overline{CS}$ = 1, I/O is in a high-impedance state.
3	CLK	Clock input from the controller. For R/$\overline{W}$ = 1, the ML6686 presents a new bit from the Status register at the I/O pin, beginning on the LSB, on every falling edge of CLK following $\overline{CS}$ going low. The controller reads the bits on the rising edges of CLK. For R/$\overline{W}$ = 0 the ML6686 samples control bits presented by the controller at the I/O pin, beginning on the LSB, on every rising edge of CLK following $\overline{CS}$ going low. For $\overline{CS}$ = 1, CLK is a don't care. This clock can be independent of the inputs at XTAL, TxCLK, and RxTPP/RxTPN.
4	XTAL	External clock input. When control bit XCLK is 1, this pin must be driven by an external 32MHz clock. When control bit XCLK is 0, this pin can be driven by an external 16MHz clock, or a 16MHz crystal must be connected between this pin and ground.

PIN DESCRIPTION (Continued)

PIN #	NAME	FUNCTION
5	DGND1	Ground pins for digital CMOS part of the chip.
6	DVCC1	Positive power supply pin (+5V) for digital part of the chip.
7	RxD	Receive data output to the next downstream Lobe port, or Ring-Out port. When the ML6686 is in INSERT mode, RxD is sourced by the PLL recovered data from receive twisted pair inputs RxTPP, RxTPN. When the ML6686 is in BYPASS mode RxD is sourced by the TxD input.
8	RxCLK	Synchronized data clock output to the next downstream Lobe port, or Ring-Out port. When the ML6686 is in INSERT mode, RxCLK is sourced from the PLL, by the clock extracted from receive twisted pair inputs RxTPP, RxTPN. When the ML6686 is in BYPASS mode RxCLK is sourced by the TxCLK input. RxCLK frequency is two times the data rate.
9	TxD	Data input from previous upstream Lobe port, or Ring-In port. In INSERT mode TxD is clocked by TxCLK out onto the transmit twisted pair cable TxTPP, TxTPN. In BYPASS mode the TxD input is internally connected to the RxD output.
10	TxCLK	Synchronized data clock input from previous upstream Lobe port, or Ring-In port. In INSERT mode TxCLK clocks TxD out onto the transmit twisted pair cable TxTPP, TxTPN. In BYPASS mode the TxCLK input is internally connected to the RxCLK output. TxCLK frequency is two times the data rate.
11 12	PHTM1, PHTM2	In "phantom sense" configuration (PHDSB bit set to 0), PHTM1 is the sense input for phantom current coming from an opto-isolator, and PHTM2 is an open collector pin that can be used to drive an LED to reflect the INSERT/BYPASS state (PHTM2 low indicates INSERT). In "phantom drive" configuration (PHDSB bit set to 1), these pins output a +5V phantom signal and sense opens and shorts as a phantom circuit fault condition.
13 16 31	AGND2, VSS, AGND3	Ground pins for analog part of the chip.
14 15	TxTPN, TxTPP	Transmitter wire pair outputs. These pins are the differential current driver outputs to the lobe. They provide data through an isolation transformer to the transmit twisted pair.
17	RVCO	External resistor input. A precision resistor of the appropriate value connected to this input sets the phase detector gain and VCO center frequency.
18	RTSET	External resistor input. A precision resistor of the appropriate value connected to this input sets the twisted-pair transmitter output level.
19 27	AVCC1, AVCC3	Positive power supply pins (+5V) for analog part of the chip.
20 21	EQ4B, EQ4A	Differential connection for external equalization component for 4Mbps operation. Shorting EQ4A to EQ4B disables the 4Mbps receive equalizer.
22 23	EQ16B, EQ16A	Differential connection for external equalization component for 16Mbps operation. Shorting EQ16A to EQ16B disables the 16Mbps receive equalizer.
24 25	RxTPN, RxTPP	Receive wire pair inputs. These inputs receive data from the twisted pair media through the receive isolation transformer. The common-mode bias point for these pins is set internally.
26	DGND2	Ground pins for digital CML part of the chip.
28	FILT4	4Mbps PLL filter input. Connection point for external PLL filter components for 4Mbps data rate.
29	FILTSL	Slave PLL filter input. Connection point for external PLL filter components for second slave PLL.
30	FILT16	16Mbps PLL filter input. Connection point for external PLL filter components for 16Mbps data rate.
32	$\overline{CS}$	Chip select bar. While this input is high, IO pin is in a high-impedance state. Driving $\overline{CS}$ low, enables the read or write functions through the serial interface.

ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage Range 6V
Input Voltage Range
  Digital Inputs ..... GND –0.3V to V_{CC} +0.3V
  RxTPP, RXTPN, XTAL ..... GND –0.3V to V_{CC} +0.3V
Output Current
  TxTPP, TxTPN 50mA
  PHTM1, PHTM2 ..... 25mA
  All Other Outputs 10mA
Junction Temperature ..... 150°C
Thermal Resistance ..... 60°C/W
Storage Temperature ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

OPERATING CONDITIONS

V_{CC} Supply Voltage ..... 5V ± 5%
Temperature Range ..... 0°C to 70°C
RTSET ..... 1.66kΩ ± 1%
RVCO ..... 2.42kΩ ± 1%
All V_{CC} supply pins must be within 0.1V of each other.
All GND pins must be within 0.1V of each other.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{CC} = 5V ± 5%, RTSET = 1.66kΩ, RVCO = 2.42kΩ, T_A = Operating Temperature Range (Note 1).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TTL Inputs (TxD, TxCLK, $\overline{CS}$, R/$\overline{W}$, I/O, CLK, XTAL when XCLK bit = 1):						
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
I_{IL}	Input Low Current	XTAL, TxD, TxCLK; V_{IN} = 0.4V	–1600			µA
I_{IH}	Input High Current	V_{IN} = 2.7V			100	µA
TTL Outputs (RxD, RxCLK, I/O):						
V_{OL}	Output Low Voltage	I_{OL} = 1mA			0.40	V
V_{OH}	Output High Voltage	I_{OH} = –0.1mA	2.4			V
16MHz Clock Input (XTAL, when XCLK bit = 0):						
V_{IL}	Input Low Voltage				0.5	V
V_{IH}	Input High Voltage		4.5			V
I_{IL}	Input Low Current	V_{IN} = 0V	–1600			µA
I_{IH}	Input High Current	V_{IN} = 5V			100	µA
Receiver						
V_{OSR}	RxTPP–RxTPN Differential Offset Voltage	SQDIS bit = 1	–35		35	mV
V_{DSQ}	RxTPP–RxTPN Differential		335		565	mV_{P-P}
V_{PSQ}	RxTPP–RxTPN Post-Squelch		167		282	mV_{P-P}
V_{IBR}	RxTPP–RxTPN Open-Circuit Common-Mode Bias Voltage		2.6		3.2	V
R_{IDR}	RxTPP–RxTPN Differential Input Resistance	Input differential voltage = 2V, centered at V_{IBR}	10.5		13.5	kΩ
I_{RTSET}	RTSET Input Current	RTSET = 1.66kΩ	575		625	µA
I_{RVCO}	RVCO Input Current	RVCO = 2.42kΩ	387		438	µA
Transmitter						
I_{TOUT}	TxTP Differential Output Current	R_L = 200Ω (see Figure 1a) Force INSERT, TxD = 0	25		31	mA
I_{TOFF}	TxTPP–TxTPN Off-state Output Current	FBYP = 1, R_L = 200Ω			1.5	mA
I_{TXI}	TxTPP–TxTPN Differential Current Imbalance	R_L = 200Ω	–350		350	µA

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Phantom Output						
V_{OHP}	Phantom Output High Voltage	I_{OHP} = –1mA, PHDSB = 1	4.1			V
		I_{OHP} = –2mA, PHDSB = 1	3.8			V
I_{OHP}	Phantom Output Short Circuit Current	V_{OHP} = 0V, PHDSB = 0	–1500		–800	µA
I_{OZP}	Phantom Output Off Current	PHDSB = 0 0V ≤ V_{OHP} ≤ V_{CC}	–100		+100	µA
Phantom Fault Conditions						
RL_{NFL}	Phantom No Fault Load Resistance		2.9		5.5	kΩ
RL_{SFL}	Phantom Short-Circuit Load Resistance				100	Ω
RL_{OFL}	Phantom Open-Circuit Load Resistance		20			kΩ
Power Supply Current						
I_{CCT}	Supply Current, Transmitting	Note 2			225	mA

AC CHARACTERISTICS

Unless otherwise specified, V_{CC} = 5V ± 5%, RTSET = 1.66kΩ, RVCO = 2.42kΩ, T_A = Operating Temperature Range (Note 1).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Transmitter (Note 3)						
t_{DF01}	TxTPP–TxTPN Output Delay Mismatch, Zeros and Ones	Note 4, 4Mbps	–0.5		0.5	ns
		Note 4, 16Mbps	0.3		1.0	ns
t_{DFMX}	TxTPP–TxTPN Output Delay Mismatch, Random Data	Note 5, 4Mbps & 16Mbps	–2.0		2.0	ns
t_{DCD}	TxTPP–TxTPN Output Duty Cycle Distortion	Note 6, 16Mbps	–1.5		1.5	ns
		Note 6, 4Mbps	–6.0		6.0	ns
Receiver						
t_{RPWR}	RxTPP-RxTPN Frequency to Reject	16Mbps, RxTP V_{DIFP-P} = 1V	18			MHz
		4Mbps, RxTP V_{DIFP-P} = 1V	4.5			MHz
t_{RPWO}	RxTPP-RxTPN Frequency to Turn On	16Mbps, RxTP V_{DIFP-P} = 1V			30	MHz
		4Mbps, RxTP V_{DIFP-P} = 1V			7.5	MHz
t_{RPWS}	RxTPP-RxTPN Pulse-Width to Shut Off	16Mbps, RxTP V_{DIFP-P} = 1V	120			ns
		4Mbps, RxTP V_{DIFP-P} = 1V	480			ns
t_{RPW}	RxTPP-RxTPN Pulse-Width, to Turn On	16Mbps, RxTP V_{DIFP-P} = 1V			99	ns
		4Mbps, RxTP V_{DIFP-P} = 1V			396	ns
t_{PL}	PLL Phase-Lock After Freq. Lock	Figure 2			1.5	ms
t_{FL}	PLL Frequency-Lock After Power-Up	Power-up to 2BR ± 1% Hz frequency at RxCLK; Note 7			500	ms
t_{DL}	PLL Phase Unlock Time	Figure 2			100	µs
t_{PVC1}	RxCLK Period, V_{FILT4} = 1.5V	DRATE = 1 (4Mbps), Note 8	225		150	ns
t_{PVC2}	RxCLK Period, V_{FILT4} = 3V	DRATE = 1 (4Mbps), Note 8	75		112	ns
t_{PVC3}	RxCLK Period, V_{FILTSL} = 1.5V	DRATE = 0 (16Mbps), Note 8	56.3		37.5	ns
t_{PVC4}	RxCLK Period, V_{FILTSL} = 3V	DRATE = 0 (16Mbps), Note 8	18.8		28	ns
K_d	Phase Detector Gain	4Mbps; Note 9 and Figure 3	0.25		0.35	µA/ns
		16Mbps; Note 9 and Figure 3	1.0		1.4	µA/ns
t_{RSTE}	PLL Static Phase Error	Note 10 and Figure 4	–2		+2	ns
IJTOLI	Jitter Tolerance	DRATE = 1 (4Mbps), Note 11 DRATE = 0 (16Mbps), Note 11	0.007 0.0172			ns/ns ns/ns
IJTOLXI	Jitter Tolerance with Noise	DRATE = 1 (4Mbps), Note 12 DRATE = 0 (16Mbps), Note 12	0.0035 0.0082			ns/ns ns/ns
t_{RDC}	RxD to RxCLK Delay		–2		2	ns
t_{RTD}	RxTP to RxD Delay	Fifo Length = 8UI	1		4	BT
t_{PTRD}	TxD to RxD Propagation Delay	FBYP = 1, Figure 5	22		30	ns
t_{PTRC}	TxCLK to RxCLK Propagation Delay	FBYP = 1, Figure 5	22		30	ns
t_{SRM}	Setup Time, RxD Valid to RxCLK Rising Edge (1.5V point)	RxCLK t_{PER} = 31.25ns, Figure 5	10			ns
t_{HRM}	Hold Time, RxD Valid After RxCLK Rising Edge (1.5V)	RxCLK t_{PER} = 31.25ns, Figure 5	2			ns
t_{RCRM}	RxCLK 10-90% Rise Time	RxCLK t_{PER} = 31.25ns, C_L = 15pF; Figure 5			5	ns

AC CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Receiver (Continued)						
t_{RCFM}	RxCLK 90-10% Fall Time	RxCLK t_{PER} = 31.25ns, C_L = 15pF; Figure 5			5	ns
t_{WRCL}	RxCLK Low Pulse Width	4Mbps, t_{PER} = 115ns; Figure 5 16Mbps, t_{PER} = 30ns; Figure 5	46 10			ns ns
t_{WRCH}	RxCLK High Pulse Width	4Mbps, t_{PER} = 115ns; Figure 5 16Mbps, t_{PER} = 30ns; Figure 5	35 8			ns ns
Serial Interface (Figure 6)						
t_{CW}	CLK Pulse Width	Read or Write Cycle	50			ns
t_{CSSU}	$\overline{CS}$ Setup Time, $\overline{CS}$ low to CLK Rising Edge (1.5V point)	Read or Write Cycle	30			ns
t_{RWSU}	R/$\overline{W}$ Setup Time, R/$\overline{W}$ high to CLK Falling Edge (1.5V point)	Read Cycle	30			ns
	R/$\overline{W}$ Setup Time, R/$\overline{W}$ low to CLK Falling Edge	Write Cycle	30			ns
t_{DOSU}	Data-out Setup Time, CLK Falling Edge to Data Valid	Read Cycle, C_L = 100pF			30	ns
t_{DISU}	Data-in Setup Time, Data Valid to CLK Rising Edge	Write Cycle	10			ns
t_{DIH}	Data-in Hold Time, Data Valid after CLK Rising Edge	Write Cycle	10			ns

Note 1: Limits are guaranteed by 100% testing, sampling or correlation with worst case test conditions.

Note 2: Current into all V_{CC} pins, V_{CC} = 5.25V, transmitting and receiving 16MHz data.

Note 3: The transmitter TxTPP-TxTPN output waveform must also conform with the ISO/IEC 8802-5q standard.

Note 4: Difference between the delay from the nearest TxCLK rising edge to TxTPP/N differential BR edge and delay from the nearest TxCLK rising edge to the TxTPP/N differential BR/2 edge. Measured for either rising output edges or falling output edges only, with measurements made for each. Measurements are to be made at the output of both test circuits shown in Figure 1bc. (See waveforms at Figure 7-4 of the IEEE 802.4q/standard.)

Note 5: Difference between the delay from the nearest TxCLK rising edge to TxTPP/N differential edge and the delay from the nearest TxCLK rising edge to TxTPP/N differential edge. Measured for either rising output edges or falling output edges only, with measurements made for each using random data (JKs, 0s, 1s). Measurements are to be made at the output of both test circuits shown in Figure 1bc. (See waveforms at Figure 7–4 of draft IEEE 802.4q/standard.)

Note 6: One-half the difference between the positive-going differential output pulsewidth and the negative-going differential output pulsewidth. Measured at the output of both test circuits in Figure 10bc with a constant stream of all zeros or all ones. Measurements are to be averaged over 128 data pulses. Measured with input drive to TxD/TxCLK.

Note 7: Not tested in production. Guaranteed by characterization measurements.

Note 8: Disconnect the filter components at the FILT4 or FILT16 pins and apply the indicated voltage to that pin. Measure the output period at RxCLK. Disconnect RxTPP/N from all input.

Note 9: See Figure 2 for timing. With the circuit in phase-lock, inject I1 = +5μA and measure the propagation delay t_{PD1} between an RxTPP rising edge and the corresponding RxCLK falling edge. Make a second delay measurement t_{PD2} while injecting I2 = –5μA. Phase detector gain is given by Kd = (I2 – I1)/(t_{PD1} – t_{PD2}).

Note 10: The ML6686 is phase-locked to the RxTPP waveform with RxTPN biased to 2.5V (see Figure 4). Monitor RxD to observe correct data being latched. For one pulse, shorten the positive pulse at RxTPP by moving the rising edge, and check to see if the short pulse was latched. Continue to shorten the pulse in this manner until incorrect data appears at RxD. The time between the rising edge and the unshortened positive pulse midpoint is t_{RSTE}. Repeat this procedure for the other 3 cases shown in Figure 4.

Note 11: The ML6686 is phase-locked to the RxTPP waveform with RxTPN biased to 2.5V (see Figure 3). Apply a signal at RxTPP consisting of alternating sequences of data_ones and data_zeros. The sequences alternate with a frequency of 4.67kHz and 9.17kHz for datarates of 4 and 16Mbps respectively. The bit time (BT) for data_ones is (1 × 0.5 × |JTOLI|)/Datarate, and the BT for data_zeros is (1 + 0.5 × |JTOLI|)/Datarate. Under these conditions the frame error rate does not exceed 10^{-5}.

Note 12: The ML6686 is phase-locked to the RxTPP waveform with RxTPN biased to 2.5V (see Figure 3). Apply a signal at RxTPP that is the summation of two components. *The first component consisting of alternating sequences of data_ones and data_zeros. The sequences alternate with a frequency of 4.67kHz and 9.17kHz for* datarates of 4 and 16Mbps respectively. The bit time (BT) for data_ones is (1 – 0.5 × |JTOLX|)/Datarate, and the BT for data_zeros is (1 + 0.5 × |JTOLX|)/Datarate. The shape of the signal should conform with the IEEE 802.4q/standard. The second component is a sinusoidal waveform with a frequency of 12MHz and an amplitude 12dB lower than the data. Under these conditions the frame error rate does not exceed 10^{-5}.

TABLE 1. STATUS REGISTER

BIT	NAME	DESCRIPTION
0	$\overline{\text{LOCK}}$	A 0 indicates that both PLLs are locked.
1	$\overline{\text{FAULT}}$	Phantom wire fault detection bit. When this bit is 0, the phantom current test has failed. In "phantom drive" configuration (PHDSB bit set to 1), this will be an open or a short at PHTM1 or PHTM2 pins. In "phantom sense" configuration (PHDSB bit set to 0), this bit follows the status of PHTM1 pin.
2	$\overline{\text{SIGVAL}}$	Signal valid bit from the squelch circuit. A 0 indicates that the signal at RxTPP/RxTPN meets frequency and amplitude requirements.
3	UOFLOW	A 1 indicated an underflow or overflow condition of the FIFO.
4	TPPRTEN	A 1 indicated that the station is inserted. A 0 indicates that the station is bypassed. When the ML6686 is bypassed, RxD and RxCLK are sourced by TxD and TxCLK, and TxTPP and TxTPN are sourced by RxTPP and RxTPN. INSERT = not(FBYP) × ($\overline{\text{ALLOW}}$ + $\overline{\text{FAULT}}$)
5	PHTMENBL	A 1 indicates that the ML6686 is in phantom drive configuration. A 0 indicates that the ML6686 is in phantom sense configuration.
6	TxENB	A 0 indicates that the transmitter differential output buffer is enabled.
17	HUBPHSEN	A 1 indicates that the ML6686 is in phantom sense confiugration and inserted.
8-16		Not used

TABLE 2. CONTROL REGISTER

BIT	NAME	DESCRIPTION
0	FBYP	Force Bypass bit. A 1 forces the ML6686 into BYPASS mode. (Defaults to 0, not forced).
1	RSL	Receive Squelch Low bit. A 1 selects the lower receive squelch level, more sensitive. A 0 selects the higher receive squelch level, less sensitive. (Defaults to 0, high level).
2	DRATE	Data Rate selection bit. A 1 selects 4Mbps operation. A 0 selects 16Mbps operation. This bit automatically switches the PLL loop filter and the equalizer filter for the appropriate data rate. (Defaults to 0, 16Mbps).
3	PHD/$\overline{S}$	"Phantom drive/$\overline{\text{sense}}$" select bit. A 0 configures the ML6686 for "phantom sense." In the "phantom sense" state PHTM1 pin serves as an input coming from an opto-isolator to sense phantom current and PHTM2 is an open collector pin that can be used to drive an LED to reflect the INSERT/BYPASS state. A 1 configures the ML6686 for "phantom drive." In the "phantom drive" state both PHTM1 and PHTM2 pins provide the phantom drive and fault detect for the transmit pair of wires. (Defaults to 0, phantom sense).
4, 5	FL0 & FL1	This two bits set the FIFO length in the following way: FL0 = FL1 = 0 then FIFO length = 8UI FL0 = 0 and FL1 = 1 then FIFO length = 4UI FL0 = 1 and FL1 = 0 then FIFO length = 2UI FL0 = FL1 = 1 then No FIFO A unit interval, UI, is equivalent to half a data bit. (Defaults to 00, 2 UI).
6	$\overline{\text{ALLOW}}$	A 0 allows the remote station to place the ML6686 into INSERT or BYPASS state with phantom control. A 1 overrides the internal phantom current test. INSERT/$\overline{\text{BYPASS}}$ = not(FBYP) × ($\overline{\text{ALLOW}}$ + $\overline{\text{FAULT}}$) (Defaults to 0, phantom control enabled).
7	BYPRETB	If this bit is set to 1, no retiming is done in BYPASS mode. The PLLs of this ML6686 are bypassed. If this bit is set to 0 the retiming is controlled by DISSL. (Defaults to 0, BYPASS retiming enabled).
8	DISSL	If this bit is set to 1, the second or slave PLL is disabled. (Defaults to 0, both PLLs enabled).
9	SQDIS	A 1 disables the RxTP wire pair squelch function by forcing SIGVALB to 0. (Defaults to 0, squelch enabled).
10	XCLK	If this bit 0, the ML6686 should have a 16MHz crystal connected between the XTAL pin and the digital ground, or this pin should be driven by an external 16MHz clock. If this bit is 1, the XTAL pin should be driven by an external 32MHz clock. (Defaults to 0, 16MHz external clock or crystal).
11	XTRST	As 1 forces the output of the power-on reset circuit to 1. (Defaults to 0, not reset).
12	FIFOTST	If this bit is set to 1, the FIFO's output clock is TxCLK instead of the extracted clock at the slave PLL. (Defaults to 0, clock from slave PLL).
13, 14 15	CNT	These bits should remain 0 for proper operation. (Defaults to 0).

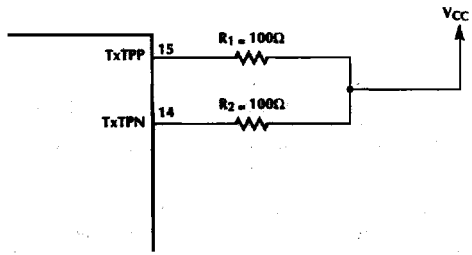


Figure 1a. Transmitter DC Test Circuit

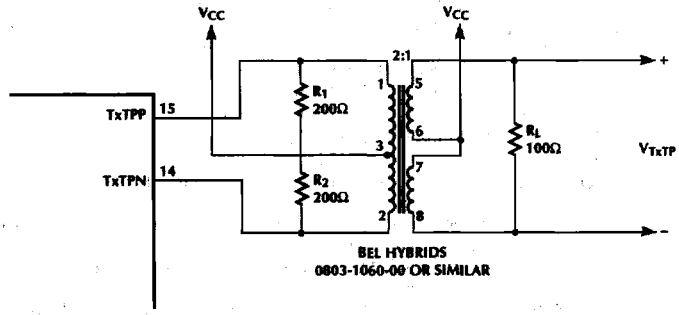


Figure 1b. Transmitter AC Test Circuit, 100 Ohms (UTP).

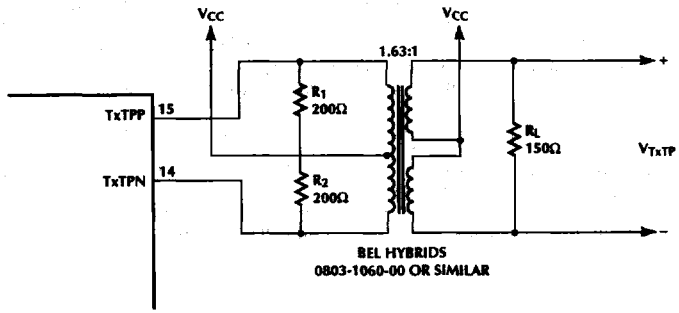


Figure 1c. Transmitter AC Test Circuit, 150 Ohms (STP).

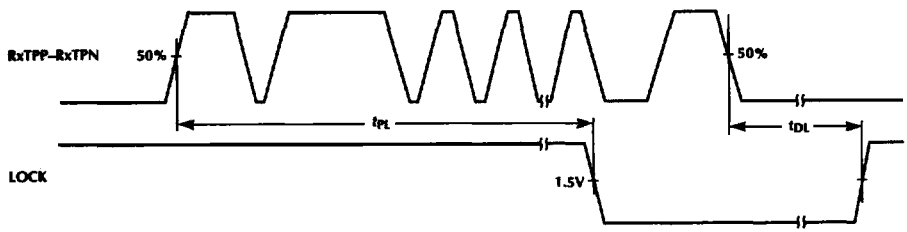


Figure 2. PLL Phase Lock Timing.

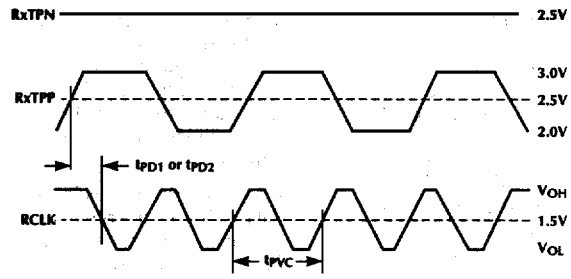


Figure 3. Phase Detector Gain Test.

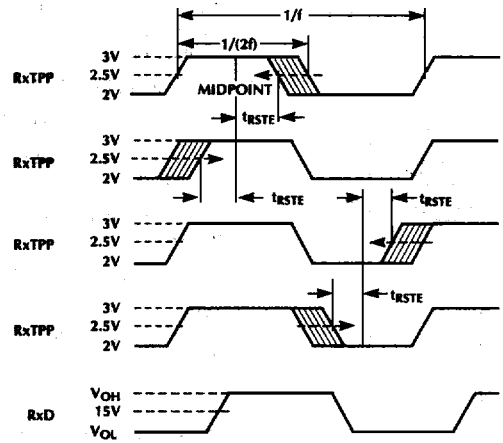


Figure 4. Receiver Static Timing Error Test.

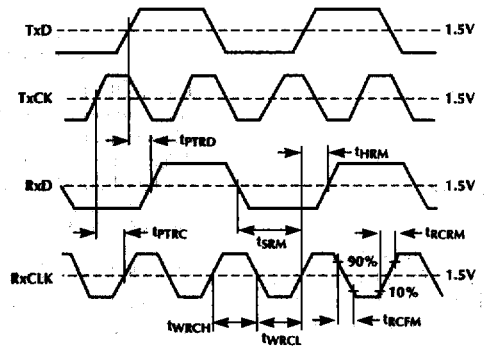


Figure 5. Receiver Timing.

FUNCTIONAL DESCRIPTION

Page 1 shows the functional block diagram of the ML6686. The device contains four major functional blocks; twisted pair line interface, port interface, control and status interface, and PLL retiming circuit. In a typical operation, the data that comes from the previous port, through TxD and TxCLK, is retransmitted on to the transmit TxTP wire pair to the station. The data from the station via the receive wire pair is retimed through the use of a dual PLL/FIFO. The retimed data is then fed to the next port by RxD and RxCLK.

PORT INTERFACE

The ML6686 can be used for implementing Lobe, Ring-In and Ring-Out ports in a MSAU. The device can be placed into either the INSERT state or the BYPASS state. Figure 6 is a functional illustration of the INSERT and BYPASS states.

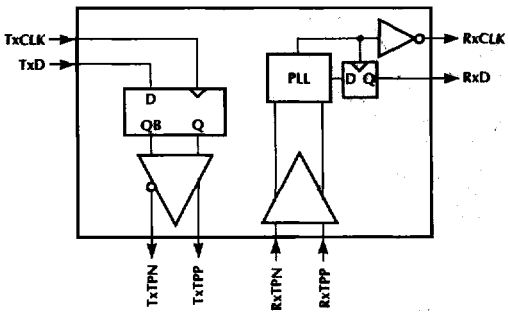


Figure 6a. Insert

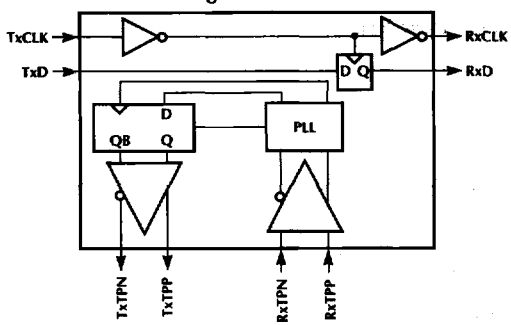


Figure 6b. Bypass

When ML6686 is in the BYPASS state, the station is "bypassed". The clock and data input from the previous port is retimed and fed directly through to the next port (see Figure 6b). Signal from the receive twisted pair is retimed via the PLL and looped back to the transmit twisted pair. However, if the signal does not meet the receive frequency squelch criteria, the signal will not be locked onto the PLL. The PLL will transmit the local clock signal onto the transmit twisted pair. The user can also select to loop back the signal to the twisted pair without retiming.

When the station is INSERTed into the ring, the transmit data TxD from the previous port is fed out on the twisted pair lines clocked by transmit clock TxCLK, and the data from the receive twisted pair input is passed through the PLL and output on RxD and RxCLK pins.

The ML6686 can be used as either Lobe, Ring-In or Ring-Out port transceiver. These different port implementation can be accomplished by placing the ML6686 into either INSERT or BYPASS state, and into phantom drive or phantom sense configuration appropriately. Through various control bits, the ML6686 may be selected for one of three options:

1. Forced into the INSERT state.
2. Forced into the BYPASS state.
3. Allow the remote station to place the ML6686 into INSERT or BYPASS state with phantom control.

The logic equation to implement these options is as follows:

$$\text{INSERT} = \text{not (FBYP)} \times (\overline{\text{ALLOW}} + \overline{\text{FAULT}})$$

When INSERT is a logic 1, the ML6686 is placed into the INSERT state as shown in Figure 6a. When INSERT is a logic 0, the ML6686 is placed into the BYPASS state. Table 3 illustrates how the three above options can be achieved.

FBYP	$\overline{\text{ALLOW}}$	$\overline{\text{FAULT}}$	INSERT	STATE
1	X	X	0	Forced Bypass Mode
0	0	0	0	Phantom controlled bypass
0	0	1	1	Phantom controlled insert
0	1	X	1	Forced insert

Table 3: Logic for INSERT/BYPASS

The $\overline{\text{FAULT}}$ bit always reflects the status of the phantom circuit regardless of whether the ML6686 is in the INSERT/BYPASS state or phantom drive/phantom sense mode. INSERT/BYPASS state can be controlled by only one bit by setting $\overline{\text{ALLOW}}$ always to 1. $\overline{\text{FAULT}}$ is used to reflect the status of the phantom circuits and FBYP is used to control INSERT/BYPASS.

TP LINE INTERFACE

TP Line Receiver consists of a line equalizer, receive squelch circuit and a resistive attenuator.

RECEIVE EQUALIZER

This receive equalizer compensates for twisted-pair cable dispersion, which otherwise would give rise to inter-symbol interference (ISI). The amount of equalization varies with the average amplitude of the received signal. The received signal amplitude gives a rough value for the length of the attached cable. The filter/equalizer characteristic is the inverse of the cable's dispersion characteristic. Both UTP and STP cables approximate a low-pass filter, so the filter/equalizer approximates an inverse root f equalizer. There are two sets of equalizers, one for 4 Mbps operation and one for 16 Mbps operation. This is switched automatically when the DRATE bit is toggled. The equalizer's filter consist of two external resistors and one external capacitor.

RECEIVE SQUELCH CIRCUIT

The TP line receiver consists of a resistive attenuator with common-mode bias set circuit.

The receive squelch circuit qualifies the incoming signal to determine whether the signal contains valid data. The circuit qualifies the signal on the basis of the pulse width of the signal. This prevents the PLL from trying to lock onto the wrong frequency when using 4 or 16 Mbps data rates. Once the signal has been qualified, the circuit will then unsquelch. The DRATE bit selects one of two frequency squelch criteria.

Pulse Width and Frequency Squelch Criteria

4Mbps max frequency limit	4.5MHz to 6.5MHz
4Mbps max pulse width limit	396ns to 480ns
16Mbps max frequency limit	18MHz to 26MHz
16Mbps max pulse width limit	99ns to 120ns

When squelch is on, the PLL is tracking the internal clock frequency coming from an external clock or the internal oscillator. When the part unsquelches the PLL switches into phase acquisition mode, attempting to phase lock onto the incoming data.

PHASE LOCK LOOP

The PLL is a third-order, type II charge-pump loop (see F. M. Gardner, "Charge-Pump Phase-Lock Loops", IEEE Trans Comm, Vol. COM-28, No. 11, pp. 1849-1858, November 1980). It has high damping factor and low loop bandwidth to minimize accumulated jitter. The third pole is at a very high frequency, since the ratio of the second and third order pole capacitors C1/C3 is about 20,000:1.

The 16Mbps loop filter as well as the 4Mbps loop filter is external to the chip and consists of two capacitors and a resistor. The switching between the two loop filters is automatic when the DRATE bit is toggled. Each data rate uses a different charge pump.

The VCO uses a MOS voltage-to-current converter at its input to give a very high input impedance and low static phase error. The high VCO input impedance also allows the elimination of a loop filter buffer and the parasitic poles a buffer would add to the loop.

The first PLL will achieve lock after several milli-seconds of a static phase error of less than ±4ns. Hysteresis is built into the lock circuit so that it is more difficult to achieve lock than it is to loose lock. This will also prevent any oscillation of the $\overline{LOCK}$ bit. Lock will be lost if the phase error exceeds ±4ns for several microseconds. Once lock is lost, the PLL will try to achieve phase lock for several milli-seconds. If it is unsuccessful, the ML6686 will switch to internal frequency acquisition mode and re-center the VCO. Once it has achieved frequency lock with its internal oscillator, it will automatically switch to phase acquisition mode and try again to phase lock onto the data.

The frequency squelch circuit will limit the frequency range allowed to pass into the PLL. This limited frequency range in addition to the stringent lock criteria will insure that the PLL will not lock onto harmonics or sidebands of the fundamental data rate.

The first PLL clocks the data into the FIFO. Each flip-flop in the FIFO stores one UI which is one half bit. The second PLL has a much narrower bandwidth set by the external filter connected to pin FILTSL. The second PLL is fed by the first PLL's clock so that it can remove more of the jitter. The clock out of the second PLL is used to clock the data out of the FIFO and onto the RxCLK and RxD pins. This dual PLL architecture is the most effective way to reduce jitter and insure optimal performance from a token ring network.

TP LINE DRIVER

The TP OUTPUT driver uses a current mode switch which develops the output voltage by driving current through the terminating resistors and the output filter. Both outputs TxTPP and TxTPN are open collector, intended to drive a center-tapped transformer, with the center tap connected to V_{CC}. The driver is capable of driving 150 ohm doubly-terminated transmission lines to a minimum $3.75V_{P-P}$ level or 100Ω doubly-terminated transmission lines to a minimum $2.5V_{P-P}$ level. The driver output is waveshaped on-chip eliminating the need for a complex external transmit filter.

PHANTOM CURRENT DETECTION

The ML6686 provides a phantom current detection function. Phantom voltage and wire fault detection circuit

- Provides correct phantom DC output voltage under normal conditions.
- Senses short-circuit and open-circuit fault conditions, and removes phantom voltage when appropriate.

In the Lobe port application (FBYP and $\overline{ALLOW}$ set low), the phantom current places the device into either the BYPASS mode or the INSERT mode. When there is a wire fault or no station is attached, the device will be placed in the BYPASS mode and data from the previous port will be passed on to the next port.

SERIAL INTERFACE

There is a 16-bit Control register, and a 16-bit Status register, that can be accessed through a bidirectional I/O pin. The controller can access a full register or only part of it, always beginning at the LSB.

To read the Status register, the controller drives the R/$\overline{W}$ pin high, and the $\overline{CS}$ pin low (Figure 7a). The ML6686 presents the LSB of the Status register to the I/O pin, at the first falling edge of CLK following $\overline{CS}$ going low. The ML6686 continues presenting new status bits at every falling edge of CLK as long as $\overline{CS}$ remains low and R/$\overline{W}$ remains high. The controller is expected to sample the state of the I/O pin at the rising edges of CLK. Once $\overline{CS}$ goes high, the interface logic is reset so that the following read operation begins at the LSB again. The controller can choose to read from one to sixteen bits, beginning at the LSB and up to the MSB.

To write to the Control register, the controller drives both the R/$\overline{W}$ and $\overline{CS}$ pins low (Figure 7b). The ML6686 samples the state of the I/O pin at the rising edges of CLK following $\overline{CS}$ going low, and as long as $\overline{CS}$ and R/$\overline{W}$ remain low. Once $\overline{CS}$ goes high, the interface logic is reset so that the following write operation begins writing to the LSB again.

CLOCK OSCILLATOR

The ML6686 provides an optional on-chip clock oscillator by connecting a 16MHz crystal to the XTAL pin. The ML6686 is expected to be driven by an external clock at the XTAL pin. The part can also be driven by a 32MHz external clock at the XTAL pin, when the bit XCLK is set to 1.

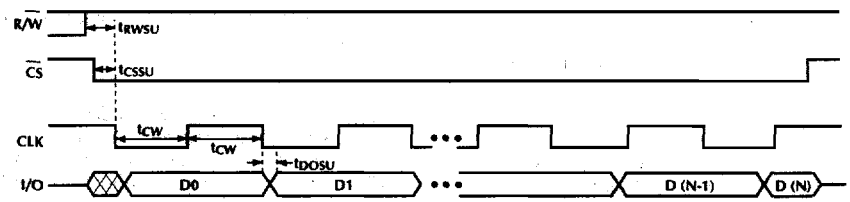


Figure 7a. Read From Status Register

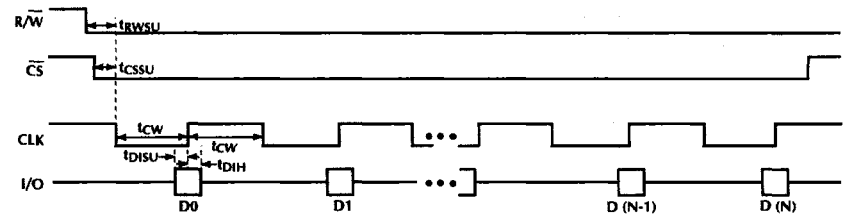


Figure 7b. Write to Control Register

APPLICATIONS

Figure 8 shows a block diagram of an intelligent Hub implementation with active retiming on each port. The architecture shown has a backup ring for fault tolerant operation. The Ring-In or the Ring-Out ports are fault tolerant by using phantom current to detect faults. When a fault is detected, the Ring-In or the Ring-Out port then goes into the bypass state and perform an automatic loopback onto the Back-up Ring. This feature is especially useful in stackable hub designs.

A microprocessor can be used to manage each individual port. All the ports including the Ring-In and Ring-Out ports can be individually programmed into "Force INSERT", "Force BYPASS" or "Allow phantom control."

LOBE PORT

Figure 9 shows a typical implementation of a Lobe port. Lobe ports are configured as phantom sense ports. Phantom current is sensed with two opto-isolators whose outputs are nor-gated and fed into pin PHTM1. PHTM2 will go low, with an open collector output, when the ML6686 goes into the INSERT state. This signal may either be used to drive an LED indicator or another opto-isolator to signal the remote station whether it is inserted or not.

RING-OUT PORT

The Ring-Out port is also configured for phantom sense when using automatic loopback fault detection. When Phantom current is detected the part is in the INSERT state. If phantom current is lost, the ML6686 will automatically switch to the BYPASS state. Using the FBYP and $\overline{\text{ALLOW}}$ bits the part can also be forced into INSERT state, for compatibility with older standard type MSAUs, or forced into BYPASS for diagnostic purposes.

Figure 9 shows the implementation of a fault tolerant Ring-Out port. In this configuration, the Ring-Out port is implemented exactly like a Lobe port. The RxD and RxCLK pins are connected to the TxD and the TxCLK pins of the Ring-In port to create a "back up" ring. When the fault tolerant feature is not needed for compatibility with the older MSAUs, the phantom current sense capability of the ML6686 should be disabled and the device should be placed in the forced insert state by using FBYP and $\overline{\text{ALLOW}}$. The LOCK bit should still be used to ensure that the proper ring speed is maintained.

RING-IN PORT

Figure 10 is an application circuit of a Ring-In port configured for phantom drive. In this mode the Ring-In port looks like a station, however when a FAULT is detected on the transmit or receive twisted pair wires, the ML6686 will automatically go into BYPASS state. The PHTM1 and PHTM2 pins drive the transmit pair transformer center taps.

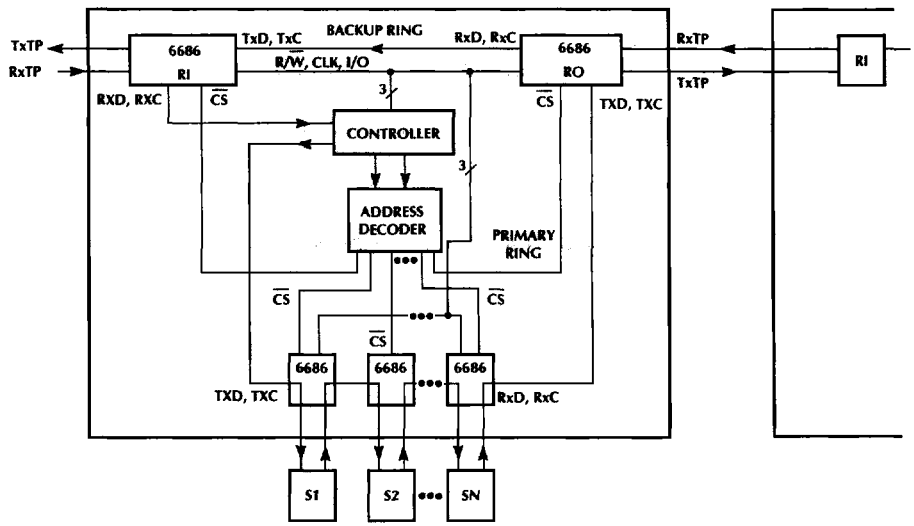


Figure 8. Intelligent Token Ring Hub

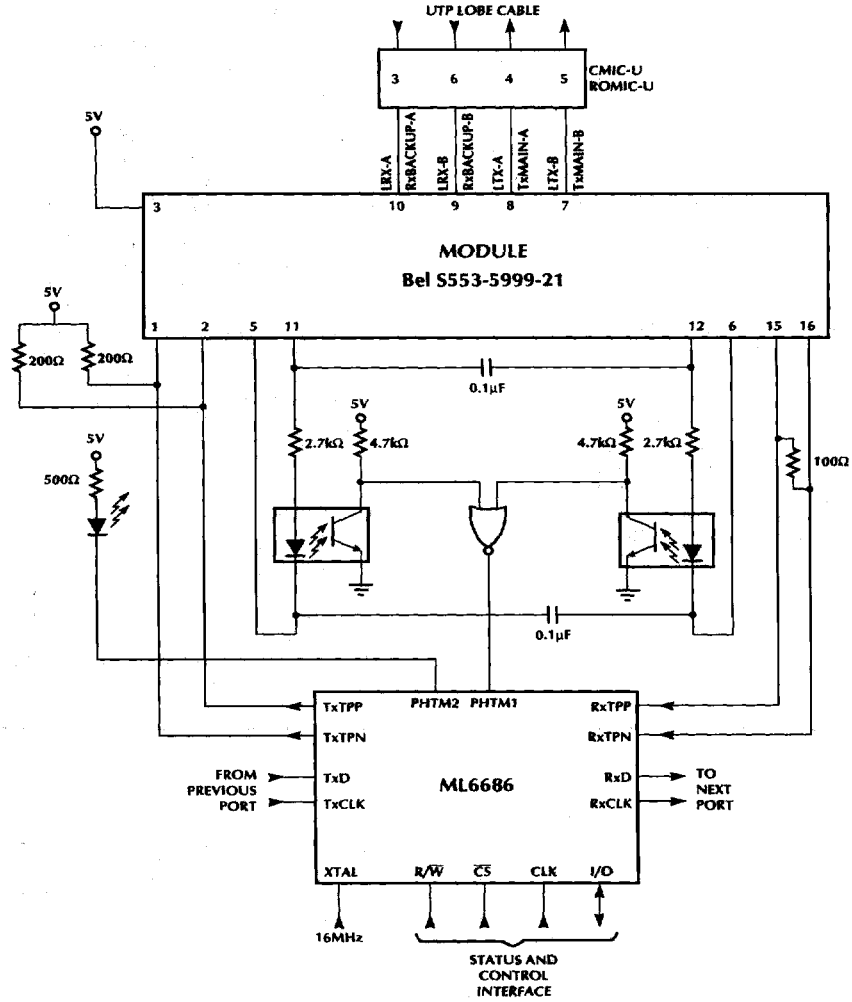


Figure 9. Lobe Port or Ring-Out Port

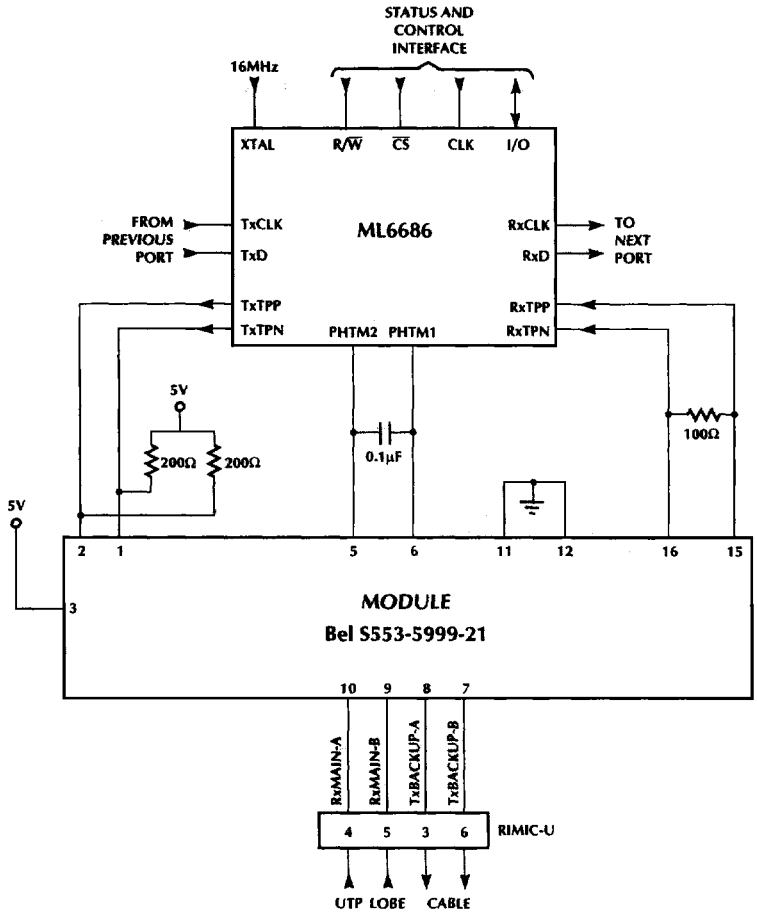


Figure 10. Ring-In Port

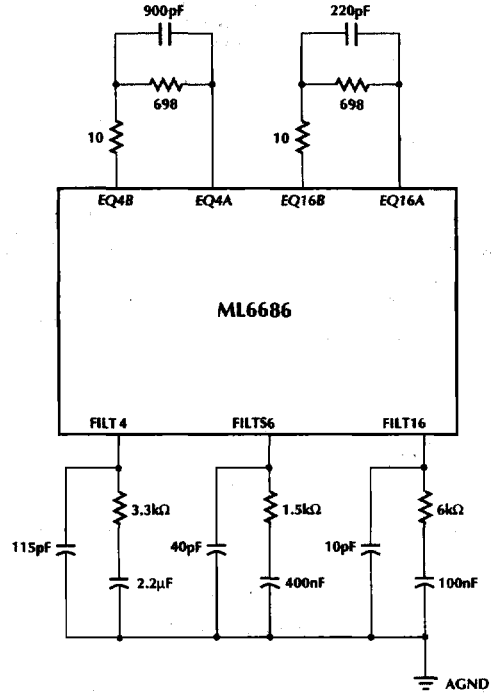


Figure 11. Suggested Filter and Equalization Networks

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6686CQ	0°C to 70°C	32-Pin PLCC (Q32)