

**260-Pin BGA**  
**Commercial Temp**  
**Industrial Temp**

## 144Mb SigmaQuad-IVe™ Burst of 2 ECCRAM™, POD I/O

**Up to 1333 MHz**  
**1.2V / 1.25V V<sub>DD</sub>**  
**1.2V / 1.25V V<sub>DDQ</sub>**

### Features

- 4Mb x 36 and 8Mb x 18 organizations available
- 1333 MHz maximum operating frequency
- 2.666 BT/s peak transaction rate (in billions per second)
- 192 Gb/s peak data bandwidth (in x36 devices)
- Separate I/O DDR Data Buses
- Non-multiplexed DDR Address Bus
- Two operations - Read and Write - per clock cycle
- Burst of 2 Read and Write operations
- 16 bank architecture
- On-chip ECC with virtually zero SER
- Loopback signal timing training capability
- Optional Data Bus Inversion
- 1.2V or 1.25V core voltage
- 1.2V or 1.25V POD I/O interface (JESD8-24 compliant)
- Configuration registers
- Configurable Read Latency (6 or 5 cycles)
- Configurable ODT (on-die termination)
- ZQ pin for programmable driver and ODT impedances
- IEEE 1149.1 JTAG-compliant Boundary Scan
- 260-pin, 14 mm x 22 mm, 1 mm ball pitch BGA package
  - K: 5/6 RoHS-compliant package
  - GK: 6/6 RoHS-compliant package

### SigmaQuad-IVe™ Family Overview

SigmaQuad-IVe ECCRAMs are the Separate I/O half of the SigmaQuad-IVe/SigmaDDR-IVe family of high performance ECCRAMs. Although similar to GSI's third generation of networking SRAMs (the SigmaQuad-IIIE/SigmaDDR-IIIE family), these fourth generation devices offer several new features that help enable significantly higher performance.

### Clocking and Addressing Schemes

The GS81314PQ18/36K SigmaQuad-IVe ECCRAMs are synchronous devices. They employ three pairs of positive and negative input clocks; one pair of master clocks,  $\overline{CK}$  and  $\overline{CK}$ , and two pairs of write data clocks,  $\overline{KD}[1:0]$  and  $\overline{KD}[1:0]$ . All six input clocks are single-ended; that is, each is received by a dedicated input buffer.

$\overline{CK}$  and  $\overline{CK}$  are used to latch address and control inputs, and to control all output timing.  $\overline{KD}[1:0]$  and  $\overline{KD}[1:0]$  are used solely to latch data inputs.

Each internal read and write operation in a SigmaQuad-IVe B2 ECCRAM is two times wider than the device I/O bus. An input data bus de-multiplexer is used to accumulate incoming data before it is simultaneously written to the memory array. An output data multiplexer is used to capture the data produced from a single memory array read and then route it to the appropriate output drivers as needed. Therefore, the address field of a SigmaQuad-IVe B2 ECCRAM is always one address pin less than the advertised index depth (e.g. the 8M x 18 has 4M addressable index).

### On-Chip Error Correction Code

GSI's ECCRAMs implement an ECC algorithm that detects and corrects all single-bit memory errors, including those induced by SER events such as cosmic rays, alpha particles, etc. The resulting Soft Error Rate of these devices is anticipated to be <0.002 FITs/Mb — a 5-order-of-magnitude improvement over comparable SRAMs with no on-chip ECC, which typically have an SER of 200 FITs/Mb or more.

All quoted SER values are at sea level in New York City.

### Parameter Synopsis

| Speed Grade | Max Operating Frequency | Read Latency | V <sub>DD</sub> |
|-------------|-------------------------|--------------|-----------------|
| -1333       | 1333 / 1100 MHz         | 6 / 5 cycles | 1.2V to 1.3V    |
| -1250       | 1250 / 1000 MHz         | 6 / 5 cycles | 1.15V to 1.3V   |
| -1100       | 1100 / 900 MHz          | 6 / 5 cycles | 1.15V to 1.3V   |
| -1000       | 1000 / 833 MHz          | 6 / 5 cycles | 1.15V to 1.3V   |

**8M x 18 Pinout (Top View)**

|          | 1                | 2                | 3                | 4                | 5                | 6                | 7                | 8                | 9                | 10               | 11               | 12               | 13               |
|----------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| <b>A</b> | V <sub>DD</sub>  | NU <sub>O</sub>  | V <sub>DD</sub>  | NU <sub>I</sub>  | NC<br>(RSVD)     | MCH<br>(CFG)     | MRW              | ZQ               | PZT1             | DINV0            | V <sub>DD</sub>  | QINV0            | V <sub>DD</sub>  |
| <b>B</b> | V <sub>SS</sub>  | NU <sub>O</sub>  | V <sub>SS</sub>  | NU <sub>I</sub>  | MCL              | MCL<br>(B4M)     | NC<br>(RSVD)     | MCH<br>(SIOM)    | PZT0             | D0               | V <sub>SS</sub>  | Q0               | V <sub>SS</sub>  |
| <b>C</b> | Q17              | V <sub>DDQ</sub> | D17              | V <sub>DDQ</sub> | V <sub>SS</sub>  | SA13             | V <sub>DD</sub>  | SA14             | V <sub>SS</sub>  | V <sub>DDQ</sub> | NU <sub>I</sub>  | V <sub>DDQ</sub> | NU <sub>O</sub>  |
| <b>D</b> | V <sub>SS</sub>  | NU <sub>O</sub>  | V <sub>SS</sub>  | NU <sub>I</sub>  | SA19             | V <sub>DDQ</sub> | NC<br>(288 Mb)   | V <sub>DDQ</sub> | SA20             | D1               | V <sub>SS</sub>  | Q1               | V <sub>SS</sub>  |
| <b>E</b> | Q16              | V <sub>DDQ</sub> | D16              | V <sub>DD</sub>  | V <sub>SS</sub>  | SA11             | V <sub>SS</sub>  | SA12             | V <sub>SS</sub>  | V <sub>DD</sub>  | NU <sub>I</sub>  | V <sub>DDQ</sub> | NU <sub>O</sub>  |
| <b>F</b> | V <sub>SS</sub>  | NU <sub>O</sub>  | V <sub>SS</sub>  | NU <sub>I</sub>  | SA17             | V <sub>DD</sub>  | V <sub>DDQ</sub> | V <sub>DD</sub>  | SA18             | D2               | V <sub>SS</sub>  | Q2               | V <sub>SS</sub>  |
| <b>G</b> | Q15              | NU <sub>O</sub>  | D15              | NU <sub>I</sub>  | V <sub>SS</sub>  | SA9              | NU <sub>I</sub>  | SA10             | V <sub>SS</sub>  | D3               | NU <sub>I</sub>  | Q3               | NU <sub>O</sub>  |
| <b>H</b> | Q14              | V <sub>DDQ</sub> | D14              | V <sub>DDQ</sub> | SA15             | V <sub>DDQ</sub> | $\bar{W}$        | V <sub>DDQ</sub> | SA16             | V <sub>DDQ</sub> | NU <sub>I</sub>  | V <sub>DDQ</sub> | NU <sub>O</sub>  |
| <b>J</b> | V <sub>SS</sub>  | NU <sub>O</sub>  | V <sub>SS</sub>  | NU <sub>I</sub>  | V <sub>SS</sub>  | SA7              | V <sub>SS</sub>  | SA8              | V <sub>SS</sub>  | D4               | V <sub>SS</sub>  | Q4               | V <sub>SS</sub>  |
| <b>K</b> | CQ1              | V <sub>DDQ</sub> | V <sub>REF</sub> | V <sub>DD</sub>  | KD1              | V <sub>DD</sub>  | CK               | V <sub>DD</sub>  | KD0              | V <sub>DD</sub>  | V <sub>REF</sub> | V <sub>DDQ</sub> | CQ0              |
| <b>L</b> | $\overline{CQ1}$ | V <sub>SS</sub>  | QVLD1            | V <sub>SS</sub>  | $\overline{KD1}$ | V <sub>DDQ</sub> | $\overline{CK}$  | V <sub>DDQ</sub> | $\overline{KD0}$ | V <sub>SS</sub>  | QVLD0            | V <sub>SS</sub>  | $\overline{CQ0}$ |
| <b>M</b> | V <sub>SS</sub>  | Q13              | V <sub>SS</sub>  | D13              | V <sub>SS</sub>  | SA5              | V <sub>SS</sub>  | SA6              | V <sub>SS</sub>  | NU <sub>I</sub>  | V <sub>SS</sub>  | NU <sub>O</sub>  | V <sub>SS</sub>  |
| <b>N</b> | NU <sub>O</sub>  | V <sub>DDQ</sub> | NU <sub>I</sub>  | V <sub>DDQ</sub> | PLL              | V <sub>DDQ</sub> | $\bar{R}$        | V <sub>DDQ</sub> | MCL              | V <sub>DDQ</sub> | D5               | V <sub>DDQ</sub> | Q5               |
| <b>P</b> | NU <sub>O</sub>  | Q12              | NU <sub>I</sub>  | D12              | V <sub>SS</sub>  | SA3              | MZT              | SA4              | V <sub>SS</sub>  | NU <sub>I</sub>  | D6               | NU <sub>O</sub>  | Q6               |
| <b>R</b> | V <sub>SS</sub>  | Q11              | V <sub>SS</sub>  | D11              | MCH              | V <sub>DD</sub>  | V <sub>DDQ</sub> | V <sub>DD</sub>  | RST              | NU <sub>I</sub>  | V <sub>SS</sub>  | NU <sub>O</sub>  | V <sub>SS</sub>  |
| <b>T</b> | NU <sub>O</sub>  | V <sub>DDQ</sub> | NU <sub>I</sub>  | V <sub>DD</sub>  | V <sub>SS</sub>  | SA1              | V <sub>SS</sub>  | SA2              | V <sub>SS</sub>  | V <sub>DD</sub>  | D7               | V <sub>DDQ</sub> | Q7               |
| <b>U</b> | V <sub>SS</sub>  | Q10              | V <sub>SS</sub>  | D10              | NC<br>(576 Mb)   | V <sub>DDQ</sub> | NC<br>(RSVD)     | V <sub>DDQ</sub> | NC<br>(1152 Mb)  | NU <sub>I</sub>  | V <sub>SS</sub>  | NU <sub>O</sub>  | V <sub>SS</sub>  |
| <b>V</b> | NU <sub>O</sub>  | V <sub>DDQ</sub> | NU <sub>I</sub>  | V <sub>DDQ</sub> | V <sub>SS</sub>  | SA21<br>(x18)    | V <sub>DD</sub>  | SA0<br>(B2)      | V <sub>SS</sub>  | V <sub>DDQ</sub> | D8               | V <sub>DDQ</sub> | Q8               |
| <b>W</b> | V <sub>SS</sub>  | Q9               | V <sub>SS</sub>  | D9               | TCK              | MCL              | RCS              | MCL              | TMS              | NU <sub>I</sub>  | V <sub>SS</sub>  | NU <sub>O</sub>  | V <sub>SS</sub>  |
| <b>Y</b> | V <sub>DD</sub>  | QINV1            | V <sub>DD</sub>  | DINV1            | TDO              | NU               | NC<br>(RSVD)     | MCL              | TDI              | NU <sub>I</sub>  | V <sub>DD</sub>  | NU <sub>O</sub>  | V <sub>DD</sub>  |

**Notes:**

1. Pins 5B, 6W, 8W, 8Y, and 9N must be tied Low in this device.
2. Pin 5R must be tied High in this device.
3. Pin 6A is defined as mode pin CFG in the pinout standard. It must be tied High in this device to select x18 configuration.
4. Pin 6B is defined as mode pin B4M in the pinout standard. It must be tied Low in this device to select Burst-of-2 configuration.
5. Pin 8B is defined as mode pin SIOM in the pinout standard. It must be tied High in this device to select Separate I/O configuration.
6. Pin 6V is defined as address pin SA for x18 devices. It is used in this device.
7. Pin 8V is defined as address pin SA for B2 devices. It is used in this device.
8. Pin 7D is reserved as address pin SA for 288 Mb devices. It is a true no connect in this device.
9. Pin 5U is reserved as address pin SA for 576 Mb devices. It is a true no connect in this device.
10. Pin 9U is reserved as address pin SA for 1152 Mb devices. It is a true no connect in this device.

**4M x 36 Pinout (Top View)**

|          | 1               | 2                | 3                | 4                | 5               | 6                        | 7                | 8                | 9               | 10               | 11               | 12               | 13              |
|----------|-----------------|------------------|------------------|------------------|-----------------|--------------------------|------------------|------------------|-----------------|------------------|------------------|------------------|-----------------|
| <b>A</b> | V <sub>DD</sub> | QINV3            | V <sub>DD</sub>  | DINV3            | NC<br>(RSVD)    | MCL<br>(CFG)             | MRW              | ZQ               | PZT1            | DINV0            | V <sub>DD</sub>  | QINV0            | V <sub>DD</sub> |
| <b>B</b> | V <sub>SS</sub> | Q35              | V <sub>SS</sub>  | D35              | MCL             | MCL<br>(B4M)             | NC<br>(RSVD)     | MCH<br>(SIOM)    | PZT0            | D0               | V <sub>SS</sub>  | Q0               | V <sub>SS</sub> |
| <b>C</b> | Q26             | V <sub>DDQ</sub> | D26              | V <sub>DDQ</sub> | V <sub>SS</sub> | SA13                     | V <sub>DD</sub>  | SA14             | V <sub>SS</sub> | V <sub>DDQ</sub> | D9               | V <sub>DDQ</sub> | Q9              |
| <b>D</b> | V <sub>SS</sub> | Q34              | V <sub>SS</sub>  | D34              | SA19            | V <sub>DDQ</sub>         | NC<br>(288 Mb)   | V <sub>DDQ</sub> | SA20            | D1               | V <sub>SS</sub>  | Q1               | V <sub>SS</sub> |
| <b>E</b> | Q25             | V <sub>DDQ</sub> | D25              | V <sub>DD</sub>  | V <sub>SS</sub> | SA11                     | V <sub>SS</sub>  | SA12             | V <sub>SS</sub> | V <sub>DD</sub>  | D10              | V <sub>DDQ</sub> | Q10             |
| <b>F</b> | V <sub>SS</sub> | Q33              | V <sub>SS</sub>  | D33              | SA17            | V <sub>DD</sub>          | V <sub>DDQ</sub> | V <sub>DD</sub>  | SA18            | D2               | V <sub>SS</sub>  | Q2               | V <sub>SS</sub> |
| <b>G</b> | Q24             | Q32              | D24              | D32              | V <sub>SS</sub> | SA9                      | NU <sub>I</sub>  | SA10             | V <sub>SS</sub> | D3               | D11              | Q3               | Q11             |
| <b>H</b> | Q23             | V <sub>DDQ</sub> | D23              | V <sub>DDQ</sub> | SA15            | V <sub>DDQ</sub>         | $\bar{W}$        | V <sub>DDQ</sub> | SA16            | V <sub>DDQ</sub> | D12              | V <sub>DDQ</sub> | Q12             |
| <b>J</b> | V <sub>SS</sub> | Q31              | V <sub>SS</sub>  | D31              | V <sub>SS</sub> | SA7                      | V <sub>SS</sub>  | SA8              | V <sub>SS</sub> | D4               | V <sub>SS</sub>  | Q4               | V <sub>SS</sub> |
| <b>K</b> | CQ1             | V <sub>DDQ</sub> | V <sub>REF</sub> | V <sub>DD</sub>  | KD1             | V <sub>DD</sub>          | CK               | V <sub>DD</sub>  | KD0             | V <sub>DD</sub>  | V <sub>REF</sub> | V <sub>DDQ</sub> | CQ0             |
| <b>L</b> | $\bar{CQ1}$     | V <sub>SS</sub>  | QVLD1            | V <sub>SS</sub>  | $\bar{KD1}$     | V <sub>DDQ</sub>         | $\bar{CK}$       | V <sub>DDQ</sub> | $\bar{KD0}$     | V <sub>SS</sub>  | QVLD0            | V <sub>SS</sub>  | $\bar{CQ0}$     |
| <b>M</b> | V <sub>SS</sub> | Q22              | V <sub>SS</sub>  | D22              | V <sub>SS</sub> | SA5                      | V <sub>SS</sub>  | SA6              | V <sub>SS</sub> | D13              | V <sub>SS</sub>  | Q13              | V <sub>SS</sub> |
| <b>N</b> | Q30             | V <sub>DDQ</sub> | D30              | V <sub>DDQ</sub> | PLL             | V <sub>DDQ</sub>         | $\bar{R}$        | V <sub>DDQ</sub> | MCL             | V <sub>DDQ</sub> | D5               | V <sub>DDQ</sub> | Q5              |
| <b>P</b> | Q29             | Q21              | D29              | D21              | V <sub>SS</sub> | SA3                      | MZT              | SA4              | V <sub>SS</sub> | D14              | D6               | Q14              | Q6              |
| <b>R</b> | V <sub>SS</sub> | Q20              | V <sub>SS</sub>  | D20              | MCH             | V <sub>DD</sub>          | V <sub>DDQ</sub> | V <sub>DD</sub>  | RST             | D15              | V <sub>SS</sub>  | Q15              | V <sub>SS</sub> |
| <b>T</b> | Q28             | V <sub>DDQ</sub> | D28              | V <sub>DD</sub>  | V <sub>SS</sub> | SA1                      | V <sub>SS</sub>  | SA2              | V <sub>SS</sub> | V <sub>DD</sub>  | D7               | V <sub>DDQ</sub> | Q7              |
| <b>U</b> | V <sub>SS</sub> | Q19              | V <sub>SS</sub>  | D19              | NC<br>(576 Mb)  | V <sub>DDQ</sub>         | NC<br>(RSVD)     | V <sub>DDQ</sub> | NC<br>(1152 Mb) | D16              | V <sub>SS</sub>  | Q16              | V <sub>SS</sub> |
| <b>V</b> | Q27             | V <sub>DDQ</sub> | D27              | V <sub>DDQ</sub> | V <sub>SS</sub> | NU <sub>I</sub><br>(x18) | V <sub>DD</sub>  | SA0<br>(B2)      | V <sub>SS</sub> | V <sub>DDQ</sub> | D8               | V <sub>DDQ</sub> | Q8              |
| <b>W</b> | V <sub>SS</sub> | Q18              | V <sub>SS</sub>  | D18              | TCK             | MCL                      | RCS              | MCL              | TMS             | D17              | V <sub>SS</sub>  | Q17              | V <sub>SS</sub> |
| <b>Y</b> | V <sub>DD</sub> | QINV2            | V <sub>DD</sub>  | DINV2            | TDO             | NU                       | NC<br>(RSVD)     | MCL              | TDI             | DINV1            | V <sub>DD</sub>  | QINV1            | V <sub>DD</sub> |

**Notes:**

1. Pins 5B, 6W, 8W, 8Y, and 9N must be tied Low in this device.
2. Pin 5R must be tied High in this device.
3. Pin 6A is defined as mode pin CFG in the pinout standard. It must be tied Low in this device to select x36 configuration.
4. Pin 6B is defined as mode pin B4M in the pinout standard. It must be tied Low in this device to select Burst-of-2 configuration.
5. Pin 8B is defined as mode pin SIOM in the pinout standard. It must be tied High in this device to select Separate I/O configuration.
6. Pin 6V is defined as address pin SA for x18 devices. It is unused in this device, and must be left unconnected or driven High.
7. Pin 8V is defined as address pin SA for B2 devices. It is used in this device.
8. Pin 7D is reserved as address pin SA for 288 Mb devices. It is a true no connect in this device.
9. Pin 5U is reserved as address pin SA for 576 Mb devices. It is a true no connect in this device.
10. Pin 9U is reserved as address pin SA for 1152 Mb devices. It is a true no connect in this device.

### Pin Description

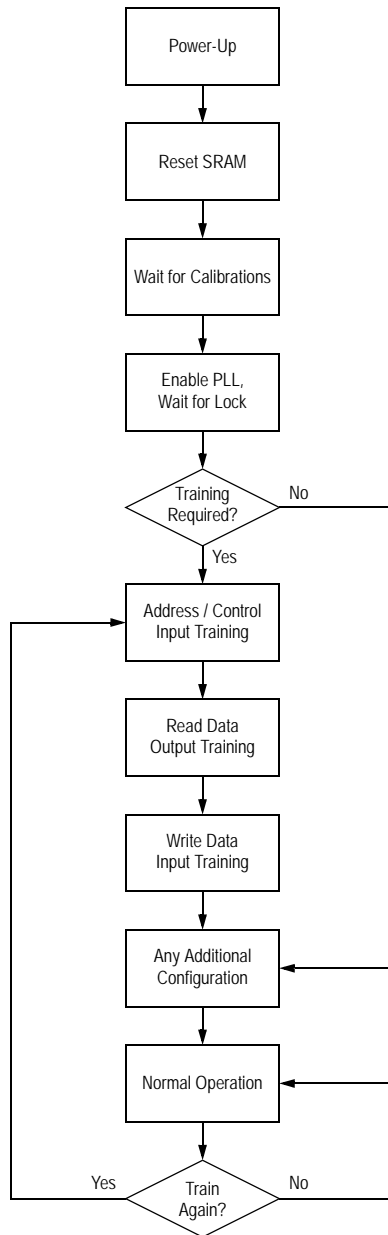
| Symbol                                   | Description   | Type   |
|--|---|--------|
| SA[21:0]                                 | <b>Address</b> — Read address is registered on $\uparrow\text{CK}$ and write address is registered on $\uparrow\overline{\text{CK}}$ .  | Input  |
| D[35:0]                                  | <b>Write Data</b> — Registered on $\uparrow\text{KD}$ and $\uparrow\overline{\text{KD}}$ during Write operations.<br>D[17:0] - x18 and x36.<br>D[35:18] - x36 only.   | Input  |
| DINV[3:0]                                | <b>Write Data Inversion</b> — Registered on $\uparrow\text{KD}$ and $\uparrow\overline{\text{KD}}$ (along with write data) during Write operations. Indicate if the associated write data byte is inverted (DINVx = 1) or not (DINVx = 0).<br>DINV0 - associated with D[8:0] in x18 and x36.<br>DINV1 - associated with D[17:9] in x18 and x36.<br>DINV2 - associated with D[26:18] in x36 only.<br>DINV3 - associated with D[35:27] in x36 only.<br><b>Note:</b> Treated as NU inputs when Data Inversion is disabled. | Input  |
| Q[35:0]                                  | <b>Read Data</b> — Aligned with $\uparrow\text{CQ}$ and $\uparrow\overline{\text{CQ}}$ during Read operations.<br>Q[17:0] - x18 and x36.<br>Q[35:18] - x36 only.  | Output |
| QINV[3:0]                                | <b>Read Data Inversion</b> — Aligned with $\uparrow\text{CQ}$ and $\uparrow\overline{\text{CQ}}$ (along with read data) during Read operations. Indicate if the associated read data byte is inverted (QINVx = 1) or not (QINVx = 0).<br>QINV0 - associated with Q[8:0] in x18 and x36.<br>QINV1 - associated with Q[17:9] in x18 and x36.<br>QINV2 - associated with Q[26:18] in x36 only.<br>QINV3 - associated with Q[35:27] in x36 only.<br><b>Note:</b> Treated as NU outputs when Data Inversion is disabled.     | Output |
| QVLD[1:0]                                | <b>Read Data Valid</b> — Driven high one half cycle before valid read data.   | Output |
| CK, $\overline{\text{CK}}$               | <b>Primary Input Clocks</b> — Dual single-ended. Used for latching address and control inputs, for internal timing control, and for output timing control.  | Input  |
| $\overline{\text{KD}}$ [1:0],<br>KD[1:0] | <b>Write Data Input Clocks</b> — Dual single-ended. Used for latching write data inputs.<br>KD0, $\overline{\text{KD}}$ 0: latch D[17:0], DINV[1:0] in x36, and D[8:0], DINV0 in x18.<br>KD1, $\overline{\text{KD}}$ 1: latch D[35:18], DINV[3:2] in x36, and D[17:9], DINV1 in x18.  | Input  |
| $\overline{\text{CQ}}$ [1:0],<br>CQ[1:0] | <b>Read Data Output Clocks</b> — Free-running output (echo) clocks, tightly aligned with read data outputs. Facilitate source-synchronous operation.<br>$\overline{\text{CQ}}$ 0, CQ0: align with Q[17:0], QINV[1:0] in x36, and Q[8:0], QINV0 in x18.<br>CQ1, $\overline{\text{CQ}}$ 1: align with Q[35:18], QINV[3:2] in x36, and Q[17:9], QINV1 in x18.  | Output |
| $\overline{\text{R}}$                    | <b>Read Enable</b> — Registered on $\uparrow\text{CK}$ . See the Clock Truth Table for functionality.   | Input  |
| $\overline{\text{W}}$                    | <b>Write Enable</b> — Registered on $\uparrow\text{CK}$ . See the Clock Truth Table for functionality.  | Input  |
| MRW                                      | <b>Mode Register Write</b> — Registered on $\uparrow\text{CK}$ . Can be used synchronously or asynchronously to enable Register Write Mode. See the State and Clock Truth Tables for functionality.   | Input  |
| PLL                                      | <b>PLL Enable</b> — Weakly pulled High internally.<br>PLL = 0: disables internal PLL.<br>PLL = 1: enables internal PLL.   | Input  |
| RST                                      | <b>Reset</b> — Holds the device inactive and resets the device to its initial power-on state when asserted High. Weakly pulled Low internally.  | Input  |

| Symbol    | Description  | Type   |
|-----------|--|--------|
| ZQ        | <b>Driver / ODT Impedance Control Resistor Input</b> — Must be connected to $V_{SS}$ through an external resistor RQ to program driver and ODT impedances.   | Input  |
| RCS       | <b>Current Source Resistor Input</b> — Must be connected to $V_{SS}$ through an external $2k\Omega$ resistor to provide an accurate current source for the PLL.  | Input  |
| MZT       | <b>ODT Mode Select</b> — Sets the default ODT state globally for all input groups during power-up and reset. Must be tied High or Low.<br>MZT = 0: disables ODT on all input groups, regardless of PZT[1:0].<br>MZT = 1: enables ODT on select input groups, as specified by PZT[1:0].<br><b>Note:</b> The ODT state for each input group can be changed at any time via the Configuration Registers.  | Input  |
| PZT[1:0]  | <b>ODT Configuration Select</b> — Set the default ODT state for various combinations of input groups during power-up and reset, when MZT = 1. Must be tied High or Low.<br>PZT[1:0] = 00: enables ODT on write data only.<br>PZT[1:0] = 01: enables ODT on write data and input clocks.<br>PZT[1:0] = 10: enables ODT on write data, address, and control.<br>PZT[1:0] = 11: enables ODT on write data, input clocks, address, and control.<br><b>Note:</b> The ODT state for each input group can be changed at any time via the Configuration Registers. | Input  |
| $V_{DD}$  | <b>Core Power Supply</b>   | —      |
| $V_{DDQ}$ | <b>I/O Power Supply</b>  | —      |
| $V_{REF}$ | <b>Input Reference Voltage</b> — Input buffer reference voltage.   | —      |
| $V_{SS}$  | <b>Ground</b>  | —      |
| TCK       | <b>JTAG Clock</b> — Weakly pulled Low internally.  | Input  |
| TMS       | <b>JTAG Mode Select</b> — Weakly pulled High internally.   | Input  |
| TDI       | <b>JTAG Data Input</b> — Weakly pulled High internally.  | Input  |
| TDO       | <b>JTAG Data Output</b>  | Output |
| MCH       | <b>Must Connect High</b> — May be tied to $V_{DDQ}$ directly or via a $1k\Omega$ resistor.   | Input  |
| MCL       | <b>Must Connect Low</b> — May be tied to $V_{SS}$ directly or via a $1k\Omega$ resistor.   | Input  |
| NC        | <b>No Connect</b> — There is no internal chip connection to these pins. They may be left unconnected, or tied/driven High or Low.  | —      |
| $NU_i$    | <b>Not Used Input</b> — There is an internal chip connection to these input pins, but they are unused by the device. They are pulled High internally. They may be left unconnected or tied/driven High. They should not be tied/driven Low.  | Input  |
| $NU_o$    | <b>Not Used Output</b> — There is an internal chip connection to these output pins, but they are unused by the device. The drivers are tri-stated internally. They should be left unconnected.   | Output |

## Initialization Summary

Prior to functional use, these devices must first be initialized and configured. The steps described below will ensure that the internal logic has been properly reset, and that functional timing parameters have been configured.

### Flow Chart



### Notes:

1. MZT and PZT[1:0] mode pins are used to set the default ODT state of all input groups at power-up, and whenever RST is asserted High. The ODT state for each input group can be changed any time thereafter using Register Write Mode to program certain bits in the Configuration Registers.
2. Calibrations are performed for driver impedance, ODT impedance, and the PLL current source immediately after RST is de-asserted Low. The calibrations can take up to 384K cycles total. See the Power-Up and Reset Requirements section for more information.
3. The PLL can be enabled by the PLL pin, or by the PLL Enable (PLE) bit in the Configuration Registers. See the PLL Operation section for more information.
4. If the PLE bit is used to enable the PLL, then Register Write Mode will likely have to be utilized in the "Asynchronous, Pre-Input Training" method, since Address / Control Input Training has not yet been performed. See the Configuration Registers section for more information.
5. It can take up to 64K cycles for the PLL to lock after it has been enabled.
6. It is expected that a Loopback Mode (one of the two supported) will be used for Address / Control Input Training. If so, the Loopback Mode is selected and enabled using Register Write Mode to program certain bits in the Configuration Registers. And, Register Write Mode will likely have to be utilized in the "Asynchronous, Pre-Input Training" method, since Address / Control Input Training has not yet been performed.
7. Loopback Mode can also be used for Read Data Output Training, if desired. See the Signal Timing Training and Loopback Mode sections for more information.
8. "Any Additional Configuration" might include enabling Data Inversion, for example. Since this step is performed after Address / Control Input Training, Register Write Mode can be utilized in the "Asynchronous, Post-Input Training" method (or perhaps the "Synchronous" method, if the synchronous timing requirements can be met at the particular operating frequency).
9. It is up to the system to determine if/when re-training is necessary.

## Power-Up and Reset Requirements

For reliability purposes, power supplies must power up simultaneously, or in the following sequence:

$V_{SS}$ ,  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{REF}$  and inputs.

Power supplies must power down simultaneously, or in the reverse sequence.

After power supplies power up, the following start-up sequence must be followed.

**Step 1:** Assert RST High for at least 1ms.

While RST is asserted high:

- The PLL is disabled.
- The states of  $\overline{R}$ ,  $\overline{W}$ , and MRW control inputs are ignored.

**Note:** If possible, RST should be asserted High before input clocks begin toggling, and remain asserted High until input clocks are stable and toggling within specification, in order to prevent unstable, out-of-spec input clocks from causing trouble in the SRAM.

**Step 2:** Begin toggling input clocks.

After input clocks begin toggling, but not necessarily within specification:

- Q are placed in the non-Read state, and remain so until the first Read operation.
- QVLD are driven Low, and remain so until the first Read operation.
- CQ,  $\overline{CQ}$  begin toggling, but not necessarily within specification.

**Step 3:** Wait until input clocks are stable and toggling within specification.

**Step 4:** De-assert RST Low.

**Step 5:** Wait at least 384K (393,216) cycles.

During this time:

- Driver and ODT impedances are calibrated. Can take up to 320K cycles.
- The current source for the PLL is calibrated (based on RCS pin). Can take up to 64K cycles.

**Step 6:** Enable the PLL.

**Step 7:** Wait at least 64K (65,536) cycles for the PLL to lock.

After the PLL has locked:

- CQ,  $\overline{CQ}$  begin toggling within specification.

**Step 8:** Continue initialization (see the Initialization Flow Chart).

## Reset Usage

Although not generally recommended, RST may be asserted High at any time after completion of the initial power-up sequence described above, to reset the SRAM control logic to its initial power-on state. However, whenever RST is subsequently de-asserted Low, as in step 4 above, steps 5~7 above must be followed before normal operation is resumed. It is up to the system to determine whether further re-initialization beyond step 7 (as outlined in the Initialization Flow Chart) is required before normal operation is resumed.

**Note:** Memory array content may be perturbed/corrupted when RST is asserted High.

## PLL Operation

A PLL is implemented in these devices to control all output timing. It uses the CK input clock as a source, and is enabled when all of the following conditions are met:

1. RST is de-asserted Low, and
2. Either the PLL Enable pin (PLL) or the PLL Enable register bit (PLE) is asserted High, and
3. CK cycle time is within the configured operating frequency range. See the PLL OFR Configuration table below.

Once enabled, the PLL requires 64K stable clock cycles in order to lock/synchronize properly.

When the PLL is enabled, it aligns output clocks and read data to input clocks (with some fixed delay), and it generates all mid-cycle output timing. See the Output Timing section for more information.

The PLL can tolerate changes in input clock frequency due to clock jitter (i.e. such jitter will not cause the PLL to lose lock/synchronization), provided the cycle-to-cycle jitter does not exceed 200ps (see “ $t_{KJITcc}$ ” in the AC Timing Specifications section for more information). However, the PLL must be resynchronized (i.e. disabled and then re-enabled) whenever the nominal input clock frequency is changed.

The PLL is disabled when any of the following conditions are met:

1. RST is asserted High, or
2. Both the PLL Enable pin (PLL) and the PLL Enable register bit (PLE) are deasserted Low, or
3. CK is stopped for at least 30ns, or CK cycle time  $\geq 30ns$ .

### PLL Operating Frequency Range (OFR) Configuration

Three register bits - OFR[2:0] - have been defined to specify the frequency range at which the device is operated, and must be programmed to configure the PLL properly.

|                              | OFR2 | OFR1 | OFR0 | $t_{KHKH}$ (min) | $t_{KHKH}$ (max) |
|------------------------------|------|------|------|------------------|------------------|
| Operating Frequency Range #1 | 0    | 0    | 0    | 100 MHz          | 170 MHz          |
| Operating Frequency Range #2 | 0    | 0    | 1    | 170 MHz          | 250 MHz          |
| Operating Frequency Range #3 | 0    | 1    | 0    | 250 MHz          | 350 MHz          |
| Operating Frequency Range #4 | 0    | 1    | 1    | 350 MHz          | 480 MHz          |
| Operating Frequency Range #5 | 1    | 0    | 0    | 480 MHz          | 680 MHz          |
| Operating Frequency Range #6 | 1    | 0    | 1    | 680 MHz          | 910 MHz          |
| Operating Frequency Range #7 | 1    | 1    | 0    | 910 MHz          | 1150 MHz         |
| Operating Frequency Range #8 | 1    | 1    | 1    | 1150 MHz         | 1400 MHz         |

### PLL OFR Bit Change Sequence

The following sequence must be followed whenever the OFR[2:0] register bits are changed to select/program a new operating frequency range, and input clock frequency is changed to within the new range.

**Prior to Step 1:** OFR[2:0] are set to OF Range “A”. Input clock frequency is within OF Range “A”.

**Step 1:** Disable the PLL via PLL pin = 0 and PLE register bit = 0.

**Step 2:** Change OFR[2:0] to select/program OF Range “B”.

**Step 3:** Change input clock frequency to within OF Range “B”.

**Step 4:** Re-enable the PLL via PLL pin = 1 or PLE register bit = 1.

**Step 5:** Wait at least 64K cycles for the PLL to resynchronize to the new operating frequency.

## Configuration Registers

These devices utilize a set of registers for device configuration. The configuration registers are written via **Register Write Mode**, which is initiated by asserting MRW High and  $\bar{R}$  Low. When Register Write Mode is utilized, up to sixteen distinct 6-bit registers can be programmed using SDR timing on the SA[10:1] address input pins. The D data input pins are not used.

**Note:** Register Write Mode only provides the ability to write the configuration registers. The ability to read the configuration registers is provided via a private JTAG instruction and register. Please contact GSI for more information.

Register Write Mode can be utilized in two ways:

1. **Asynchronous Method:** MRW is driven asynchronously, such that it does not meet setup and hold time specs to  $\uparrow$ CK.
2. **Synchronous Method:** MRW is driven synchronously, such that it meets setup and hold time specs to  $\uparrow$ CK.

Regardless how Register Write Mode is utilized, at least 16 NOPs must be initiated before beginning a Register Write sequence, to ensure any previous Read and Write operations are completed before the sequence begins. And, at least 16 NOPs must be initiated after completing a Register Write sequence and before initiating Read and Write operations, and before utilizing Loopback Mode, to allow sufficient time for the newly programmed register settings to take effect.

### Register Write Mode Utilization - Asynchronous Method

Register Write Mode can be utilized asynchronously up to the full operating speed of the device. When Register Write Mode is utilized asynchronously, there are two cases to consider:

1. **Pre Input Training:** SA[10:1],  $\bar{R}$ ,  $\bar{W}$  are driven such that they do not meet setup and hold time specs to  $\uparrow$ CK.
2. **Post Input Training:** SA[10:1],  $\bar{R}$ ,  $\bar{W}$  are driven such that they meet setup and hold time specs to  $\uparrow$ CK.

Each case is examined separately below.

#### Pre Input Training Requirements

In this case, MRW,  $\bar{R}$ ,  $\bar{W}$ , and SA[10:1] are all driven asynchronously. When Register Write Mode is utilized in this manner, only one register can be programmed during any particular instance that MRW is asserted High.

The requirements for this usage case are as follows:

- At least 16 NOPs must be initiated before and after the Register Write sequence.
- MRW High must meet minimum pulse width requirements (tMRWPW).
- $\bar{R}$  Low and SA[10:1] Valid must meet minimum setup time requirements (tMRWS) to MRW High.
- $\bar{R}$  Low and SA[10:1] Valid must meet minimum hold time requirements (tMRWH) from MRW Low.
- $\bar{W}$  High must also meet minimum setup time requirements (tMRWS) to MRW High, if inadvertent memory writes are to be prevented during the Register Write process. Otherwise,  $\bar{W}$  state is “don’t care”.
- $\bar{W}$  High must also meet minimum hold time requirements (tMRWH) from MRW Low, if inadvertent memory writes are to be prevented during the Register Write process. Otherwise,  $\bar{W}$  state is “don’t care”.

**Note:** tMRWPW = tMRWS = tMRWH = 4 cycles (minimum).

**Note:** Inadvertent memory reads will occur while MRW and  $\bar{R}$  are Low during the Register Write process. The memory reads are harmless, and can be ignored.

### Post Input Training Requirements

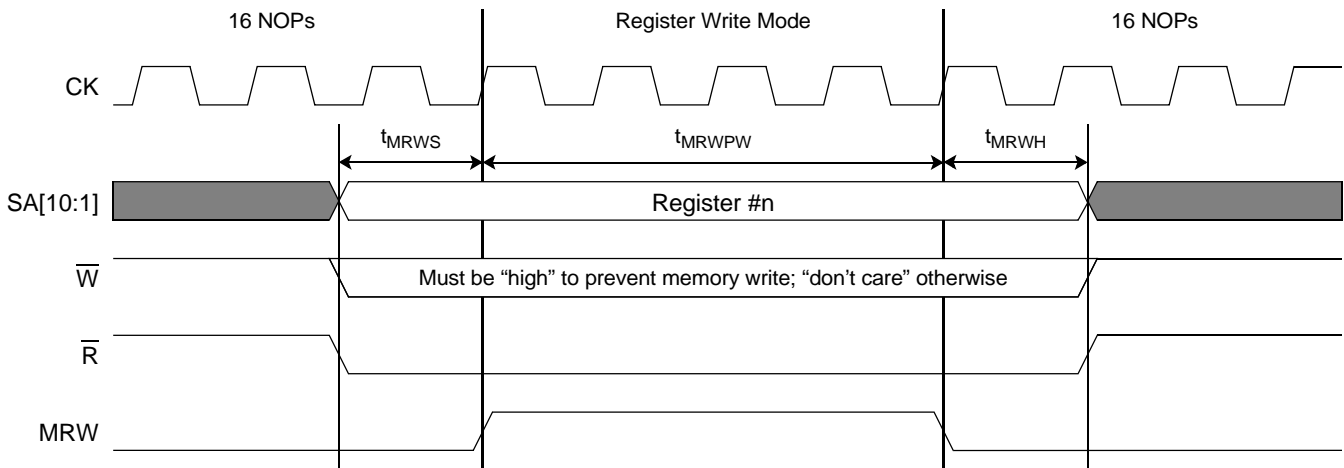
In this case, MRW is driven asynchronously, whereas  $\bar{R}$ ,  $\bar{W}$ , and SA[10:1] are all driven synchronously (i.e. they all meet setup and hold time specs to  $\uparrow\text{CK}$ ). When Register Write Mode is utilized in this manner, multiple registers can be programmed during any particular instance that MRW is asserted High. The timing diagrams below arbitrarily show four registers programmed while MRW is asserted High, but in practice it can be any number greater than or equal to one.

The requirements for this usage case are as follows:

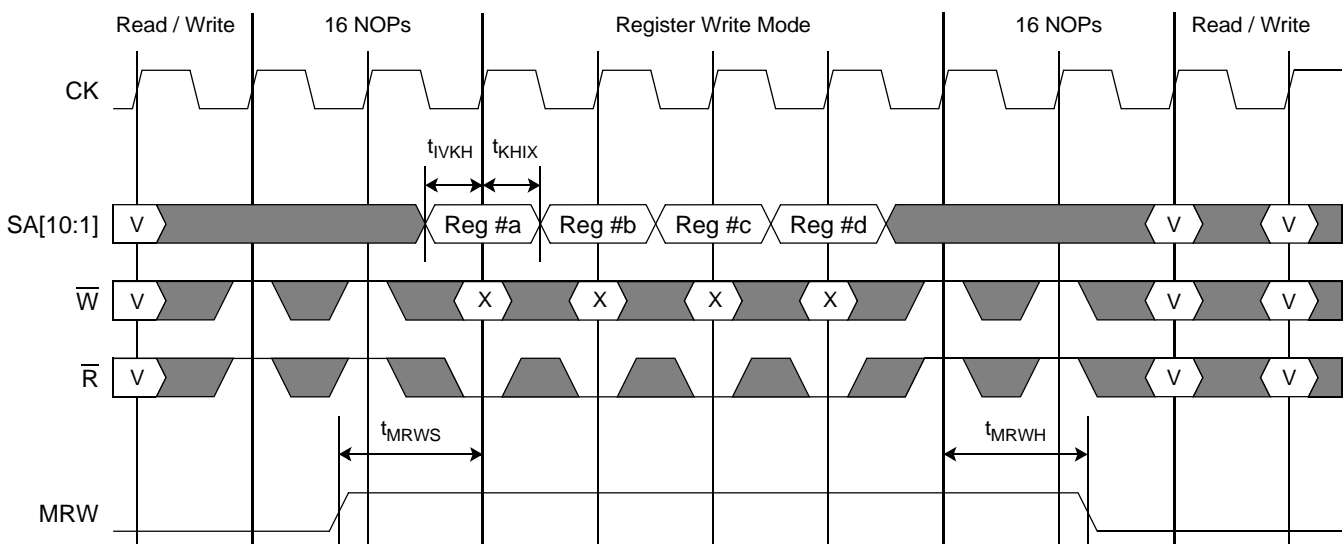
- At least 16 NOPs must be initiated before and after the Register Write(s).
- MRW High must meet minimum setup time requirements ( $t_{\text{MRWS}}$ ) to the  $\uparrow\text{CK}$  that generates the first Register Write.
- MRW High must meet minimum hold time requirements ( $t_{\text{MRWH}}$ ) from the  $\uparrow\text{CK}$  that generates the first NOP after the last Register Write.
- $\bar{R}$  must be driven Low (synchronously) and SA[10:1] must be driven Valid (synchronously) for each Register Write.
- $\bar{W}$  state is a “don’t care” (synchronously) for each Register Write.

**Note:**  $t_{\text{MRWS}} = t_{\text{MRWH}} = 4$  cycles (minimum).

### Asynchronous Register Write Timing Diagram - Pre Input Training



### Asynchronous Register Write Timing Diagram - Post Input Training



### Register Write Mode Utilization - Synchronous Method

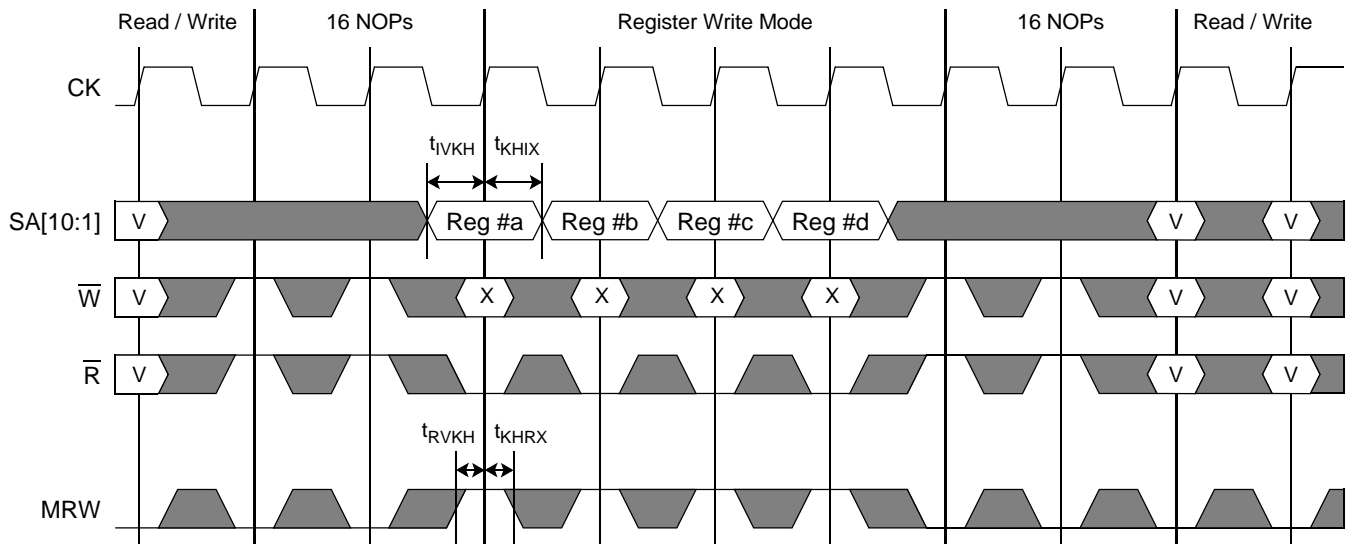
Register Write Mode can also be utilized synchronously up to the full operating speed of the device. However, MRW cannot be trained using Loopback Mode, so the ability to use it synchronously may be limited to slower operating frequencies where the lack of training capability is less problematic for the user.

In this case, MRW,  $\bar{R}$ ,  $\bar{W}$ , and SA[10:1] are all driven synchronously (i.e. they all meet setup and hold time specs to  $\uparrow\text{CK}$ ). When Register Write Mode is utilized in this manner, multiple registers can be programmed in successive cycles. The timing diagrams below arbitrarily show four registers programmed in successive cycles, but in practice it can be any number greater than or equal to one.

The requirements for this usage case are as follows:

- At least 16 NOPs must be initiated before and after the Register Write(s).
- MRW must be driven High (synchronously),  $\bar{R}$  must be driven Low (synchronously), and SA[10:1] must be driven Valid (synchronously) for each Register Write.
- $\bar{W}$  state is a “don’t care” (synchronously) for each Register Write.

**Synchronous Register Write Timing Diagram**



## Register Description

As described previously, Register Write Mode provides the ability to program up to sixteen distinct 6-bit configuration registers using SDR timing on the SA[10:1] address input pins. Specifically, SA[4:1] are used to select one of the sixteen distinct registers, and SA[10:5] are used to program the six data bits of the selected register.

The registers are defined as follows:

| Address   | SA10                               | SA9 | SA8      | SA7      | SA6 | SA5  | SA4                      | SA3 | SA2 | SA1 | Reg #   |
|-----------|------------------------------------|-----|----------|----------|-----|------|--------------------------|-----|-----|-----|---------|
| Pin       | 8G                                 | 6G  | 8J       | 6J       | 8M  | 6M   | 8P                       | 6P  | 8T  | 6T  |         |
| Bit Usage | Register Data Bits                 |     |          |          |     |      | Register Select Bits     |     |     |     |         |
| Active    |                                    | DI  |          |          |     | RLM  | 0                        | 0   | 0   | 0   | 1       |
| Active    |                                    |     | OFR[2:0] |          |     | PLE  | 0                        | 0   | 0   | 1   | 2       |
| Active    |                                    |     |          | LBK[1:0] |     | LBKE | 0                        | 0   | 1   | 0   | 3       |
| Active    |                                    | DZT |          | KDZT     |     | CKZT | 0                        | 0   | 1   | 1   | 4       |
| Active    |                                    |     |          | CZT      |     | AZT  | 0                        | 1   | 0   | 0   | 5       |
| Unused    |                                    |     |          |          |     |      | All Others except "111X" |     |     |     | 6 ~ 14  |
| Active    | Reserved for GSI Internal Use Only |     |          |          |     |      | 1                        | 1   | 1   | X   | 15 ~ 16 |

**Note:** Registers #15 and #16 are reserved for GSI internal use only. Users should not access these registers.

## Register Bit Definitions

| Read Latency Select |                         |
|---------------------|-------------------------|
| RLM                 |                         |
| 0                   | Read Latency = 5 cycles |
| 1                   | Read Latency = 6 cycles |
| 1                   | POR/RST Default         |

| Data Inversion Enable |                        |
|-----------------------|------------------------|
| DI                    |                        |
| 0                     | Disable Data Inversion |
| 1                     | Enable Data Inversion  |
| 0                     | POR/RST Default        |

| PLL Enable |                             |
|------------|-----------------------------|
| PLE        |                             |
| 0          | Disable PLL, if PLL pin = 0 |
| 1          | Enable PLL                  |
| 0          | POR/RST Default             |

| Loopback Mode Enable |                       |
|----------------------|-----------------------|
| LBKE                 |                       |
| 0                    | Disable Loopback Mode |
| 1                    | Enable Loopback Mode  |
| 0                    | POR/RST Default       |

**Note:** The default state of OFR[2:0] is set depending on the speed grade of the part. For example, in a 1200 MHz speed grade part, OFR[2:0] defaults to the setting applicable to 1200 MHz operation.

| PLL Operating Frequency Range |                          |
|-------------------------------|--------------------------|
| OFR[2:0]                      |                          |
| 000                           | Configure PLL for OFR #1 |
| 001                           | Configure PLL for OFR #2 |
| ...                           | ....                     |
| 111                           | Configure PLL for OFR #8 |
| See Note                      | POR/RST Default          |

| Loopback Mode Select |   |                                   |
|----------------------|---|-----------------------------------|
| LBK[1:0]             |   |                                   |
| 0                    | 0 | XOR Loopback Mode, input group #1 |
| 0                    | 1 | XOR Loopback Mode, input group #2 |
| 1                    | 0 | INV Loopback Mode, input group #1 |
| 1                    | 1 | INV Loopback Mode, input group #2 |
| 0                    | 0 | POR/RST Default                   |

**Note:** In the ODT Control register bit definitions below, MZT and PZT[1:0] pins set the default state of the register bits at power-up and whenever RST is asserted High. The register bits can then be overwritten (via Register Write Mode), while RST is de-asserted Low, to change the state of the feature controlled by the register bits.

| Input Clock ODT Control                                 |                              |
|---|------------------------------|
| CKZT  |                              |
| KDZT  |                              |
| 0   | disabled                     |
| 1   | enabled: $PU = 0.3 \cdot RQ$ |
| 0, if MZT = 0 or PZT0 = 0<br>1, if MZT = 1 and PZT0 = 1 | POR/RST Default              |

| Address & Control ODT Control                           |                              |
|---|------------------------------|
| AZT   |                              |
| CZT   |                              |
| 0   | disabled                     |
| 1   | enabled: $PU = 0.3 \cdot RQ$ |
| 0, if MZT = 0 or PZT1 = 0<br>1, if MZT = 1 and PZT1 = 1 | POR/RST Default              |

| Write Data ODT Control         |                              |
|--------------------------------|------------------------------|
| DZT                            |                              |
| 0                              | disabled                     |
| 1                              | enabled: $PU = 0.3 \cdot RQ$ |
| 0, if MZT = 0<br>1, if MZT = 1 | POR/RST Default              |

## Signal Timing Training

Signal timing training (aka “deskew”) is often required for reliable signal transmission between components at the I/O speeds supported by these devices. Typically, the timing training is performed in the following sequence:

Step 1: Address / Control input training.

These devices support a special Loopback Mode of operation to facilitate address / control input training.

Step 2: Read Data output training.

These devices support a special Loopback Mode of operation to facilitate read data output training.

Alternatively, slow-frequency Memory Write operations can be used to store DDR data patterns in the memory array reliably (full-frequency Memory Write operations cannot be used because write data signals have not been trained yet), and full-frequency Memory Read operations can then be used to train the read data output signals.

Step 3: Write Data input training.

Since address, control, and read data signals have already been trained at this point, full-frequency Memory Write and Read operations can then be used to train the write data inputs.

## Loopback Mode

These devices support two distinct **Loopback Modes** of operation, which can be used to:

1. Perform per-pin training on the address ( $SA$ ), control ( $\overline{R}$ ,  $\overline{W}$ ), and write data clock ( $KD$ ,  $\overline{KD}$ ) inputs.
2. Perform per-pin training on the data ( $Q$ ,  $QINV$ ) outputs.

In both cases,  $SA$ ,  $\overline{R}$ ,  $\overline{W}$ ,  $KD$ ,  $\overline{KD}$  input pin values are sampled, logically manipulated, and looped back to  $Q$ ,  $QINV$  output pins.

Register bit  $LBKE$  is used to enable/disable Loopback Mode. When  $LBKE = 1$  and  $MRW = 0$ , Loopback Mode is enabled, and Memory Read and Write operations are blocked regardless of the states of  $\overline{R}$  and  $\overline{W}$ . When  $LBKE = 0$  or  $MRW = 1$ , Loopback Mode is disabled. See the State Truth Table for more information.

Register bits  $LBK[1:0]$  are used to select between the two distinct Loopback Modes supported by the design (controlled by  $LBK1$ ), and between the two groups of inputs used during the selected Loopback Mode (controlled by  $LBK0$ ), as follows:

- $LBK[1:0] = 00$ : selects XOR LBK Mode using Input Group 1. Loopback Mode “00”.
- $LBK[1:0] = 01$ : selects XOR LBK Mode using Input Group 2. Loopback Mode “01”.
- $LBK[1:0] = 10$ : selects INV LBK Mode using Input Group 1. Loopback Mode “10”.
- $LBK[1:0] = 11$ : selects INV LBK Mode using Input Group 2. Loopback Mode “11”.

**Note:** For convenience,  $KD$  clocks have been included in the group of inputs that can be trained via Loopback Mode. However, the timing requirement for  $KD$  clocks is that their edges be tightly aligned to  $CK$  clock edges, unlike the timing requirement for address/control signals, whose edges must be centered (approximately) between  $CK$  edges in order to optimize setup and hold times to those  $CK$  edges. Consequently, it is questionable whether Loopback mode can be used to train  $KD$  clocks effectively.

**Note:** When Loopback Mode is enabled, Data Inversion is disabled regardless of the state of register bit  $DI$ .

## Loopback Latency

Loopback Latency (“ $LBKL$ ”) - i.e. the number of cycles from when the inputs are sampled to when the proper result appears on the output pins, is equal to “ $RL+2$ ” cycles. That is, it equals 8 cycles when  $RL=6$ , and it equals 7 cycles when  $RL=5$ .

## Enabling Loopback Mode

Loopback Mode is enabled as follows:

Step 1: Initiate a Register Write operation with  $SA[10:1] = “000ab1.0010”$  to select Register #2, set  $LBKE = 1$  to enable Loopback Mode, and set  $LBK[1:0]$  to “ab” to select Loopback Mode “ab”.

Step 2: Wait 16 cycles for new register settings to take effect.

Loopback Mode “ab” is enabled after step 2 because  $MRW = 0$ ,  $LBKE = 1$ , and  $LBK[1:0] = “ab”$ .

### Changing Loopback Modes

Once enabled, Loopback Mode can be changed as follows

Step 1: Initiate a Register Write operation with SA[10:1] = “000cd1.0010” to select Register #2, keep LBKE = 1 to keep Loopback Mode enabled, and set LBK[1:0] to “cd” to select Loopback Mode “cd”.

Step 2: Wait 16 cycles for new register settings to take effect.

Loopback Mode “cd” is enabled after step 2 because MRW = 0, LBKE = 1, and LBK[1:0] = “cd”.

### Disabling Loopback Mode

Loopback Mode is disabled as follows:

Step 1: Initiate a Register Write operation with SA[10:1] = “000xx0.0010” to select Register #2 and set LBKE = 0 to disable Loopback Mode.

Step 2: Wait 16 cycles for new register settings to take effect.

Loopback Mode is disabled after step 2 because LBKE = 0.

### XOR LBK Mode

XOR LBK Mode is for *address/control input training*. It is defined as follows:

- Each input pin of the selected input group is sampled on  $\uparrow\text{CK}$  and  $\uparrow\overline{\text{CK}}$ .
- For each input sampled, the value sampled on  $\uparrow\text{CK}$  is XORed with the value sampled on  $\uparrow\overline{\text{CK}}$ .
- For each input sampled, the XOR result is subsequently driven out on its associated output pin (concurrently with  $\uparrow\text{CQ}$ ) for one full clock cycle, beginning “LBKL” cycles after the input is sampled.

Consequently, the output data pattern is always SDR regardless of the input data pattern, and regardless whether the SRAM samples the inputs correctly or not. The SDR output data pattern enables address/control inputs to be trained before data outputs.

XOR LBK Mode enables the controller to input various SDR and DDR data patterns on a particular input, and then determine whether the SRAM sampled them correctly or not by observing SDR data patterns on the associated output. Via multiple iterations of this process, the controller can adjust its output timing (in order to adjust the SRAM input timing) until optimum setup and hold margin at both SRAM input sample points is achieved, thereby individually “training” each address/control input pin.

### INV LBK Mode

INV LBK Mode is primarily for *read data output training*. It is defined as follows:

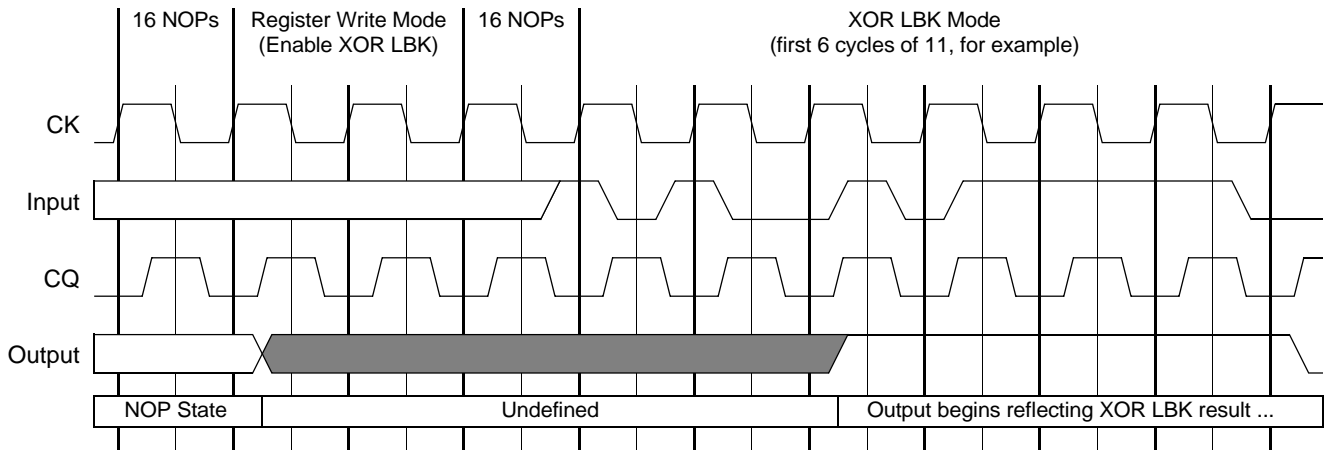
- Each input pin of the selected input group is sampled on  $\uparrow\text{CK}$  and  $\uparrow\overline{\text{CK}}$ .
- For each input sampled, the value sampled on  $\uparrow\text{CK}$  is subsequently driven out on its associated output pin (concurrently with  $\uparrow\text{CQ}$ ) for half a clock cycle, beginning “LBKL” cycles after the input is sampled.
- For each input sampled, the value sampled on  $\uparrow\overline{\text{CK}}$  is *inverted* and then subsequently driven out on its associated output pin (concurrently with  $\uparrow\overline{\text{CQ}}$ ) for half a clock cycle, beginning “LBKL + 0.5” cycles after the input is sampled.

Consequently, the output data pattern is DDR if the input data pattern is SDR (and vice versa), provided the SRAM samples the inputs correctly. Therefore, to ensure deterministic output behavior, address/control inputs should be trained before data outputs.

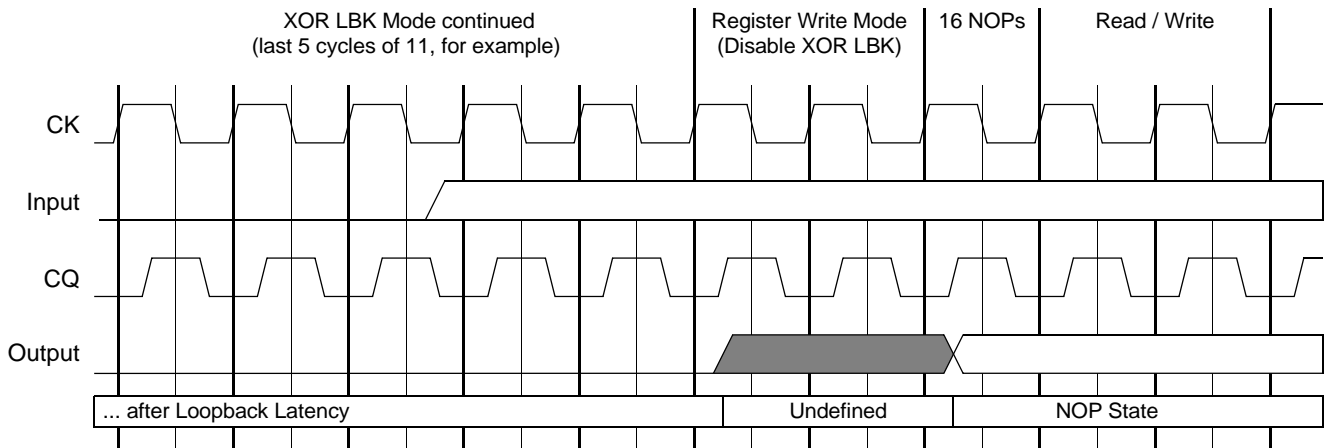
INV LBK Mode enables the controller to input various SDR (or DDR) data patterns on a particular input, to generate deterministic DDR (or SDR) data patterns on a particular output. The controller latches the output as it would during a normal Read operation, and verifies whether it received the expected values or not. Via multiple iterations of this process, the controller can adjust its input timing until optimum setup and hold margin at both controller input sample points is achieved, thereby individually “training” each read data output pin.

**Note:** INV LBK Mode can be used for address/control input training, if desired. However, such usage can be problematic because the output data pattern may be erroneous (i.e. it could be SDR or DDR regardless of the input pattern) if the SRAM samples the input incorrectly. In which case the controller may have difficulty detecting the erroneous behavior, and/or interpreting it.

### Entering XOR LBK Mode

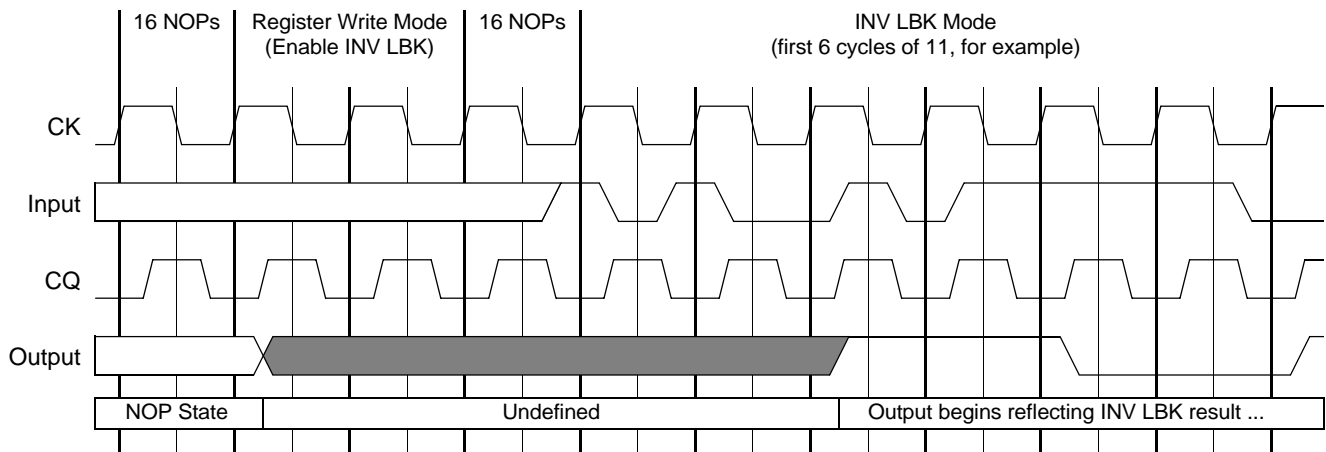


### Exiting XOR LBK Mode

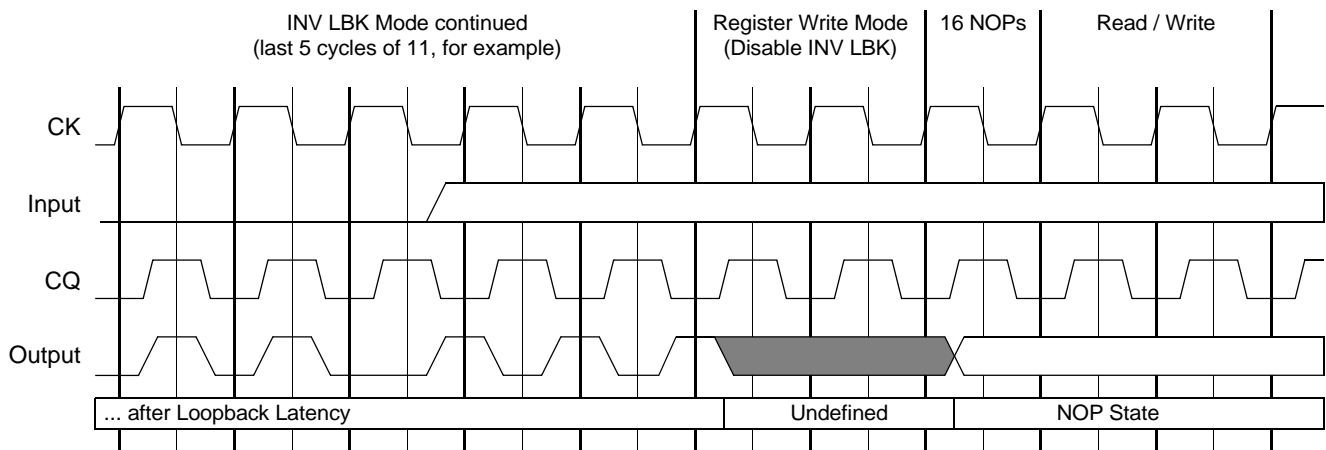


**Note:** “Input” represents any loop-backed input pin. “Output” represents the output pin on which “Input” is looped back.

### Entering INV LBK Mode



### Exiting INV LBK Mode



**Note:** “Input” represents any loop-backed input pin. “Output” represents the output pin on which “Input” is looped back.

### Loopback Mode Input Group Definition and Input-to-Output Pin Mapping

Inputs are divided into 2 groups because there are up to 28 inputs to train (22 address, 2 control, and 4 KD clocks), but as few as 18 outputs available to loop them back to (in x18 devices).

There are 20 inputs per group - one per Q, QINV output in x18 devices, and one per two Q, QINV outputs in x36 devices.

| Bit # | Input Pins |     | Input Signals |                         | Output Pins |          | Output Signals |          |                                |
|-------|------------|-----|---------------|-------------------------|-------------|----------|----------------|----------|--------------------------------|
|       | GP1        | GP2 | GP1           | GP2                     | x18         | x36      | x18            | x36      |                                |
| 1     | 8T         | --- | SA2           | RSVD                    | n/a         | 12Y      | n/a            | QINV1    | Right Side Output Data Byte(s) |
| 2     | 8P         | 8V  | SA4           | SA0                     | 13V         | 13V, 12W | Q8             | Q8, Q17  |                                |
| 3     | 8M         | 8T  | SA6           | SA2                     | 13T         | 13T, 12U | Q7             | Q7, Q16  |                                |
| 4     | 8J         | --- | SA8           | RSVD                    | 13P         | 13P, 12R | Q6             | Q6, Q15  |                                |
| 5     | 9H         | 9L  | SA16          | $\overline{\text{KD0}}$ | 13N         | 13N, 12P | Q5             | Q5, Q14  |                                |
| 6     | 8G         | 9K  | SA10          | KD0                     | 12J         | 12J, 12M | Q4             | Q4, Q13  |                                |
| 7     | 9F         | 7H  | SA18          | $\overline{\text{W}}$   | 12G         | 12G, 13H | Q3             | Q3, Q12  |                                |
| 8     | 8E         | --- | SA12          | RSVD                    | 12F         | 12F, 13G | Q2             | Q2, Q11  |                                |
| 9     | 9D         | --- | SA20          | RSVD                    | 12D         | 12D, 13E | Q1             | Q1, Q10  |                                |
| 10    | 8C         | --- | SA14          | RSVD                    | 12B         | 12B, 13C | Q0             | Q0, Q9   |                                |
| 20    | 6C         | --- | SA13          | RSVD                    | 12A         | 12A      | QINV0          | QINV0    |                                |
| 1     | 8T         | --- | SA2           | RSVD                    | 2Y          | 2Y       | QINV1          | QINV2    | Left Side Output Data Byte(s)  |
| 11    | 6T         | --- | SA1           | RSVD                    | 2W          | 2W, 1V   | Q9             | Q18, Q27 |                                |
| 12    | 6P         | 6V  | SA3           | SA21                    | 2U          | 2U, 1T   | Q10            | Q19, Q28 |                                |
| 13    | 6M         | --- | SA5           | RSVD                    | 2R          | 2R, 1P   | Q11            | Q20, Q29 |                                |
| 14    | 6J         | 7N  | SA7           | $\overline{\text{R}}$   | 2P          | 2P, 1N   | Q12            | Q21, Q30 |                                |
| 15    | 5H         | 5L  | SA15          | $\overline{\text{KD1}}$ | 2M          | 2M, 2J   | Q13            | Q22, Q31 |                                |
| 16    | 6G         | 5K  | SA9           | KD1                     | 1H          | 1H, 2G   | Q14            | Q23, Q32 |                                |
| 17    | 5F         | --- | SA17          | RSVD                    | 1G          | 1G, 2F   | Q15            | Q24, Q33 |                                |
| 18    | 6E         | --- | SA11          | RSVD                    | 1E          | 1E, 2D   | Q16            | Q25, Q34 |                                |
| 19    | 5D         | 6C  | SA19          | SA13                    | 1C          | 1C, 2B   | Q17            | Q26, Q35 |                                |
| 20    | 6C         | --- | SA13          | RSVD                    | n/a         | 2A       | n/a            | QINV3    |                                |

**Notes:**

1. Blue shading indicates input pins that are unused (NU) in certain device configurations. During Loopback Mode, the associated output pins loop back the states of those input pins regardless whether they are used or unused.
2. Gray shading indicates Group 2 inputs that are reserved (RSVD) for future use. During Loopback Mode, the associated output pins act as if they were looping back input pins tied Low.
3. Green shading indicates QINV output pins that are unused (NU) when Data Inversion is disabled. During Loopback Mode, they loop back the states of the associated input pins regardless whether Data Inversion is enabled or disabled.
4. The 18 unused Q and the 2 unused QINV in x18 devices remain in their “NU” states during Loopback Mode.
5. Bit #1 and bit #20 are repeated in the table to show that they are used in both the right and left side data bytes in x36 devices.

### Address Bus Utilization and Bank Access Restrictions

The address bus is a non-multiplexed DDR bus. Up to two memory addresses may be loaded per cycle - a read address at  $\uparrow\text{CK}$  and /or a write address at  $\uparrow\overline{\text{CK}}$ ; consequently two memory operations - a Read and a Write - may be initiated per clock cycle. The address bus is also sampled at  $\uparrow\text{CK}$  during a Register Write operation.

#### Address Bit Encoding

| Command        | Addr Load                      | Device | SA Address Bits |         |    |    |    |    |    |    |    |    |    |    |   |   |   |               |              |              |   |            |   |   |
|----------------|--------------------------------|--------|-----------------|---------|----|----|----|----|----|----|----|----|----|----|---|---|---|---------------|--------------|--------------|---|------------|---|---|
|                |                                |        | 21              | 20      | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6             | 5            | 4            | 3 | 2          | 1 | 0 |
| Read           | $\uparrow\text{CK}$            | x36    | NU              | Address |    |    |    |    |    |    |    |    |    |    |   |   |   |               |              | Bank Address |   |            |   |   |
|                |                                | x18    | Address         |         |    |    |    |    |    |    |    |    |    |    |   |   |   |               | Bank Address |              |   |            |   |   |
| Write          | $\uparrow\overline{\text{CK}}$ | x36    | NU              | Address |    |    |    |    |    |    |    |    |    |    |   |   |   |               |              | Bank Address |   |            |   |   |
|                |                                | x18    | Address         |         |    |    |    |    |    |    |    |    |    |    |   |   |   |               | Bank Address |              |   |            |   |   |
| Register Write | $\uparrow\text{CK}$            | x36    | NU              | X       | X  | X  | X  | X  | X  | X  | X  | X  | X  | X  | X | X | X | Register Data |              |              |   | Register # |   | X |
|                |                                | x18    | X               | X       | X  | X  | X  | X  | X  | X  | X  | X  | X  | X  | X | X | X | Register Data |              |              |   | Register # |   | X |

#### Bank Access Restrictions

1. Read in cycle “n” must be to a different bank than Read in cycle “n-1”.
2. Read in cycle “n” must be to a different bank than Write in cycle “n-5” (due to Write Buffering).

## Data Bus Inversion

Because the POD I/O standard employs high-side (pull-up) termination only, signals driven High consume less power than those driven Low. Consequently, these devices provide the ability to invert all data pins on a per byte basis, such that any transmitted data byte always contains more 1s than 0s, thereby reducing average I/O power as well as SSO noise. To accomplish this, one data inversion (DINV, QINV) bit is utilized per 9-bit data (D, Q) byte.

During Write operations, the controller inverts a particular 9-bit write data byte before transmitting it to the SRAM if it contains less than 5 High bits; otherwise, it transmits the data byte uninverted. If it inverts the data byte, the controller drives the corresponding write data inversion bit High; otherwise, it drives it Low. Upon receiving the write data byte, the SRAM uses the state of the corresponding write data inversion bit to determine whether or not to invert the data byte before storing it in the memory array.

During Read operations, the SRAM inverts a particular 9-bit read data byte before transmitting it to the controller if it contains less than 5 High bits; otherwise, it transmits the data byte uninverted. If it inverts the data byte, the SRAM drives the corresponding read data inversion bit High; otherwise, it drives it Low. Upon receiving the read data byte, the controller uses the state of the corresponding read data inversion bit to determine whether or not to invert the data byte before utilizing it.

With this implementation, each 10-bit data group (nine data bits plus one data inversion bit) is guaranteed to have no more than five pins driven low at any given time. Consequently, no more than five pins in each group can switch in the same direction during each bit time, reducing SSO noise effects.

**Note:** Data Inversion can be enabled and disabled via register bit DI.

## Read Latency

Read Latency (i.e. the number of cycles from read command input to first read data output) is programmable via register bit RLM as follows:

| RLM | Read Latency | Comment  |
|-----|--------------|--|
| 0   | 5 cycles     | First read data output 5 cycles after read command input |
| 1   | 6 cycles     | First read data output 6 cycles after read command input |

## Write Latency

Write Latency (i.e. the number of cycles from write command input to first write data input) is specified as follows:

| Write Latency | Comment  |
|---------------|--|
| 0 cycles      | First write data input concurrent with write command input |

## Read / Write Coherency

These devices are fully coherent. That is, Read operations always return the most recently written data to a particular address, even when a Read operation to a particular address occurs one cycle after a Write operation to the same address.

If a Read and Write operation are initiated to the same address in the same cycle, the Read operation returns the *previous* write data associated with a *previous* Write operation (which may have occurred as little as one cycle earlier), not the *current* write data associated with the *current* Write operation.

### State Truth Table

| RST | MRW | LBKE | $\bar{R}$ | $\bar{W}$             | SA | D | SRAM State                        | Q                     |
|-----|-----|------|-----------|-----------------------|----|---|-----------------------------------|-----------------------|
| 1   | X   | X    | X         | X                     | X  | X | Reset                             | NOP State             |
| 0   | 1   | X    | 0         | X                     | V  | X | Register Write Mode               | Undefined             |
| 0   | 0   | 1    | X         | X                     | X  | X | Loopback Mode                     | Loopback              |
| 0   | 1   | X    | 1         | See Clock Truth Table |    |   | Memory Mode<br>(Read, Write, NOP) | See Clock Truth Table |
| 0   | 0   | 0    | X         |                       |    |   |                                   |                       |

**Note:** 1 = High; 0 = Low; V = Valid; X = don't care.

### Clock Truth Table

| SA                               |  | MRW                              | $\bar{R}$                              | $\bar{W}$                        | Current Operation | D, DINV                          |  | Q, QINV                          |  |
|----------------------------------|--|----------------------------------|--|----------------------------------|-------------------|----------------------------------|--|----------------------------------|--|
| $\uparrow\text{CK}$<br>( $t_n$ ) | $\uparrow\bar{\text{CK}}$<br>( $t_{n+1/2}$ ) | $\uparrow\text{CK}$<br>( $t_n$ ) | $\uparrow\bar{\text{CK}}$<br>( $t_n$ ) | $\uparrow\text{CK}$<br>( $t_n$ ) | ( $t_n$ )         | $\uparrow\text{KD}$<br>( $t_n$ ) | $\uparrow\bar{\text{KD}}$<br>( $t_{n+1/2}$ ) | $\uparrow\text{CQ}$<br>( $t_m$ ) | $\uparrow\bar{\text{CQ}}$<br>( $t_{m+1/2}$ ) |
| X                                | X  | 0                                | 1                                      | 1                                | NOP               | X                                | X  | 1 / Hi-Z                         |  |
| X                                | V  | 0                                | 1                                      | 0                                | Write Only        | D1                               | D2   | 1 / Hi-Z                         |  |
| V                                | X  | 0                                | 0                                      | 1                                | Read Only         | X                                | X  | Q1                               | Q2   |
| V                                | V  | 0                                | 0                                      | 0                                | Read + Write      | D1                               | D2   | Q1                               | Q2   |
| V                                | V  | 1                                | 0                                      | X                                | Register Write    | X                                | X  | Undefined                        |  |
| V                                | V  | 1                                | 1                                      | X                                | NOP               | X                                | X  | 1 / Hi-Z                         |  |

**Notes:**

- 1 = High; 0 = Low; V = Valid; X = don't care.
- $t_m = t_{n+RL}$ , where RL indicates the Read Latency of the device.
- D1 and D2 indicate the first and second pieces of write data transferred during Write operations.
- Q1 and Q2 indicate the first and second pieces of read data transferred during Read operations.
- When D ODT is enabled, Q pins are driven High for one cycle in response to NOP and Write Only commands, RL cycles after the command is sampled.
- When D ODT is disabled, Q pins are tri-stated for one cycle in response to NOP and Write Only commands, RL cycles after the command is sampled.

## Input Timing

These devices utilize three pairs of positive and negative input clocks, CK &  $\overline{\text{CK}}$  and KD[1:0] &  $\overline{\text{KD}}$ [1:0], to latch the various synchronous inputs. Specifically:

During Memory Mode,  $\uparrow\text{CK}$  and  $\uparrow\overline{\text{CK}}$  latch address (SA) inputs, and  $\uparrow\text{CK}$  latches control ( $\overline{\text{R}}$ ,  $\overline{\text{W}}$ , MRW) inputs.

During Register Write Mode,  $\uparrow\text{CK}$  latches address and control inputs.

During Loopback Mode,  $\uparrow\text{CK}$  and  $\uparrow\overline{\text{CK}}$  latch address, control, and write data clock (KD,  $\overline{\text{KD}}$ ) inputs.

During Memory Mode,  $\uparrow\text{KD}$ [1:0] and  $\uparrow\overline{\text{KD}}$ [1:0] latch particular write data (D, DINV) inputs, as follows:

- $\uparrow\text{KD0}$  and  $\uparrow\overline{\text{KD0}}$  latch D[17:0], DINV[1:0] in x36 devices, and D[8:0], DINV0 in x18 devices.
- $\uparrow\text{KD1}$  and  $\uparrow\overline{\text{KD1}}$  latch D[35:18], DINV[3:2] in x36 devices, and D[17:9], DINV1 in x18 devices.

## Output Timing

These devices provide two pairs of positive and negative output clocks (aka “echo clocks”), CQ[1:0] &  $\overline{\text{CQ}}$ [1:0], whose timing is tightly aligned with read data in order to enable reliable source-synchronous data transmission.

These devices utilize a PLL to control output timing. When the PLL is enabled, it generates 0° and 180° phase clocks from  $\uparrow\text{CK}$  that control read data output clock (CQ,  $\overline{\text{CQ}}$ ), read data (Q, QINV), and read data valid (QVLD) output timing, as follows:

- $\uparrow\text{CK}+0^\circ$  generates  $\uparrow\text{CQ}$ [1:0],  $\downarrow\overline{\text{CQ}}$ [1:0], Q1 active, and Q2 inactive.
- $\uparrow\text{CK}+180^\circ$  generates  $\uparrow\overline{\text{CQ}}$ [1:0],  $\downarrow\text{CQ}$ [1:0], Q1 inactive, Q2 active, and QVLD active/inactive.

**Note:** Q1 and Q2 indicate the first and second pieces of read data transferred in any given clock cycle during Read operations.

When the PLL is enabled,  $\uparrow\text{CQ}$  is aligned to an internally-delayed version of  $\uparrow\text{CK}$ . See the AC Timing Specifications for more information.

$\uparrow\text{CQ}$ [1:0] and  $\uparrow\overline{\text{CQ}}$ [1:0] align with particular Q, QINV, and QVLD outputs, as follows:

- $\uparrow\text{CQ0}$  and  $\uparrow\overline{\text{CQ0}}$  align with Q[17:0], QINV[1:0], QVLD0 in x36 devices, and Q[8:0], QINV0, QVLD0 in x18 devices.
- $\uparrow\text{CQ1}$  and  $\uparrow\overline{\text{CQ1}}$  align with Q[35:18], QINV[3:2], QVLD1 in x36 devices, and Q[17:9], QINV1, QVLD1 in x18 devices.

## Driver Impedance Control

**Programmable Driver Impedance** is implemented on the following output signals:

- CQ,  $\overline{\text{CQ}}$ , Q, QINV, QVLD.

Driver impedance is programmed by connecting an external resistor RQ between the ZQ pin and V<sub>SS</sub>.

Driver impedance is set to the programmed value within 320K cycles after input clocks are operating within specification and RST is de-asserted Low. It is updated periodically thereafter to compensate for temperature and voltage fluctuations in the system.

| Output Signal                              | Pull-Down Impedance (R <sub>OUTL</sub> ) | Pull-Up Impedance (R <sub>OUTH</sub> ) |
|--|--|--|
| CQ, $\overline{\text{CQ}}$ , Q, QINV, QVLD | RQ*0.2 ± 10%                             | RQ*0.3 ± 10%                           |

**Notes:**

1. R<sub>OUTL</sub> and R<sub>OUTH</sub> apply when 175Ω ≤ RQ ≤ 225Ω.
2. The mismatch between R<sub>OUTL</sub> and R<sub>OUTH</sub> is less than 10%, guaranteed by design.

## ODT Impedance Control

**Programmable ODT Impedance** is implemented on the following input signals:

- CK,  $\overline{\text{CK}}$ , KD,  $\overline{\text{KD}}$ , SA,  $\overline{\text{R}}$ ,  $\overline{\text{W}}$ , MRW, D, DINV.

ODT impedance is programmed by connecting an external resistor RQ between the ZQ pin and V<sub>SS</sub>.

ODT impedance is set to the programmed value within 320K cycles after input clocks are operating within specification and RST is de-asserted Low. It is updated periodically thereafter to compensate for temperature and voltage fluctuations in the system.

| Input Signal  | Register Bit | Pull-Up Impedance (R <sub>INH</sub> ) |
|---|--------------|---------------------------------------|
| CK, $\overline{\text{CK}}$                          | CKZT = 0     | off                                   |
|   | CKZT = 1     | RQ*0.3 ± 10%                          |
| KD, $\overline{\text{KD}}$                          | KDZT = 0     | off                                   |
|   | KDZT = 1     | RQ*0.3 ± 10%                          |
| SA  | AZT = 0      | off                                   |
|   | AZT = 1      | RQ*0.3 ± 10%                          |
| $\overline{\text{R}}$ , $\overline{\text{W}}$ , MRW | CZT = 0      | off                                   |
|   | CZT = 1      | RQ*0.3 ± 10%                          |
| D, DINV   | DZT = 0      | off                                   |
|   | DZT = 1      | RQ*0.3 ± 10%                          |

**Notes:**

1. R<sub>INH</sub> applies when 175Ω ≤ RQ ≤ 225Ω.
2. All ODT is disabled during JTAG EXTEST and SAMPLE-Z instructions.

### Absolute Maximum Ratings

| Parameter            | Symbol    | Rating                  | Units | Notes |
|----------------------|-----------|-------------------------|-------|-------|
| Core Supply Voltage  | $V_{DD}$  | -0.3 to +1.4            | V     |       |
| I/O Supply Voltage   | $V_{DDQ}$ | -0.3 to $V_{DD}$        | V     |       |
| Input Voltage (HS)   | $V_{IN1}$ | -0.3 to $V_{DDQ} + 0.3$ | V     | 2     |
|                      | $V_{IN2}$ | $V_{DDQ} - 1.5$ to +1.7 |       |       |
| Input Voltage (LS)   | $V_{IN3}$ | -0.3 to $V_{DDQ} + 0.3$ | V     | 3     |
| Junction Temperature | $T_J$     | 0 to 125                | °C    |       |
| Storage Temperature  | $T_{STG}$ | -55 to 125              | °C    |       |

**Notes:**

- Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Recommended Operating Conditions for an extended period of time may affect reliability of this component.
- Parameters apply to High Speed Inputs: CK,  $\overline{CK}$ , KD,  $\overline{KD}$ , SA, D, DINV,  $\overline{R}$ ,  $\overline{W}$ , MRW.  $V_{IN1}$  and  $V_{IN2}$  must both be met.
- Parameters apply to Low Speed Inputs: RST, PLL, MZT, PZT.

### Recommended Operating Conditions

| Parameter                       | Symbol    | Min  | Typ  | Max      | Units | Notes |
|---------------------------------|-----------|------|------|----------|-------|-------|
| Core Supply Voltage             | $V_{DD}$  | 1.2  | 1.25 | 1.3      | V     | 2     |
|                                 |           | 1.15 | 1.2  | 1.3      | V     | 3     |
| I/O Supply Voltage              | $V_{DDQ}$ | 1.15 | 1.2  | $V_{DD}$ | V     |       |
| Commercial Junction Temperature | $T_{JC}$  | 0    | —    | 85       | °C    |       |
| Industrial Junction Temperature | $T_{JI}$  | -40  | —    | 100      | °C    |       |

**Notes:**

- For reliability purposes, power supplies must power up simultaneously, or in the following sequence:  
 $V_{SS}$ ,  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{REF}$ , and Inputs.  
 Power supplies must power down simultaneously, or in the reverse sequence.
- Parameters apply to -1333 speed grade devices only.
- Parameters apply to all but -1333 speed grade devices.

### Thermal Impedances

| Package | $\theta_{JA}$ (C°/W)<br>Airflow = 0 m/s | $\theta_{JA}$ (C°/W)<br>Airflow = 1 m/s | $\theta_{JA}$ (C°/W)<br>Airflow = 2 m/s | $\theta_{JB}$ (C°/W) | $\theta_{JC}$ (C°/W) |
|---------|---|---|---|----------------------|----------------------|
| FBGA    | TBD                                     | TBD                                     | TBD                                     | TBD                  | TBD                  |

### I/O Capacitance

| Parameter          | Symbol    | Min | Max | Units | Notes |
|--------------------|-----------|-----|-----|-------|-------|
| Input Capacitance  | $C_{IN}$  | —   | 5.0 | pF    | 1, 3  |
| Output Capacitance | $C_{OUT}$ | —   | 5.5 | pF    | 2, 3  |

**Notes:**

- $V_{IN} = V_{DDQ}/2$ .
- $V_{OUT} = V_{DDQ}/2$ .
- $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ .

### Input Electrical Characteristics

| Parameter                  | Symbol      | Min              | Typ              | Max              | Units | Notes  |
|----------------------------|-------------|------------------|------------------|------------------|-------|--------|
| DC Input Reference Voltage | $V_{REFdc}$ | $0.69 * V_{DDQ}$ | $0.70 * V_{DDQ}$ | $0.71 * V_{DDQ}$ | V     | —      |
| DC Input High Voltage (HS) | $V_{IH1dc}$ | $V_{REF} + 0.08$ | $V_{DDQ}$        | $V_{DDQ} + 0.15$ | V     | 5      |
| DC Input Low Voltage (HS)  | $V_{IL1dc}$ | -0.15            | $0.40 * V_{DDQ}$ | $V_{REF} - 0.08$ | V     | 1, 5   |
| DC Input High Voltage (LS) | $V_{IH2dc}$ | $0.75 * V_{DDQ}$ | $V_{DDQ}$        | $V_{DDQ} + 0.15$ | V     | 6      |
| DC Input Low Voltage (LS)  | $V_{IL2dc}$ | -0.15            | 0                | $0.25 * V_{DDQ}$ | V     | 6      |
| AC Input Reference Voltage | $V_{REFac}$ | $0.68 * V_{DDQ}$ | $0.70 * V_{DDQ}$ | $0.72 * V_{DDQ}$ | V     | 2      |
| AC Input High Voltage (HS) | $V_{IH1ac}$ | $V_{REF} + 0.15$ | $V_{DDQ}$        | $V_{DDQ} + 0.25$ | V     | 3-5    |
| AC Input Low Voltage (HS)  | $V_{IL1ac}$ | -0.25            | $0.40 * V_{DDQ}$ | $V_{REF} - 0.15$ | V     | 1, 3-5 |
| AC Input High Voltage (LS) | $V_{IH2ac}$ | $V_{DDQ} - 0.2$  | $V_{DDQ}$        | $V_{DDQ} + 0.25$ | V     | 3, 6   |
| AC Input Low Voltage (LS)  | $V_{IL2ac}$ | -0.25            | 0                | 0.2              | V     | 3, 6   |

**Notes:**

- "Typ" parameter applies when Controller  $R_{OUTL} = 40\Omega$  and SRAM  $R_{INH} = 60\Omega$ .
- $V_{REFac}$  is equal to  $V_{REFdc}$  plus noise.
- $V_{IH}$  max and  $V_{IL}$  min apply for pulse widths less than one-quarter of the cycle time.
- Input rise and fall times must be a minimum of 1V/ns, and within 10% of each other.
- Parameters apply to High Speed Inputs: CK,  $\overline{CK}$ , KD,  $\overline{KD}$ , SA, D, DINV,  $\overline{R}$ , W, MRW.
- Parameters apply to Low Speed Inputs: RST, PLL, MZT, PZT.

### Output Electrical Characteristics

| Parameter              | Symbol     | Min   | Typ              | Max              | Units | Notes |
|------------------------|------------|-------|------------------|------------------|-------|-------|
| DC Output High Voltage | $V_{OHdc}$ | —     | $V_{DDQ}$        | $V_{DDQ} + 0.15$ | V     | 2     |
| DC Output Low Voltage  | $V_{OLdc}$ | -0.15 | $0.40 * V_{DDQ}$ | —                | V     | 1, 2  |
| AC Output High Voltage | $V_{OHac}$ | —     | $V_{DDQ}$        | $V_{DDQ} + 0.25$ | V     | 2     |
| AC Output Low Voltage  | $V_{OLac}$ | -0.25 | $0.40 * V_{DDQ}$ | —                | V     | 1, 2  |

**Note:**

1. "Typ" parameter applies when SRAM  $R_{OUTL} = 40\Omega$  and Controller  $R_{INH} = 60\Omega$ .
2. Parameters apply to: CQ,  $\overline{CQ}$ , Q, QINV, QVLD.

### Leakage Currents

| Parameter              | Symbol    | Min | Max | Units | Notes |
|------------------------|-----------|-----|-----|-------|-------|
| Input Leakage Current  | $I_{LI1}$ | -2  | 2   | uA    | 1, 2  |
|                        | $I_{LI2}$ | -20 | 2   | uA    | 1, 3  |
|                        | $I_{LI3}$ | -2  | 20  | uA    | 1, 4  |
| Output Leakage Current | $I_{LO}$  | -2  | 2   | uA    | 5, 6  |

**Notes:**

1.  $V_{IN} = V_{SS}$  to  $V_{DDQ}$ .
2. Parameters apply to CK,  $\overline{CK}$ , KD,  $\overline{KD}$ , SA, D, DINV,  $\overline{R}$ ,  $\overline{W}$ , MRW when ODT is disabled.  
Parameters apply to MZT, PZT.
3. Parameters apply to PLL, TMS, TDI (weakly pulled up).
4. Parameters apply to RST, TCK (weakly pulled down).
5.  $V_{OUT} = V_{SS}$  to  $V_{DDQ}$ .
6. Parameters apply to CQ,  $\overline{CQ}$ , Q, QINV, QVLD, TDO.

### Operating Currents

| Parameter             | Symbol          | Operating Frequency | @ 1.15V<br>V <sub>DD</sub> | @ 1.2V<br>V <sub>DD</sub> | @ 1.25V<br>V <sub>DD</sub> | @ 1.3V<br>V <sub>DD</sub> | Units |
|-----------------------|-----------------|---------------------|----------------------------|---------------------------|----------------------------|---------------------------|-------|
| x18 Operating Current | I <sub>DD</sub> | 1333 MHz            | n/a                        | TBD                       | TBD                        | TBD                       | mA    |
|                       |                 | 1250 MHz            | TBD                        | TBD                       | TBD                        | TBD                       | mA    |
|                       |                 | 1100 MHz            | TBD                        | TBD                       | TBD                        | TBD                       | mA    |
|                       |                 | 1000 MHz            | TBD                        | TBD                       | TBD                        | TBD                       | mA    |
|                       |                 | 900 MHz             | TBD                        | TBD                       | TBD                        | TBD                       | mA    |
|                       |                 | 833 MHz             | TBD                        | TBD                       | TBD                        | TBD                       | mA    |
| x36 Operating Current | I <sub>DD</sub> | 1333 MHz            | n/a                        | TBD                       | TBD                        | TBD                       | mA    |
|                       |                 | 1250 MHz            | TBD                        | TBD                       | TBD                        | TBD                       | mA    |
|                       |                 | 1100 MHz            | TBD                        | TBD                       | TBD                        | TBD                       | mA    |
|                       |                 | 1000 MHz            | TBD                        | TBD                       | TBD                        | TBD                       | mA    |
|                       |                 | 900 MHz             | TBD                        | TBD                       | TBD                        | TBD                       | mA    |
|                       |                 | 833 MHz             | TBD                        | TBD                       | TBD                        | TBD                       | mA    |

**Notes:**

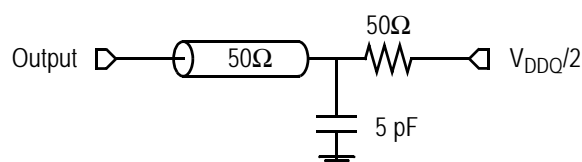
1. I<sub>OUT</sub> = 0 mA; V<sub>IN</sub> = V<sub>IH</sub> or V<sub>IL</sub>.
2. Applies at 100% Reads + Writes.

### AC Test Conditions

| Parameter                                       | Symbol           | Conditions   | Units |
|---|------------------|--------------|-------|
| Core Supply Voltage (-1333 speed grade)         | V <sub>DD</sub>  | 1.2 to 1.3   | V     |
| Core Supply Voltage (all but -1333 speed grade) | V <sub>DD</sub>  | 1.15 to 1.3  | V     |
| I/O Supply Voltage                              | V <sub>DDQ</sub> | 1.15 to 1.25 | V     |
| Input Reference Voltage                         | V <sub>REF</sub> | 0.84         | V     |
| Input High Level                                | V <sub>IH</sub>  | 1.14         | V     |
| Input Low Level                                 | V <sub>IL</sub>  | 0.54         | V     |
| Input Rise and Fall Time                        | —                | 2.0          | V/ns  |
| Input and Output Reference Level                | —                | 0.84         | V     |

**Note:** Output Load Conditions R<sub>O</sub> = 200Ω. Refer to figure below.

#### AC Test Output Load



### AC Timing Specifications (independent of device speed grade)

| Parameter  | Symbol                  | Min                                   | Max                                   | Units  | Notes |
|--|-------------------------|---------------------------------------|---------------------------------------|--------|-------|
| <b>Input Clock Timing</b>                            |                         |                                       |                                       |        |       |
| Clk High Pulse Width                                 | $t_{KHKL}$              | 0.45                                  | —                                     | cycles | 1     |
| Clk Low Pulse Width                                  | $t_{KLKH}$              | 0.45                                  | —                                     | cycles | 1     |
| Clk High to $\overline{\text{Clk}}$ High             | $t_{KH\overline{KH}}$   | 0.45                                  | 0.55                                  | cycles | 2     |
| Clk High to Write Data Clk High                      | $t_{KHKD}$              | -0.25                                 | +0.25                                 | cycles | 3     |
| Clk Cycle-to-Cycle Jitter                            | $t_{KJITcc}$            | —                                     | 60                                    | ps     | 1,4,5 |
| PLL Lock Time  | $t_{Klock}$             | 65,536                                | —                                     | cycles | 6     |
| Clk Static to PLL Reset                              | $t_{Kreset}$            | 30                                    | —                                     | ns     | 7,11  |
| <b>Output Timing</b>                                 |                         |                                       |                                       |        |       |
| Echo Clk High to Output Valid / Hold                 | $t_{CQHQV/X}$           | -100                                  | 100                                   | ps     | 8     |
| Echo Clk High to $\overline{\text{Echo Clock}}$ High | $t_{CQH\overline{COH}}$ | $0.5 \cdot t_{KHKH}(\text{nom}) - 30$ | $0.5 \cdot t_{KHKH}(\text{nom}) + 30$ | ps     | 9,11  |
| $\overline{\text{Echo Clk}}$ High to Echo Clock High | $t_{\overline{COH}COH}$ | $0.5 \cdot t_{KHKH}(\text{nom}) - 30$ | $0.5 \cdot t_{KHKH}(\text{nom}) + 30$ | ps     | 10,11 |

#### Notes:

All parameters are measured from the mid-point of the object signal to the mid-point of the reference signal unless otherwise noted.

- Parameters apply to CK,  $\overline{\text{CK}}$ , KD,  $\overline{\text{KD}}$ .
- Parameter specifies  $\uparrow\text{CK} \rightarrow \uparrow\overline{\text{CK}}$  and  $\uparrow\text{KD} \rightarrow \uparrow\overline{\text{KD}}$  requirements.
- Parameter specifies  $\uparrow\text{CK} \rightarrow \uparrow\text{KD}$  and  $\uparrow\overline{\text{CK}} \rightarrow \uparrow\overline{\text{KD}}$  requirements.
- Parameter specifies *Cycle-to-Cycle (C2C) Jitter* (i.e. the maximum variation from clock rising edge to the next clock rising edge).  
As such, it limits *Period Jitter* (i.e. the maximum variation in clock cycle time from nominal) to  $\pm 30\text{ps}$ .  
And as such, it limits *Absolute Jitter* (i.e. the maximum variation in clock rising edge from its nominal position) to  $\pm 15\text{ps}$ .
- The device can tolerate C2C Jitter greater than 60ps, up to a maximum of 200ps. However, when using a device from a particular speed grade,  $t_{KHKH}(\text{min})$  of that speed grade must be derated (increased) by half the difference between the actual C2C Jitter and 60ps. For example, if the actual C2C Jitter is 100ps, then  $t_{KHKH}(\text{min})$  for the -1333 speed grade is derated to 0.77ns ( $0.75\text{ns} + 0.5 \cdot (100\text{ps} - 60\text{ps})$ ).
- $V_{DD}$  slew rate must be  $< 0.1\text{V DC per } 50\text{ns}$  for PLL lock retention. PLL lock time begins once  $V_{DD}$  and input clock are stable.
- Parameter applies to CK.
- Parameters apply to Q, QVLD and are referenced to  $\uparrow\text{CQ}$  &  $\uparrow\overline{\text{CQ}}$ .
- Parameter specifies  $\uparrow\text{CQ} \rightarrow \uparrow\overline{\text{CQ}}$  timing.  $t_{KHKH}(\text{nom})$  is the nominal input clock cycle time applied to the device.
- Parameter specifies  $\uparrow\overline{\text{CQ}} \rightarrow \uparrow\text{CQ}$  timing.  $t_{KHKH}(\text{nom})$  is the nominal input clock cycle time applied to the device.
- Parameters are not tested. They are guaranteed by design, and verified through extensive corner-lot characterization.

**AC Timing Specifications (variable with device speed grade)**

| Parameter                            | Symbol       | -1333 |      | -1250 |      | -1100 |      | -1000 |      | Units | Notes |
|--------------------------------------|--------------|-------|------|-------|------|-------|------|-------|------|-------|-------|
|                                      |              | Min   | Max  | Min   | Max  | Min   | Max  | Min   | Max  |       |       |
| <b>Input Clock Timing</b>            |              |       |      |       |      |       |      |       |      |       |       |
| Clk Cycle Time                       | $t_{KHKH}$   | 0.75  | 6.0  | 0.8   | 6.0  | 0.9   | 6.0  | 1.0   | 6.0  | ns    | 1,2   |
|                                      |              | 0.9   | 6.0  | 1.0   | 6.0  | 1.1   | 6.0  | 1.2   | 6.0  | ns    | 1,3   |
| <b>Input Setup &amp; Hold Timing</b> |              |       |      |       |      |       |      |       |      |       |       |
| Input Valid to Clk High              | $t_{IVKH}$   | 150   | —    | 150   | —    | 150   | —    | 150   | —    | ps    | 4     |
| Clk High to Input Hold               | $t_{KHIX}$   | 150   | —    | 150   | —    | 150   | —    | 150   | —    | ps    |       |
| Input Pulse Width                    | $t_{IPW1}$   | 300   | —    | 300   | —    | 300   | —    | 300   | —    | ps    | 5     |
|                                      | $t_{IPW2}$   | 150   | —    | 150   | —    | 150   | —    | 150   | —    | ps    | 6     |
| MRW Valid to Clk High                | $t_{RVKH}$   | 150   | —    | 150   | —    | 150   | —    | 150   | —    | ps    | 7     |
| Clk High to MRW Hold                 | $t_{KHRX}$   | 150   | —    | 150   | —    | 150   | —    | 150   | —    | ps    |       |
| <b>Output Timing</b>                 |              |       |      |       |      |       |      |       |      |       |       |
| Clk High to Output Valid / Hold      | $t_{KHQVIX}$ | 0.4   | 1.4  | 0.2   | 1.2  | 0.2   | 1.2  | 0.2   | 1.2  | ns    | 8     |
|                                      |              | 0.85  | 1.95 | 0.65  | 1.75 | 0.65  | 1.75 | 0.65  | 1.75 | ns    | 9     |
| Clk High to Echo Clock High          | $t_{KHCOH}$  | 0.4   | 1.4  | 0.2   | 1.2  | 0.2   | 1.2  | 0.2   | 1.2  | ns    | 10    |
|                                      |              | 0.85  | 1.95 | 0.65  | 1.75 | 0.65  | 1.75 | 0.65  | 1.75 | ns    | 11    |

**Notes:**

All parameters are measured from the mid-point of the object signal to the mid-point of the reference signal.

1. Parameters apply to CK,  $\overline{CK}$ , KD,  $\overline{KD}$ .
2. Parameter applies when RL=6.
3. Parameter applies when RL=5.
4. Parameters apply to  $\overline{SA}$ , and are referenced to  $\uparrow CK$  &  $\uparrow \overline{CK}$ .  
Parameters apply to  $\overline{R}$ ,  $\overline{W}$ , and are referenced to  $\uparrow CK$  (and to  $\uparrow \overline{CK}$  during Loopback Mode).  
Parameters apply to D,  $\overline{DINV}$ , and are referenced to  $\uparrow KD$  &  $\uparrow \overline{KD}$ .  
Parameters apply to KD,  $\overline{KD}$ , and are referenced to  $\uparrow CK$  &  $\uparrow \overline{CK}$  during Loopback Mode.
5. " $t_{IPW1}$ " Input Pulse Width Requirements - For use with no Input Training  
 $t_{IPW1}$  applies to the set of inputs described in note 4.  
 $t_{IPW1}$  applies to ALL inputs across ALL PVT conditions. That is, it is the Monte Carlo spread across all inputs on all dies.  
 $t_{IPW1}$  includes everything associated with  $t_{IPW2}$  (see below), plus:  
Input vs. Input and Input vs. Clock die layout mismatch.  
Input vs. Input and Input vs. Clock package trace mismatch.  
Input vs. Input and Input vs. Clock timing mismatch due to P variation across multiple dies.  
Input vs. Input and Input vs. Clock timing mismatch due to P variation on a single die.

6. "t<sub>IPW2</sub>" Input Pulse Width Requirements - For use with Per-Bit Input Training

t<sub>IPW2</sub> applies to the set of inputs described in note 4.

t<sub>IPW2</sub> applies to each input individually, across ALL VT conditions.

t<sub>IPW2</sub> includes the following:

The fundamental setup and hold requirements of the SRAM input register.

Input vs. Clock timing variation that occurs due to:

Rising/falling edge timing mismatches.

Internal clock jitter.

Internal V<sub>DD</sub>, V<sub>DDQ</sub>, and V<sub>SS</sub> noise.

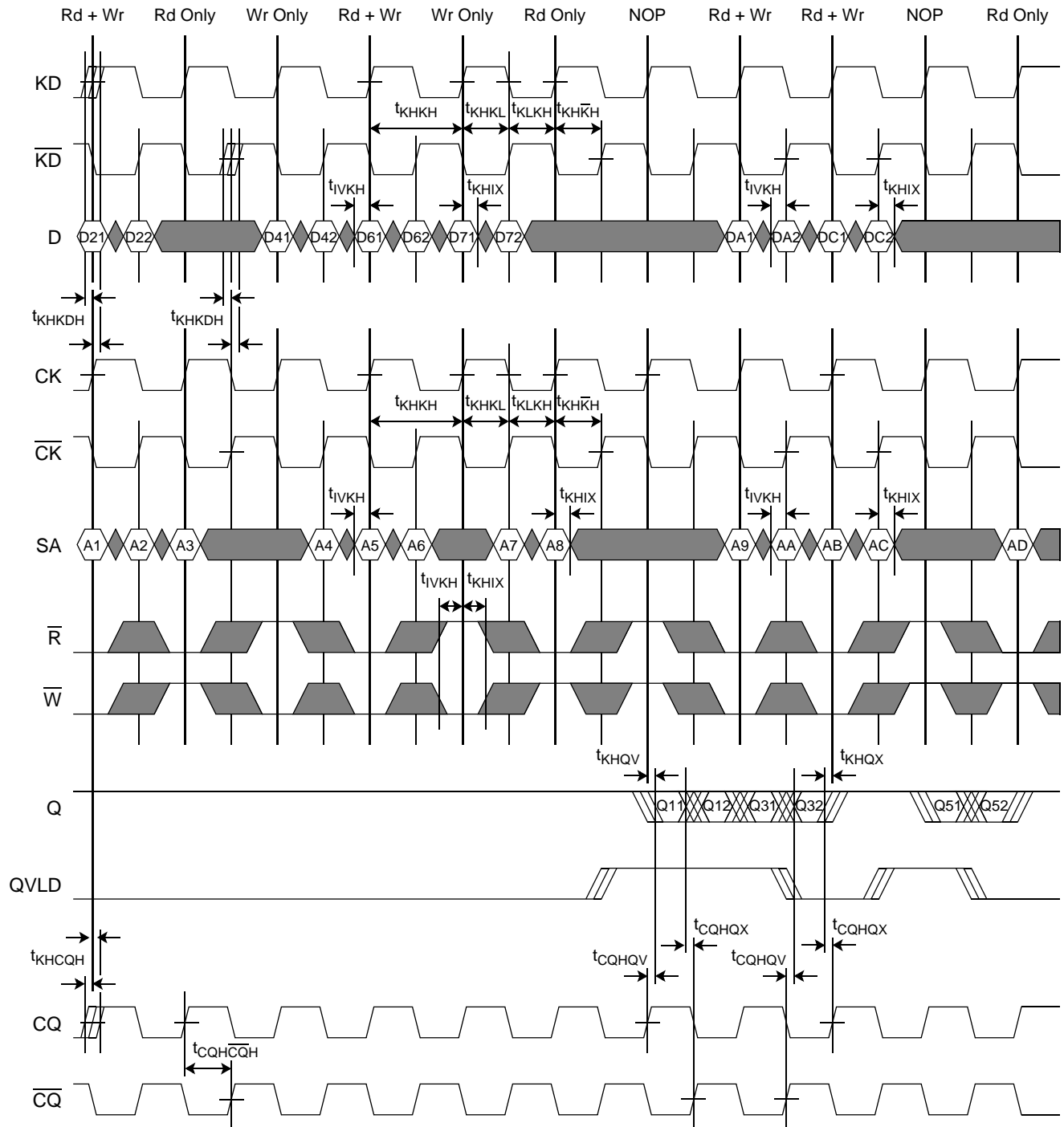
Package inductance.

Crosstalk.

**Per-bit input training** must be performed in order to take advantage of this parameter specification. Such training can compensate for all of the SRAM-related timing mismatches that are associated exclusively with t<sub>IPW1</sub>.

7. Parameters apply to MRW, and are referenced to ↑CK. Applicable when Register Write Mode is utilized synchronously.
8. Parameters apply to Q, and are referenced to ↑CK. Applicable when Data Inversion is disabled.
9. Parameters apply to Q, QINV, and are referenced to ↑CK. Applicable when Data Inversion is enabled.
10. Parameter specifies ↑CK → ↑CQ timing. Applicable when Data Inversion is disabled.
11. Parameter specifies ↑CK → ↑CQ timing. Applicable when Data Inversion is enabled.

### Memory Read and Write Timing Diagram (RL=6)



**Note:** MRW=0 (not shown).

## JTAG Test Mode Description

These devices provide a JTAG Test Access Port (TAP) and Boundary Scan interface using a limited set of IEEE std. 1149.1 functions. This test mode is intended to provide a mechanism for testing the interconnect between master (processor, controller, etc.), ECCRAM, other components, and the printed circuit board. In conformance with a subset of IEEE std. 1149.1, these devices contain a TAP Controller and multiple TAP Registers. The TAP Registers consist of one Instruction Register and multiple Data Registers.

The TAP consists of the following four signals:

| Pin | Pin Name         | I/O | Description  |
|-----|------------------|-----|--|
| TCK | Test Clock       | I   | Induces (clocks) TAP Controller state transitions.                                 |
| TMS | Test Mode Select | I   | Inputs commands to the TAP Controller. Sampled on the rising edge of TCK.          |
| TDI | Test Data In     | I   | Inputs data serially to the TAP Registers. Sampled on the rising edge of TCK.      |
| TDO | Test Data Out    | O   | Outputs data serially from the TAP Registers. Driven from the falling edge of TCK. |

### Concurrent TAP and Normal ECCRAM Operation

According to IEEE std. 1149.1, most public TAP Instructions do not disrupt normal device operation. In these devices, the only exceptions are EXTEST and SAMPLE-Z. See the Tap Registers section for more information.

### Disabling the TAP

When JTAG is not used, TCK should be tied Low to prevent clocking the ECCRAM. TMS and TDI should either be tied High through a pull-up resistor or left unconnected. TDO should be left unconnected.

## JTAG DC Operating Conditions

| Parameter                | Symbol    | Min              | Max              | Units | Notes |
|--------------------------|-----------|------------------|------------------|-------|-------|
| JTAG Input High Voltage  | $V_{TIH}$ | $0.75 * V_{DDQ}$ | $V_{DDQ} + 0.15$ | V     | 1     |
| JTAG Input Low Voltage   | $V_{TIL}$ | -0.15            | $0.25 * V_{DDQ}$ | V     | 1     |
| JTAG Output High Voltage | $V_{TOH}$ | $V_{DDQ} - 0.2$  | —                | V     | 2, 3  |
| JTAG Output Low Voltage  | $V_{TOL}$ | —                | 0.2              | V     | 2, 4  |

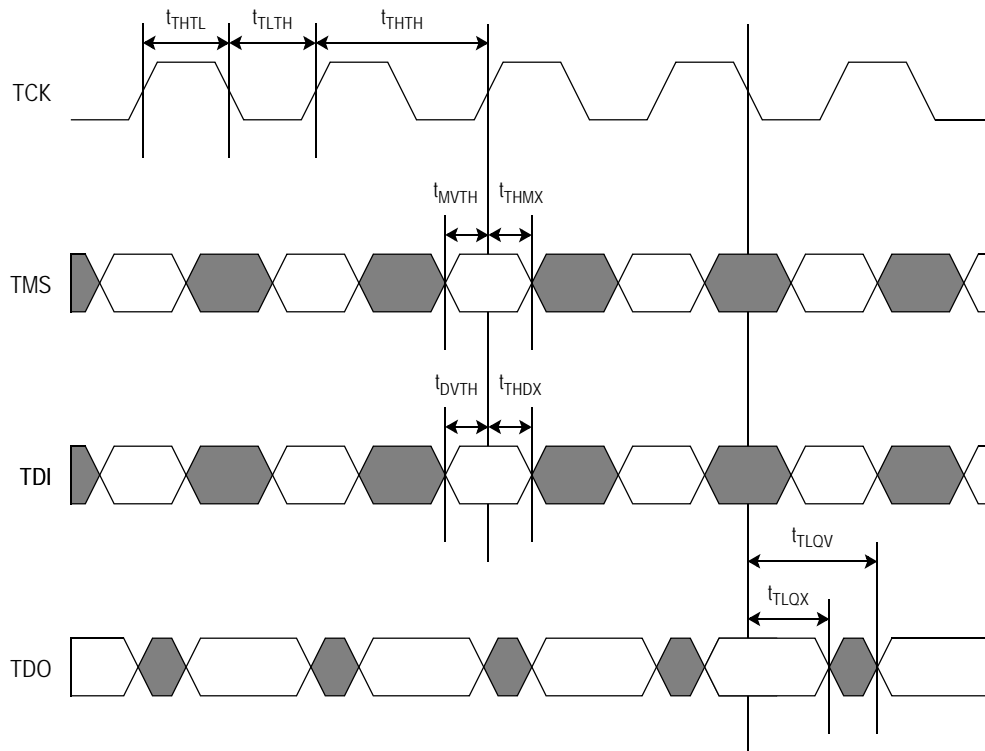
#### Notes:

- Parameters apply to TCK, TMS, and TDI.
- Parameters apply to TDO.
- $I_{TOH} = -2.0$  mA.
- $I_{TOL} = 2.0$  mA.

### JTAG AC Timing Specifications

| Parameter  | Symbol     | Min | Max | Units |
|--|------------|-----|-----|-------|
| TCK Cycle Time                                     | $t_{THTH}$ | 50  | —   | ns    |
| TCK High Pulse Width                               | $t_{THTL}$ | 20  | —   | ns    |
| TCK Low Pulse Width                                | $t_{TLTH}$ | 20  | —   | ns    |
| TMS Setup Time                                     | $t_{MVTH}$ | 10  | —   | ns    |
| TMS Hold Time                                      | $t_{THMX}$ | 10  | —   | ns    |
| TDI Setup Time                                     | $t_{DVTH}$ | 10  | —   | ns    |
| TDI Hold Time                                      | $t_{THDX}$ | 10  | —   | ns    |
| Capture Setup Time (Address, Control, Data, Clock) | $t_{CS}$   | 10  | —   | ns    |
| Capture Hold Time (Address, Control, Data, Clock)  | $t_{CH}$   | 10  | —   | ns    |
| TCK Low to TDO Valid                               | $t_{TLOV}$ | —   | 10  | ns    |
| TCK Low to TDO Hold                                | $t_{TLOX}$ | 0   | —   | ns    |

**JTAG Timing Diagram**



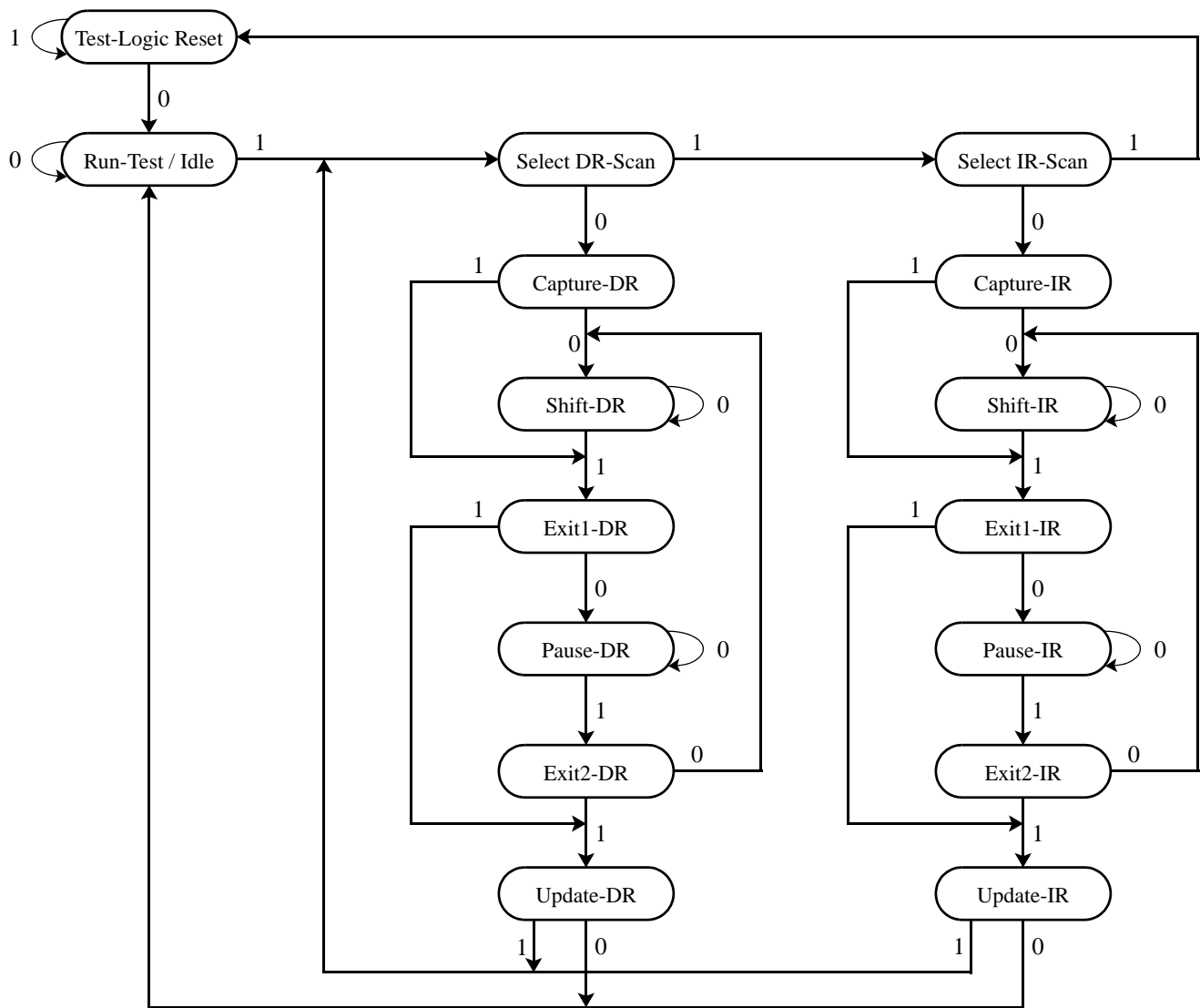
## TAP Controller

The TAP Controller is a 16-state state machine that controls access to the various TAP Registers and executes the operations associated with each TAP Instruction. State transitions are controlled by TMS and occur on the rising edge of TCK. The TAP Controller enters the Test-Logic Reset state in one of two ways:

1. At power up.
2. When a logic 1 is applied to TMS for at least 5 consecutive rising edges of TCK.

The TDI input receiver is sampled only when the TAP Controller is in either the Shift-IR state or the Shift-DR state. The TDO output driver is enabled only when the TAP Controller is in either the Shift-IR state or the Shift-DR state.

### TAP Controller State Diagram



## TAP Registers

TAP Registers are serial shift registers that capture serial input data (from TDI) on the rising edge of TCK, and drive serial output data (to TDO) on the subsequent falling edge of TCK. They are divided into two groups: Instruction Registers (IR), which are manipulated via the IR states in the TAP Controller, and Data Registers (DR), which are manipulated via the DR states in the TAP Controller.

### Instruction Register (IR - 3 bits)

The Instruction Register stores the various TAP Instructions supported by ECCRAM. It is loaded with the IDCODE instruction (logic 001) at power-up, and when the TAP Controller is in the Test-Logic Reset and Capture-IR states. It is inserted between TDI and TDO when the TAP Controller is in the Shift-IR state, at which time it can be loaded with a new instruction. However, newly loaded instructions are not executed until the TAP Controller has reached the Update-IR state.

The Instruction Register is 3 bits wide, and is encoded as follows:

| Code<br>(2:0) | Instruction | Description  |
|---------------|-------------|--|
| 000           | EXTEST      | Loads the logic states of all signals composing the ECCRAM I/O ring into the Boundary Scan Register when the TAP Controller is in the Capture-DR state, and inserts the Boundary Scan Register between TDI and TDO when the TAP Controller is in the Shift-DR state.<br>Also transfers the contents of the Boundary Scan Register associated with output signals (Q, QINV, QVLD, CQ, CQ) directly to their corresponding output pins. However, newly loaded Boundary Scan Register contents do not appear at the output pins until the TAP Controller has reached the Update-DR state.<br>Also disables all ODT.<br>See the Boundary Scan Register description for more information. |
| 001           | IDCODE      | Loads a predefined device- and manufacturer-specific identification code into the ID Register when the TAP Controller is in the Capture-DR state, and inserts the ID Register between TDI and TDO when the TAP Controller is in the Shift-DR state.<br>See the ID Register description for more information.   |
| 010           | SAMPLE-Z    | Loads the logic states of all signals composing the ECCRAM I/O ring into the Boundary Scan Register when the TAP Controller is in the Capture-DR state, and inserts the Boundary Scan Register between TDI and TDO when the TAP Controller is in the Shift-DR state.<br>Also disables all ODT.<br>Also forces Q, QINV output drivers to a High-Z state.<br>See the Boundary Scan Register description for more information.  |
| 011           | PRIVATE     | Reserved for manufacturer use only.  |
| 100           | SAMPLE      | Loads the logic states of all signals composing the ECCRAM I/O ring into the Boundary Scan Register when the TAP Controller is in the Capture-DR state, and inserts the Boundary Scan Register between TDI and TDO when the TAP Controller is in the Shift-DR state.<br>See the Boundary Scan Register description for more information.   |
| 101           | PRIVATE     | Reserved for manufacturer use only.  |
| 110           | PRIVATE     | Reserved for manufacturer use only.  |
| 111           | BYPASS      | Loads a logic 0 into the Bypass Register when the TAP Controller is in the Capture-DR state, and inserts the Bypass Register between TDI and TDO when the TAP Controller is in the Shift-DR state.<br>See the Bypass Register description for more information.  |

**Bypass Register (DR - 1 bit)**

The Bypass Register is one bit wide, and provides the minimum length serial path between TDI and TDO. It is loaded with a logic 0 when the BYPASS instruction has been loaded in the Instruction Register and the TAP Controller is in the Capture-DR state. It is inserted between TDI and TDO when the BYPASS instruction has been loaded into the Instruction Register and the TAP Controller is in the Shift-DR state.

**ID Register (DR - 32 bits)**

The ID Register is loaded with a predetermined device- and manufacturer-specific identification code when the IDCODE instruction has been loaded into the Instruction Register and the TAP Controller is in the Capture-DR state. It is inserted between TDI and TDO when the IDCODE instruction has been loaded into the Instruction Register and the TAP Controller is in the Shift-DR state.

The ID Register is 32 bits wide, and is encoded as follows:

| See BSDL Model<br>(31:12) | GSI ID<br>(11:1) | Start Bit<br>(0) |
|---------------------------|------------------|------------------|
| XXXX XXXX XXXX XXXX XXXX  | 0001 1011 001    | 1                |

Bit 0 is the LSB of the ID Register, and Bit 31 is the MSB. When the ID Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

**Boundary Scan Register (DR - 137 bits)**

The Boundary Scan Register is equal in length to the number of active signal connections to the ECCRAM (excluding the TAP pins) plus a number of place holder locations reserved for functional and/or density upgrades. It is loaded with the logic states of all signals composing the ECCRAM's I/O ring when the EXTEST, SAMPLE, or SAMPLE-Z instruction has been loaded into the Instruction Register and the TAP Controller is in the Capture-DR state. It is inserted between TDI and TDO when the EXTEST, SAMPLE, or SAMPLE-Z instruction has been loaded into the Instruction Register and the TAP Controller is in the Shift-DR state.

Additionally, the contents of the Boundary Scan Register associated with the ECCRAM outputs (Q, QVLD, CQ,  $\overline{CQ}$ ) are driven directly to the corresponding ECCRAM output pins when the EXTEST instruction is selected. However, after the EXTEST instruction has been selected, any new data loaded into Boundary Scan Register when the TAP Controller is in the Shift-DR state does not appear at the output pins until the TAP Controller has reached the Update-DR state.

The value captured in the boundary scan register for NU pins is determined by the external pin state. The value captured in the boundary scan register for NC pins is 0 regardless of the external pin state. The value captured in the Internal Cell (Bit 129) is 1.

**Output Driver State During EXTEST**

EXTEST allows the Internal Cell (Bit 137) in the Boundary Scan Register to control the state of Q, QINV drivers. That is, when Bit 137 = 1, Q, QINV drivers are enabled (i.e., driving High or Low), and when Bit 137 = 0, Q, QINV drivers are disabled (i.e., forced to High-Z state). See the Boundary Scan Register section for more information.

**ODT State During EXTEST and SAMPLE-Z**

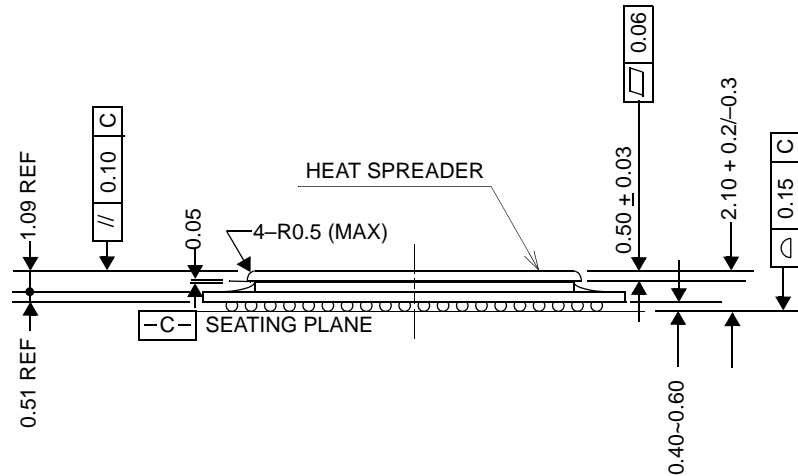
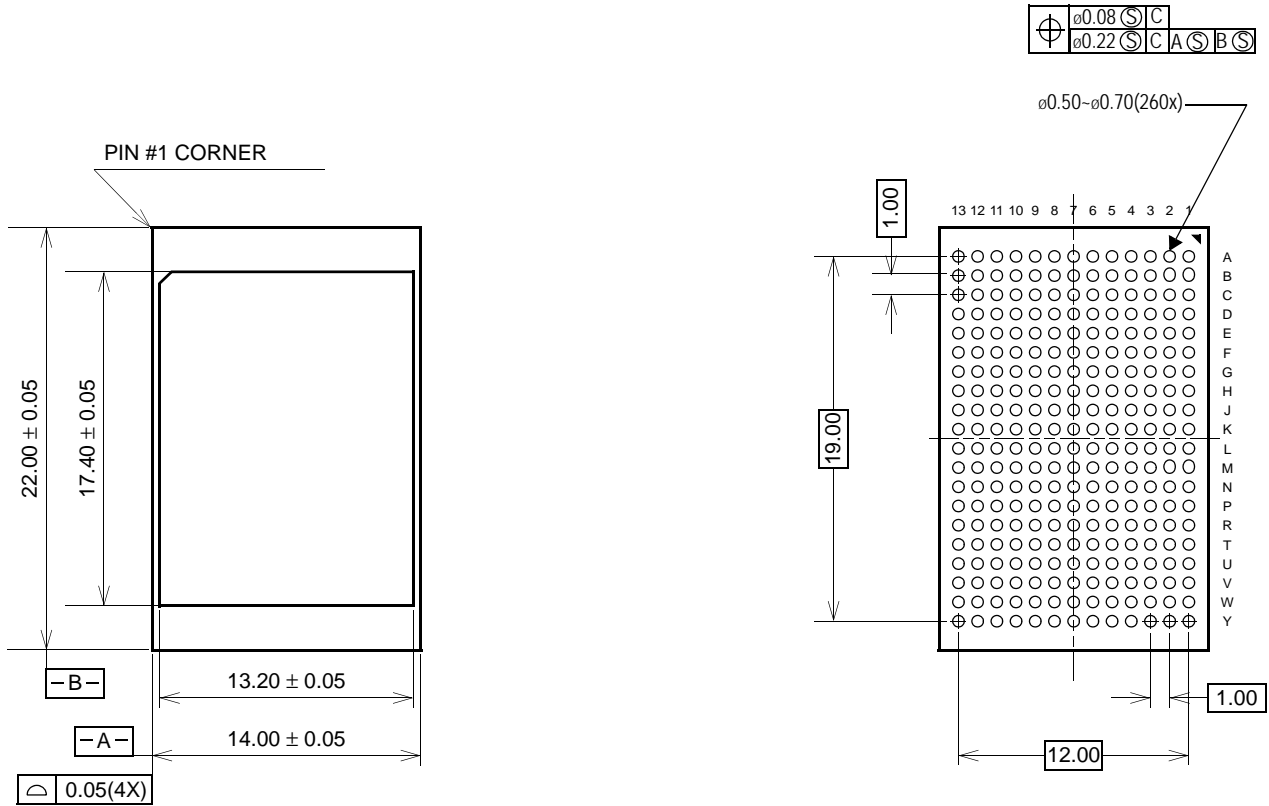
ODT on all inputs is disabled during EXTEST and SAMPLE-Z.

### Boundary Scan Register Bit Order Assignment

The table below depicts the order in which the bits are arranged in the Boundary Scan Register. Bit 1 is the LSB and Bit 137 is the MSB. When the Boundary Scan Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

| Bit | Pad | Bit | Pad | Bit | Pad | Bit | Pad | Bit | Pad      |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|----------|
| 1   | 7L  | 29  | 13E | 57  | 13V | 85  | 2W  | 113 | 2F       |
| 2   | 7K  | 30  | 10F | 58  | 11V | 86  | 3V  | 114 | 4F       |
| 3   | 9L  | 31  | 12F | 59  | 12W | 87  | 1V  | 115 | 1E       |
| 4   | 9K  | 32  | 11G | 60  | 10W | 88  | 4U  | 116 | 3E       |
| 5   | 8J  | 33  | 13G | 61  | 12Y | 89  | 2U  | 117 | 2D       |
| 6   | 7H  | 34  | 10G | 62  | 10Y | 90  | 3T  | 118 | 4D       |
| 7   | 9H  | 35  | 12G | 63  | 8V  | 91  | 1T  | 119 | 1C       |
| 8   | 7G  | 36  | 11H | 64  | 9U  | 92  | 4R  | 120 | 3C       |
| 9   | 8G  | 37  | 13H | 65  | 8T  | 93  | 2R  | 121 | 2B       |
| 10  | 9F  | 38  | 10J | 66  | 9R  | 94  | 3P  | 122 | 4B       |
| 11  | 8E  | 39  | 12J | 67  | 8P  | 95  | 1P  | 123 | 2A       |
| 12  | 7D  | 40  | 13K | 68  | 9N  | 96  | 4P  | 124 | 4A       |
| 13  | 9D  | 41  | 13L | 69  | 8M  | 97  | 2P  | 125 | 5A       |
| 14  | 8C  | 42  | 11L | 70  | 6M  | 98  | 3N  | 126 | 6A       |
| 15  | 7B  | 43  | 12M | 71  | 7N  | 99  | 1N  | 127 | 6B       |
| 16  | 8B  | 44  | 10M | 72  | 5N  | 100 | 4M  | 128 | 6C       |
| 17  | 9B  | 45  | 13N | 73  | 7P  | 101 | 2M  | 129 | 5D       |
| 18  | 7A  | 46  | 11N | 74  | 6P  | 102 | 3L  | 130 | 6E       |
| 19  | 9A  | 47  | 12P | 75  | 5R  | 103 | 1L  | 131 | 5F       |
| 20  | 10A | 48  | 10P | 76  | 6T  | 104 | 1K  | 132 | 6G       |
| 21  | 12A | 49  | 13P | 77  | 7U  | 105 | 2J  | 133 | 5H       |
| 22  | 10B | 50  | 11P | 78  | 5U  | 106 | 4J  | 134 | 6J       |
| 23  | 12B | 51  | 12R | 79  | 6V  | 107 | 1H  | 135 | 5K       |
| 24  | 11C | 52  | 10R | 80  | 6W  | 108 | 3H  | 136 | 5L       |
| 25  | 13C | 53  | 13T | 81  | 7Y  | 109 | 2G  | 137 | Internal |
| 26  | 10D | 54  | 11T | 82  | 4Y  | 110 | 4G  |     |          |
| 27  | 12D | 55  | 12U | 83  | 2Y  | 111 | 1G  |     |          |
| 28  | 11E | 56  | 10U | 84  | 4W  | 112 | 3G  |     |          |

260-Pin BGA Package Drawing (Package K)



|                |      |                      |      |
|----------------|------|----------------------|------|
| Ball Pitch:    | 1.00 | Substrate Thickness: | 0.51 |
| Ball Diameter: | 0.60 | Mold Thickness:      | —    |

**Ordering Information — GSI SigmaQuad-IVe ECCRAM**

| Org     | Part Number         | Type             | Package                    | Speed (MHz) | T <sub>A</sub> |
|---------|---------------------|------------------|----------------------------|-------------|----------------|
| 8M x 18 | GS81314PQ18K-1333   | SigmaQuad-IVe B2 | 260-Pin BGA                | 1333        | C              |
| 8M x 18 | GS81314PQ18K-1250   | SigmaQuad-IVe B2 | 260-Pin BGA                | 1250        | C              |
| 8M x 18 | GS81314PQ18K-1100   | SigmaQuad-IVe B2 | 260-Pin BGA                | 1100        | C              |
| 8M x 18 | GS81314PQ18K-1000   | SigmaQuad-IVe B2 | 260-Pin BGA                | 1000        | C              |
| 8M x 18 | GS81314PQ18K-1333I  | SigmaQuad-IVe B2 | 260-Pin BGA                | 1333        | I              |
| 8M x 18 | GS81314PQ18K-1250I  | SigmaQuad-IVe B2 | 260-Pin BGA                | 1250        | I              |
| 8M x 18 | GS81314PQ18K-1100I  | SigmaQuad-IVe B2 | 260-Pin BGA                | 1100        | I              |
| 8M x 18 | GS81314PQ18K-1000I  | SigmaQuad-IVe B2 | 260-Pin BGA                | 1000        | I              |
| 4M x 36 | GS81314PQ36K-1333   | SigmaQuad-IVe B2 | 260-Pin BGA                | 1333        | C              |
| 4M x 36 | GS81314PQ36K-1250   | SigmaQuad-IVe B2 | 260-Pin BGA                | 1250        | C              |
| 4M x 36 | GS81314PQ36K-1100   | SigmaQuad-IVe B2 | 260-Pin BGA                | 1100        | C              |
| 4M x 36 | GS81314PQ36K-1000   | SigmaQuad-IVe B2 | 260-Pin BGA                | 1000        | C              |
| 4M x 36 | GS81314PQ36K-1333I  | SigmaQuad-IVe B2 | 260-Pin BGA                | 1333        | I              |
| 4M x 36 | GS81314PQ36K-1250I  | SigmaQuad-IVe B2 | 260-Pin BGA                | 1250        | I              |
| 4M x 36 | GS81314PQ36K-1100I  | SigmaQuad-IVe B2 | 260-Pin BGA                | 1100        | I              |
| 4M x 36 | GS81314PQ36K-1000I  | SigmaQuad-IVe B2 | 260-Pin BGA                | 1000        | I              |
| 8M x 18 | GS81314PQ18GK-1333  | SigmaQuad-IVe B2 | ROHS-Compliant 260-Pin BGA | 1333        | C              |
| 8M x 18 | GS81314PQ18GK-1250  | SigmaQuad-IVe B2 | ROHS-Compliant 260-Pin BGA | 1250        | C              |
| 8M x 18 | GS81314PQ18GK-1100  | SigmaQuad-IVe B2 | ROHS-Compliant 260-Pin BGA | 1100        | C              |
| 8M x 18 | GS81314PQ18GK-1000  | SigmaQuad-IVe B2 | ROHS-Compliant 260-Pin BGA | 1000        | C              |
| 8M x 18 | GS81314PQ18GK-1333I | SigmaQuad-IVe B2 | ROHS-Compliant 260-Pin BGA | 1333        | I              |
| 8M x 18 | GS81314PQ18GK-1250I | SigmaQuad-IVe B2 | ROHS-Compliant 260-Pin BGA | 1250        | I              |
| 8M x 18 | GS81314PQ18GK-1100I | SigmaQuad-IVe B2 | ROHS-Compliant 260-Pin BGA | 1100        | I              |
| 8M x 18 | GS81314PQ18GK-1000I | SigmaQuad-IVe B2 | ROHS-Compliant 260-Pin BGA | 1000        | I              |
| 4M x 36 | GS81314PQ36GK-1333  | SigmaQuad-IVe B2 | ROHS-Compliant 260-Pin BGA | 1333        | C              |
| 4M x 36 | GS81314PQ36GK-1250  | SigmaQuad-IVe B2 | ROHS-Compliant 260-Pin BGA | 1250        | C              |
| 4M x 36 | GS81314PQ36GK-1100  | SigmaQuad-IVe B2 | ROHS-Compliant 260-Pin BGA | 1100        | C              |
| 4M x 36 | GS81314PQ36GK-1000  | SigmaQuad-IVe B2 | ROHS-Compliant 260-Pin BGA | 1000        | C              |
| 4M x 36 | GS81314PQ36GK-1333I | SigmaQuad-IVe B2 | ROHS-Compliant 260-Pin BGA | 1333        | I              |
| 4M x 36 | GS81314PQ36GK-1250I | SigmaQuad-IVe B2 | ROHS-Compliant 260-Pin BGA | 1250        | I              |
| 4M x 36 | GS81314PQ36GK-1100I | SigmaQuad-IVe B2 | ROHS-Compliant 260-Pin BGA | 1100        | I              |
| 4M x 36 | GS81314PQ36GK-1000I | SigmaQuad-IVe B2 | ROHS-Compliant 260-Pin BGA | 1000        | I              |

**Note:** C = Commercial Temperature Range. I = Industrial Temperature Range.

**Revision History**

| Rev. Code         | Types of Changes<br>Format or Content | Revisions                   |
|-------------------|---------------------------------------|-----------------------------|
| GS81314PQ1836K_r1 | —                                     | • Creation of new datasheet |
|                   |                                       | •                           |
|                   |                                       | •                           |