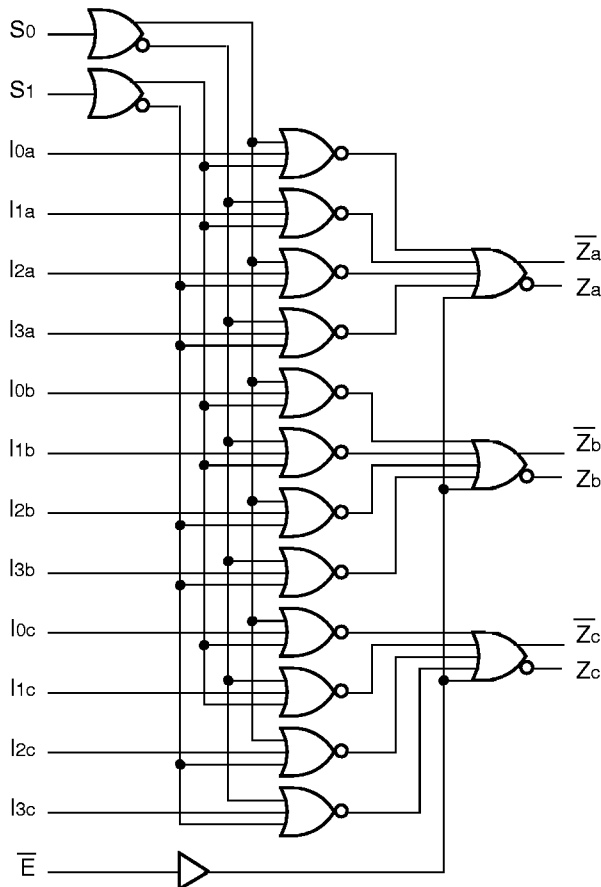


FEATURES

- Max. propagation delay of 1000ps
- IEE min. of -68mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- 40% faster than National or Signetics
- 40% lower power than National or Signetics
- Function and pinout compatible with National and Signetics F100K
- ESD protection of 2000V
- Available in 24-pin CERDIP, 24-pin CERPAC and 28-pin PLCC packages

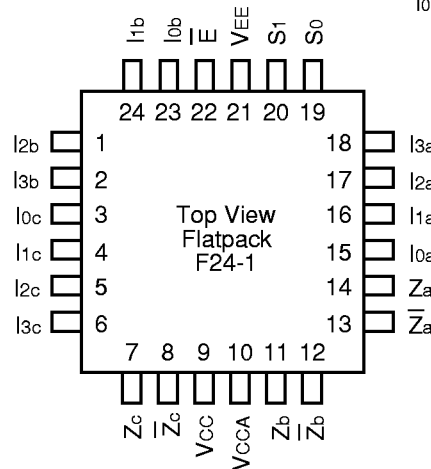
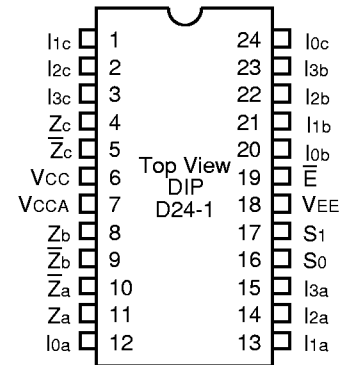
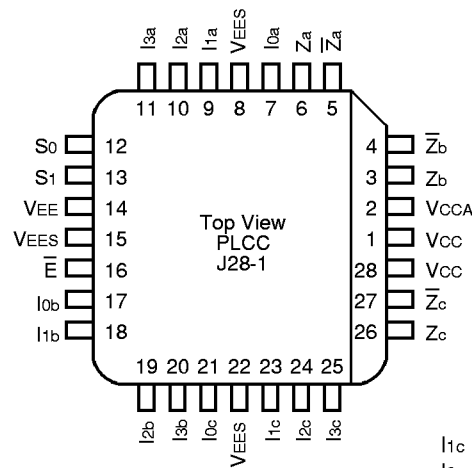
BLOCK DIAGRAM



DESCRIPTION

The SY100S371 is an ultra-fast triple 4-input multiplexer with true and complementary outputs designed for use in high-performance ECL systems. The multiplexer is controlled by common select inputs S0 and S1. A logic HIGH on the Enable (\bar{E}) control input takes the outputs to a logic LOW. The inputs on the device have 75KΩ pull-down resistors.

PIN CONFIGURATIONS



PIN NAMES

Pin	Function
$I_{0X} - I_{3X}$	Data Inputs (x = a, b or c)
S ₀ , S ₁	Select Inputs
\bar{E}	Enable Input (Active LOW)
Z _a – Z _c	Data Outputs
$\bar{Z}_a - \bar{Z}_c$	Complementary Data Outputs
V _{EE} S	V _{EE} Substrate
V _{CCA}	V _{CC0} for ECL Outputs

TRUTH TABLE⁽¹⁾

Inputs			Outputs
\bar{E}	S ₀	S ₁	Z _n
L	L	L	I _{0X}
L	H	L	I _{1X}
L	L	H	I _{2X}
L	H	H	I _{3X}
H	X	X	L

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC ELECTRICAL CHARACTERISTICS

V_{EE} = -4.2V to -5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current $I_{0X} - I_{3X}$ S ₀ , S ₁ , \bar{E}	—	—	250 300	μA	V _{IN} = V _{IH} (Max.)
I _{EE}	Power Supply Current	-68	-48	-34	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay I _{OX} – I _{3X} to Output	300	1200	300	1200	300	1200	ps	
tPLH tPHL	Propagation Delay S ₀ , S ₁ to Output	400	1600	400	1600	400	1600	ps	
tPLH tPHL	Propagation Delay S ₀ , S ₁ to Output	400	1500	400	1500	400	1500	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

CERPACK

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND

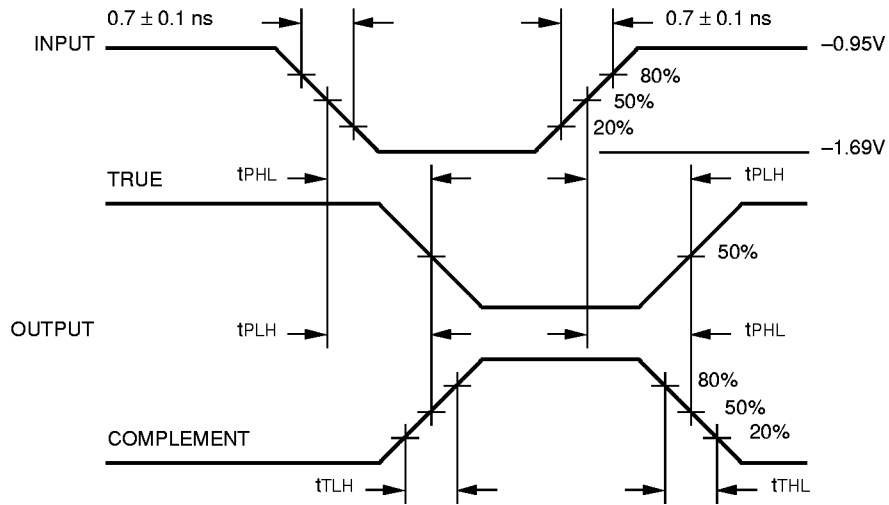
Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay I _{OX} – I _{3X} to Output	300	1100	300	1100	300	1100	ps	
tPLH tPHL	Propagation Delay S ₀ , S ₁ to Output	400	1500	400	1500	400	1500	ps	
tPLH tPHL	Propagation Delay S ₀ , S ₁ to Output	400	1400	400	1400	400	1400	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

PLCC

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay I _{OX} – I _{3X} to Output	300	1000	300	1000	300	1000	ps	
tPLH tPHL	Propagation Delay S ₀ , S ₁ to Output	400	1400	400	1400	400	1400	ps	
tPLH tPHL	Propagation Delay S ₀ , S ₁ to Output	400	1300	400	1300	400	1300	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM



Propagation Delay and Transition Times

NOTE:

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S371DC	D24-1	Commercial
SY100S371FC	F24-1	Commercial
SY100S371JC	J28-1	Commercial
SY100S371JCTR	J28-1	Commercial

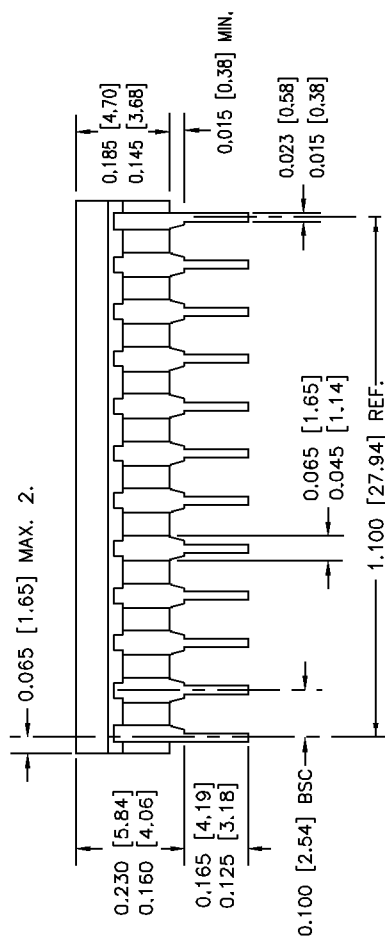
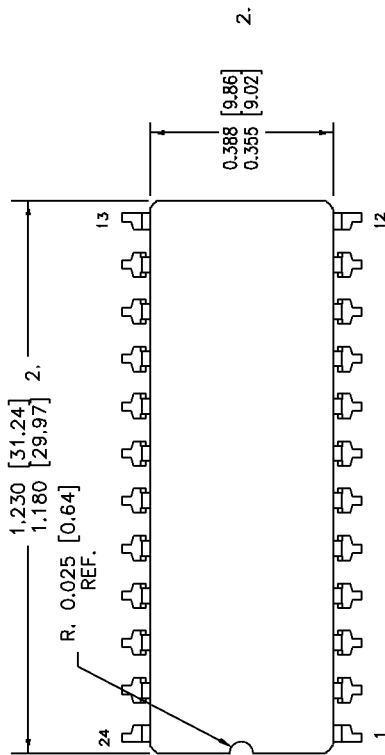
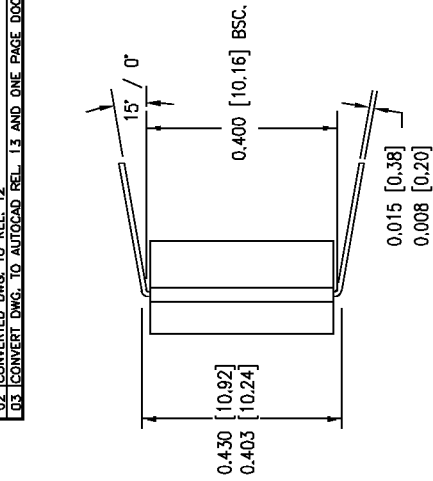
24 LEAD CERDIP (D24-1)

FILE/REV #: PD0003A03

PD/0003/ASCORP

PAGE 1 OF 1

REV.	REVISION DESCRIPTION	DATE
01	CONVERT DWG. TO DESIGNER VERSION 4.0 FORMAT.	12/30/93
02	CONVERTED DWG. TO REL. 12	03/15/96
03	CONVERT DWG. TO AUTOCAD REL. 1.3 AND ONE PAGE DOCUMENT.	02/18/98



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
- THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.



3250 SCOTT BOULEVARD
SANTA CLARA CA 95054
TEL: 408-980-9191
FAX: 408-567-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	24 LEAD CERDIP (400" WIDE) PACKAGE OUTLINE
ORIGINATOR: FERMIN G. LURRITA	02/23/98	QUALITY: MARSHALL WILDER		A	
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			
RELEASE DATE:					

SCALE
N/A
REVISION
03

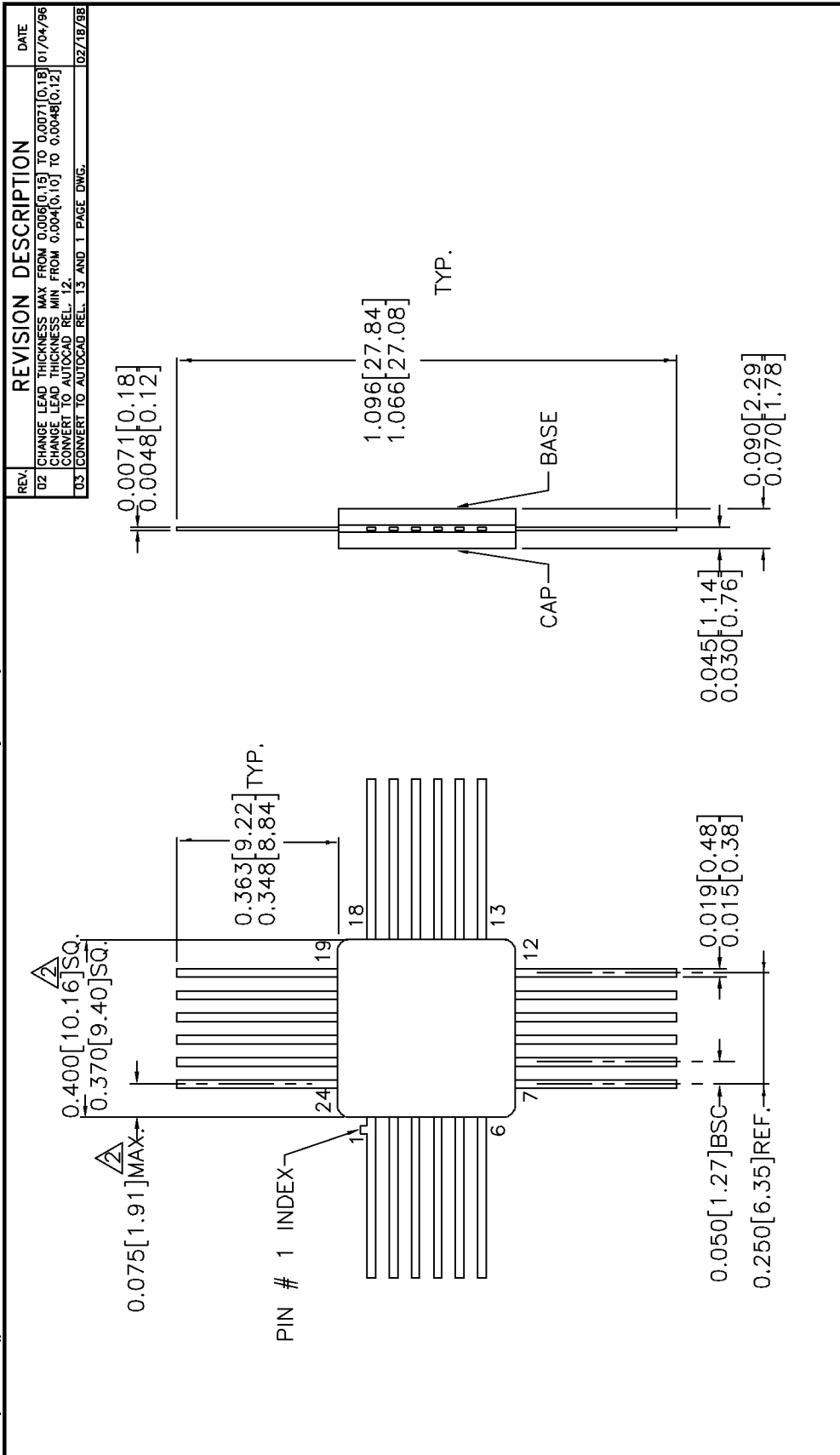
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24 LEAD CERPACK (F24-1)

FILE/REV #: PD0006A03

PD/0006/ASCORP

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<p>SYNERGY SEMICONDUCTOR</p>		<p>3250 SCOTT BOULEVARD SANTA CLARA CA 95054 TEL: 408-980-9191 FAX: 408-587-7878</p>	
<p>ORIGINATOR: FERNUN G. URRUTIA</p>	<p>DATE 02/23/98</p>	<p>APPROVALS QUALITY: MARSHALL WILDER DOCUMENT CONTROL: BRIAN SANFILIPPO</p>	<p>DATE</p>
<p>CHK'D: WON CHANG</p>	<p>RELEASE DATE:</p>	<p>SIZE A</p>	<p>24 LEAD CERPACK PACKAGE OUTLINE</p>
<p>NOTES: 1. DIMENSIONS ARE IN INCHES[MM]. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES. 3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.</p>			<p>SCALE N/A</p>
<p>REVISION</p>			<p>REVISION 03</p>
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28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)

FILE/REV #: PD0008A03

PD/0008/ASCORP

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