MOS DIGITAL INTEGRATED CIRCUIT
μPD6120

MULTI-PURPOSE REMOTE CONTROL TRANSMITTER IC
CMOS LSI

DESCRIPTION

The μPD6120 is an LSI for the transmission of general-purpose, infrared, remote control codes to TVs, VTRs, audio equipment, air-conditioners, and so on. The LSI, combined with external diodes and resistors, can create 1 024 custom codes. If the mask ROM is used, 65 536 custom codes can be created with it. A send code is composed of leader code, custom code (16 bits), and data code (16 bits). Codes generated by the LSI can be applied to various systems by decoding with a microprocessor.

FEATURES

- Operation at low voltages : V_{DD} = 2.0 to 3.3 V
- Low current consumption : 1 μA max. at standby
- Custom codes : 1 024 codes with external diodes and resistors; 65 536 codes with mask ROM
- Data code : 20 codes (single action); 3 codes (dual action)
- Send codes compatible with μPD1913C, μPD1943G, μPD6102G, μPD6121G, and μPD6122G
- Standard products : μPD6120C-101 (pins compatible with μPD1913C; the capacity of capacitors connected to oscillator pins is different from that of μPD1913C) μPD6120C-102 (with built-in custom code ROM)

ORDERING INFORMATION

Order Code	Package	Features	Quality Grade
μPD6120C-101	16-pin plastic DIP (300 mil)	Standard product (pins compatible with μPD1913C)	Standard
μPD6120C-102	16-pin plastic DIP (300 mil)	Standard product (a part of custom codes stored in ROM)	Standard
μPD6120C-xxx	16-pin plastic DIP (300 mil)	Custom product	Standard

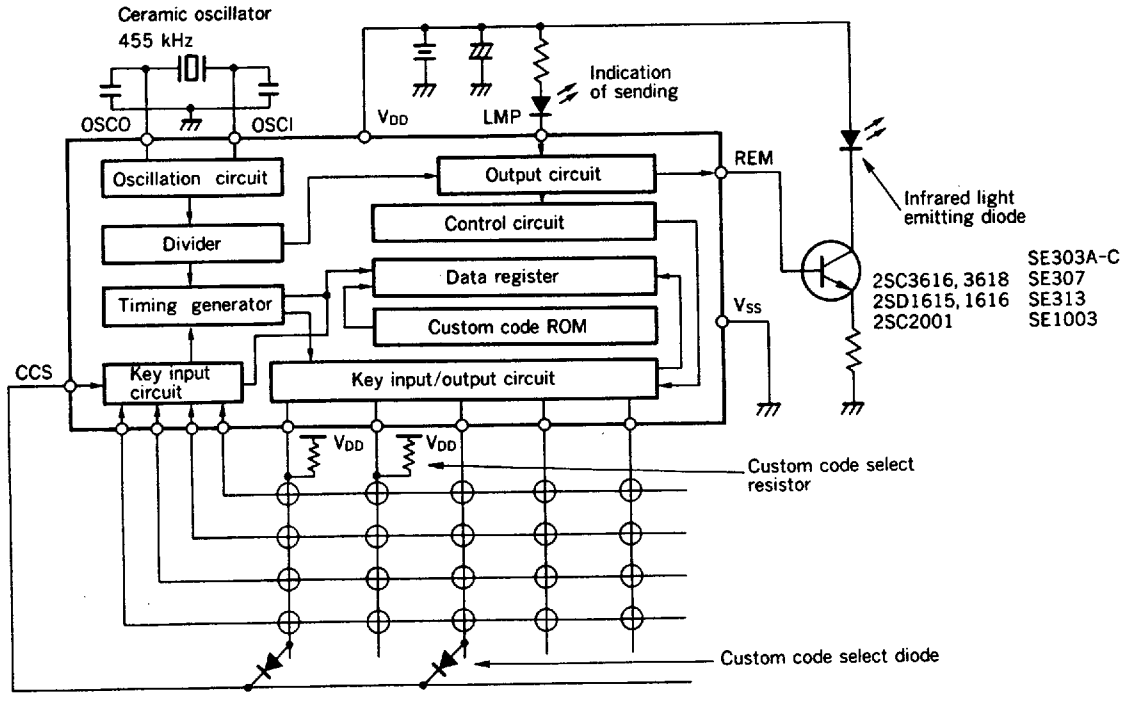
In custom products, custom codes are written to the mask ROM.

Custom products with the mask ROM do not require external elements, such as those used with standard products for coding.

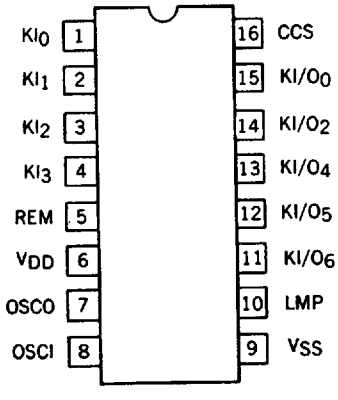
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Document No. IC-1812B
(O.D.No. IC-6856C)

BLOCK DIAGRAM



PIN CONNECTIONS (Top View)



Pin		
1	KI_0	Key Input 0
2	KI_1	Key Input 1
3	KI_2	Key Input 2
4	KI_3	Key Input 3
5	REM	Remote Output
6	V_{DD}	Power
7	OSCO	Oscillator Output
8	OSCI	Oscillator Input
9	V_{SS}	
10	LMP	Lamp Output
11	KI/O_6	Key I/O 6
12	KI/O_5	Key I/O 5
13	KI/O_4	Key I/O 4
14	KI/O_2	Key I/O 2
15	KI/O_0	Key I/O 0
16	CCS	Customer Code Select Input

Description of Pins

(1) KI_0 to KI_3, KI/O_0 to KI/O_6 (Key Input/Output)

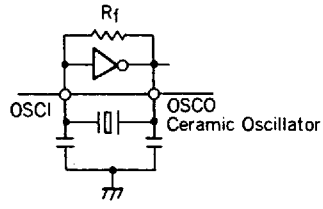
A pull-down resistor is inserted between a key input pin and the V_{SS} pin. If more than two keys are pressed together, the multi-action protective circuit inhibits transmission. While two keys are pressed together (±36 ms), transmission is inhibited; when they are released, the key that is released last becomes effective.

When a key is pressed, the system starts reading custom codes and data codes, and 36 ms later a send code is output from the REM pin. If a key is pressed for this 36 ms, a transmission of code is completed. If a key is held depressed for 108 ms or longer, only a leader code is transmitted continuously. The LSI can handle as quick a key operation as 126 ms (an ON-to-ON interval), enabling use of systems with very quick response.

(2) OSCI, OSCO (Oscillator Input/Output)

The oscillation circuit starts operating on key input to the LSI.

It uses a ceramic oscillator of 400 to 500 kHz that requires no adjustment.



(3) V_{DD} (Power)

The LSI operates with 3 V supplied by two dry cells and has a wide operation voltage of 2.0 to 3.3 V. The supply current is not more than 1 μA unless a key is pressed because the oscillator is halted.

(4) REM (Remote Output)

The LSI outputs from the REM pin a send code made up of leader code, custom code (16 bits) and data code (16 bits). (See Send Codes below.)

(5) CCS (Custom Code Select Input)

Custom codes can be created with diodes connected to the CCS pin and KI/O pins. When the CCS pin and KI/O pins are connected through diodes, the custom code's bits corresponding to the connected KI/O pins are set to 1, and the other bits are set to 0.

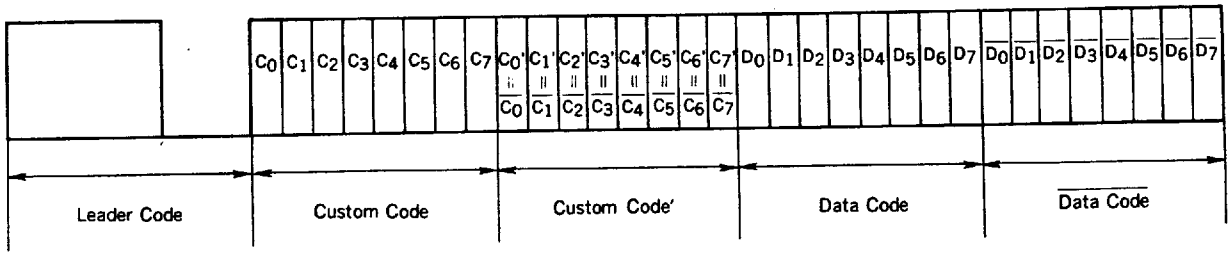
(6) LMP (Lamp Output)

A low-level signal is output from the LMP pin while a send code is output from the REM pin.

Send Codes

(1) REM Output

A send code is composed of leader code, 16-bit custom code, and 8-bit data code. An 8-bit inverse data code is also sent, so a code output in one transmission consists of 32 bits.



REM Output Code

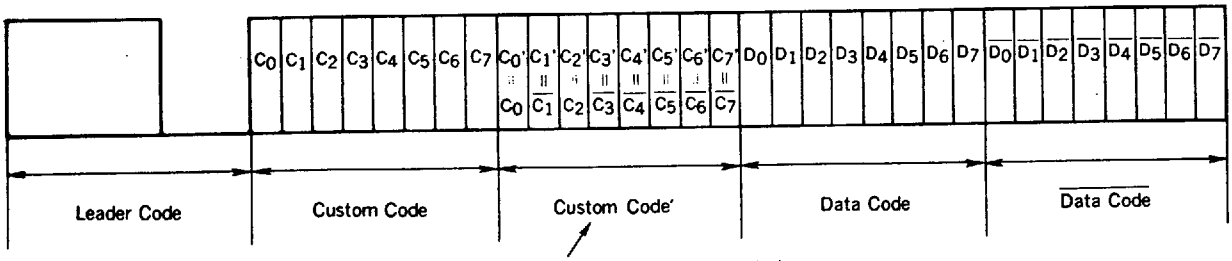
A leader code is composed of a 9 ms carrier wave and a 4.5 ms OFF wave and serves as a leader for the following codes. This allows a receiving microcomputer to effectively assign its operation to the reception of codes and other processes. Codes are sent in Pulse Position Modulation (PPM) to discriminate between 1 and 0 by an interval between pulses. Individual codes consist of eight bits, and corresponding inverse codes are also sent. Hence, constructed systems hardly ever malfunction.

(2) Expansion of Custom Codes

When only diodes are used to create custom codes, as in the μPD1913C, codes are output in the format shown above in section (1).

Custom codes can be expanded by connecting a 200 kΩ pull-up resistor to any of the KI/O_0 to KI/O_6 pins to prevent corresponding bits of an output custom code' from being inverted.

Coding a custom code' provides 1 024 custom codes, 32 times those of the μPD1913C.



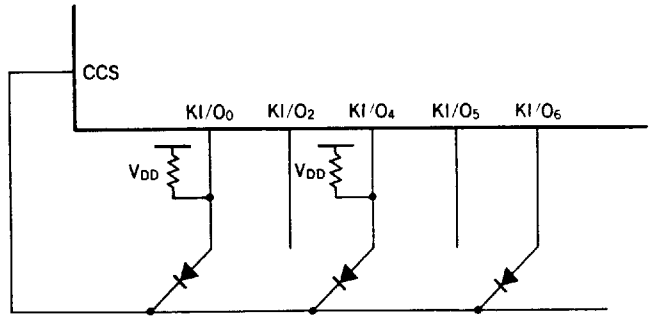
* A pull-up resistor is connected to the KI/O_0 and KI/O_2 pins. C_0 and C_2 are output without inversion (uninverted bit).

(3) Custom Codes

Diodes connected to the CCS and KI/O pins and pull-up resistors connected to the KI/O pins make 1 024 custom codes available for selection for output from the REM pin. For assignment of custom codes other than 00000000 (a code that is created when no diode is connected), consult NEC to prevent inter-system malfunction.

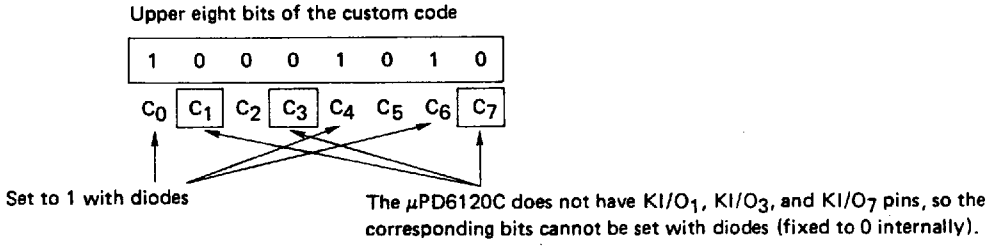
Example of coding

(Example of setup)



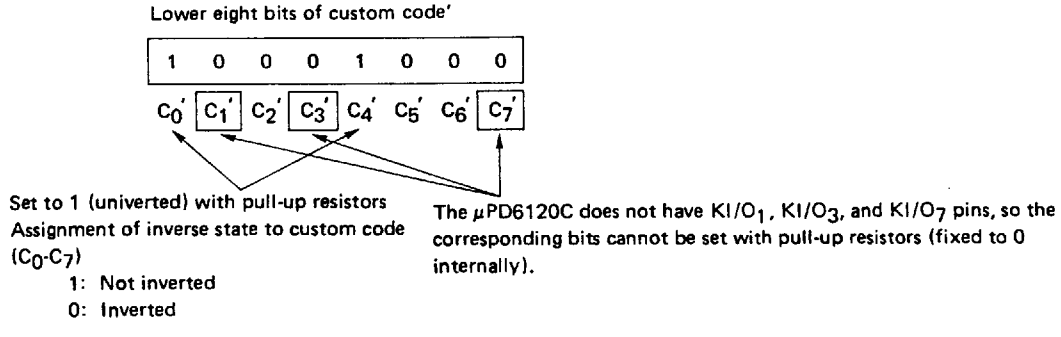
The state of the upper eight bits of a custom code is determined with diodes connected to the CCS and KI/O pins.

Custom code to be created



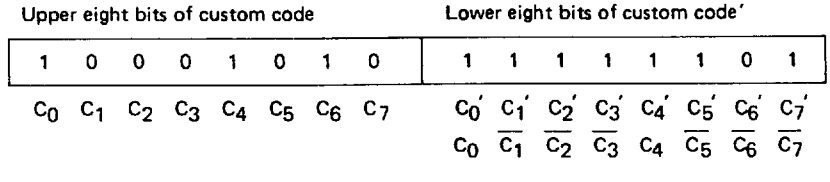
The state of the lower eight bits of a custom code' is determined with pull-up resistors connected to the KI/O pins.

Custom code to be created



The above coding brings about an output of the following custom code.

Custom code



(4) Custom Coding on Mask ROM

Custom codes can be written to the mask ROM without connecting external diodes or resistors. By combining the mask ROM with external diodes and resistors, custom codes different from those contained in the mask ROM can be output. When the mask ROM is to be used, Ver I and Ver II are available for selection.

	Upper Eight Bits of Custom Code	Lower Eight Bits of Custom Code'
Ver I	Determined by logical OR of internal ROM1 and external diode positions.	Determined by logical OR of internal ROM2 and external pull-up resistor positions.
Ver II	C_0, C_1, C_2: Determined by connecting the CCS pin with any of KI/O_0 to KI/O_6. C_3 to C_7: Determined by the internal ROM3 and whether an external pull-up resistor is connected to KI/O_6.	Determined by logical OR of internal ROM2 and external pull-up resistor positions (KI/O_0 to KI/O_5).

* The standard product μPD6120C-101 is Ver I and is pin compatible with the μPD1913C.
When the μPD6120C-101 is to be pin compatible with the μPD1913C, note the following:

(1) Change the capacity of capacitors to be connected to oscillator pins (pin 8 (OSCO), pin 7 (OSCI)). (See page 15.)
The internal ROM is programmed as follows:

ROM1
Upper eight bits of custom code

0	0	0	0	0	0	0	0
C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7

ROM2
Lower eight bits of custom code'

0	0	0	0	0	0	0	0
C_0'	C_1'	C_2'	C_3'	C_4'	C_5'	C_6'	C_7'

* The standard product μPD6120C-102 is Ver II.
The internal ROM is programmed as follows:

ROM3
Bits C_7, C_6, C_5, C_4, and C_3 of custom code

ROM3	C_7	C_6	C_5	C_4	C_3	KI/O_6
ROM3-0	0	0	0	0	0	Not connected
ROM3-2	1	0	0	0	0	Connected

ROM2
Lower eight bits of custom code'

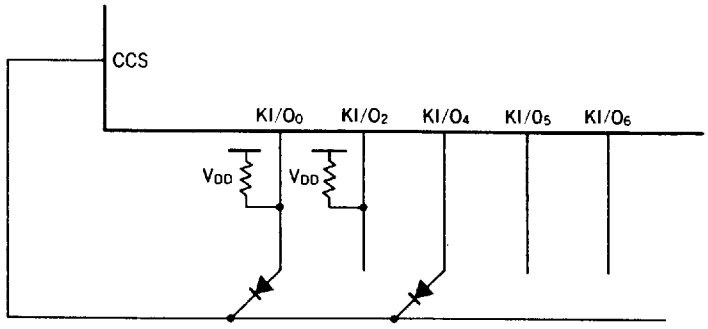
0	0	0	0	0	0	0	0
C_0'	C_1'	C_2'	C_3'	C_4'	C_5'	C_6'	C_7'

(Ver I)

Internal custom code ROM1 and ROM2 (16 bits in total) are effective. ROM1 (8 bits) corresponds to the external diodes, and ROM2 (8 bits) to the external pull-up resistors.

Example of coding

(Example of setup)



The state of the upper eight bits of a custom code is determined by logical OR of external diode positions and internal ROM1.

External code setting (see the diagram above)

Upper eight bits of custom code

1	0	0	0	1	0	0	0
C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7

Diode position (KI/O_0, KI/O_4)

The μPD6120C does not have KI/O_1, KI/O_3, and KI/O_7 pins, so the corresponding bits cannot be set with diodes (fixed to 0 internally).

Internal ROM1 (example of coding)

ROM1

0	1	0	1	0	0	0	0

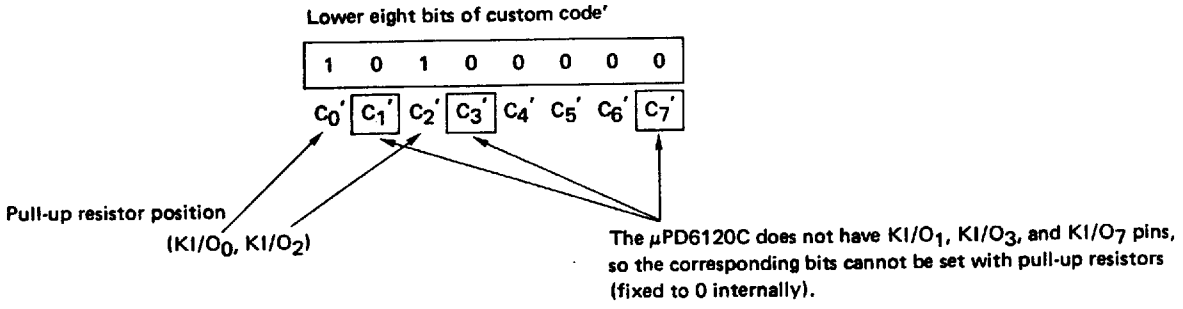
Logical OR of external code setting and internal ROM1

1	1	0	1	1	0	0	0

Custom code

The state of the lower eight bits of a custom code' is determined by logical OR of external pull-up resistor positions and internal ROM2.

External code setting (see the diagram above)



Internal ROM2 (example of coding)

ROM2

0	1	0	0	0	0	0	1

Logical OR of external code setting and internal ROM2

1	1	1	0	0	0	0	1

Assignment of inverse state to custom code (C_0 to C_7)

1: Not inverted
0: Inverted

The above code setting with pull-up resistors, diodes, ROM1, and ROM2 brings about the output of the following custom code.

Custom Code

Upper eight bits of custom code								Lower eight bits of custom code'							
1	1	0	1	1	0	0	0	1	1	0	0	0	1	1	0
C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_0'	C_1'	C_2'	C_3'	C_4'	C_5'	C_6'	C_7'
								C_0	C_1	$\overline{C_2}$	$\overline{C_3}$	$\overline{C_4}$	$\overline{C_5}$	$\overline{C_6}$	C_7

(Ver II)

In Ver II, the CCS pin cannot recognize external diodes.

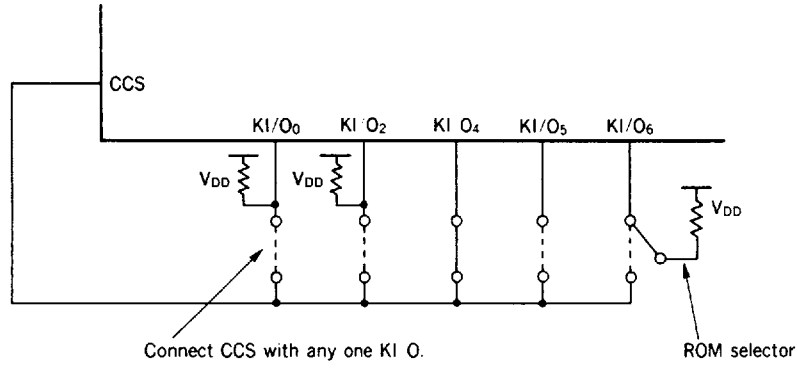
Internal custom code ROM2 and ROM3 (18 bits in total) are effective. ROM3 (10 bits) has two 5-bit channels of C_7, C_6, C_5, C_4, and C_3 for selection. ROM2 (8 bits) corresponds to external pull-up resistors (excluding KI/O_6). The state (0 or 1) of the upper bits C_2, C_1, and C_0 of a custom code is determined by connection of the CCS pin with any of KI/O_0 to KI/O_6, as shown in the table below.

CCS-	C_2	C_1	C_0
KI/O_0	0	0	0
KI/O_2	0	1	0
KI/O_4	1	0	0
KI/O_5	1	0	1
KI/O_6	1	1	0

With CCS being open,
$(C_2, C_1, C_0) = (0, 0, 0)$

Example of coding

(Example of setup)



The state of the upper bits C_2, C_1, and C_0 of a custom code is determined by connecting the CCS pin with any of KI/O_0 to KI/O_6. In the example shown above, they are set as follows:

0	0	1
C_0	C_1	C_2

The state of the upper bits C_7, C_6, C_5, C_4, and C_3 of a custom code is set to either state of two channels in intrnal ROM3, depending on whether a pull-up resistor is connected to KI/O_6.

KI/O_6	ROM3	C_7	C_6	C_5	C_4	C_3
Pull-up resistor not connected	ROM3-0	1	0	1	1	0
Pull-up resistor connected	ROM3-2	0	0	1	1	1

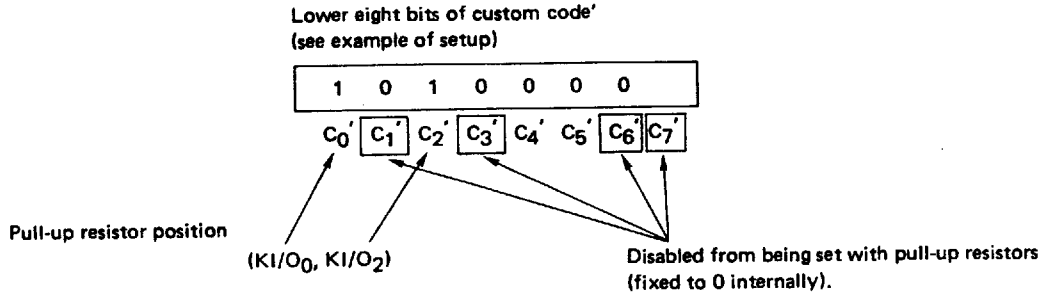
(Example of code setting)

In the example shown above, the upper bits C_3 to C_7 of a custom code are set as follows:

1	1	1	0	0
C_3	C_4	C_5	C_6	C_7

The state of the lower eight bits of a custom code' is determined by logical OR of KI/O_0 to KI/O_5 and external pull-up resistor positions.

External code setting



Internal ROM2 (example of coding)

ROM2

0	1	0	0	0	0	1	0
C_0'	C_1'	C_2'	C_3'	C_4'	C_5'	C_6'	C_7'

Logical OR of external code setting and internal ROM2

1	1	1	0	0	0	1	0

Assignment of inverse state to custom code (C_0 to C_7)

1: Not inverted
0: Inverted

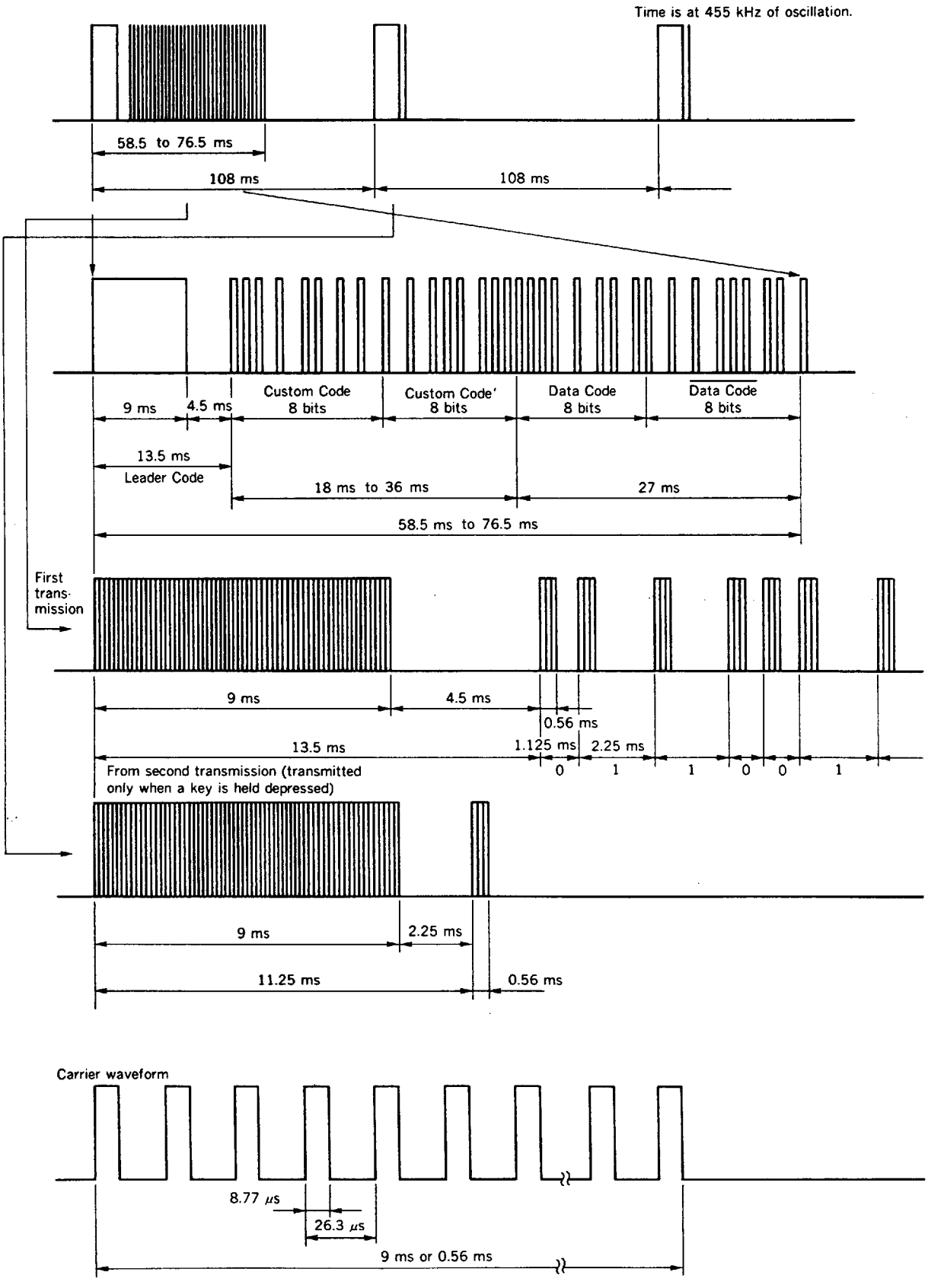
The above code setting with pull-up resistors, CCS-KI/O connection, ROM2, and ROM3 brings about the output of the following custom code.

Custom Code

Upper eight bits of custom code								Lower eight bits of custom code'							
0	0	1	1	1	1	0	0	0	0	1	0	0	0	0	1
C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_0'	C_1'	C_2'	C_3'	C_4'	C_5'	C_6'	C_7'
								C_0	C_1	C_2	$\overline{C_3}$	$\overline{C_4}$	$\overline{C_5}$	C_6	$\overline{C_7}$

Note: A send custom code is output from LSB.

OUTPUT WAVEFORMS AT REM PIN



Carrier frequency·····$f_c = f_{OSC}/12 = 38$ kHz

Key Data Code

KEY	CONNECTION					DATA CODE								NOTES
	KI_0	KI_1	KI_2	KI_3	KI/O	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	
K 1	*				KI/O_0	0	0	0	0	0	0	0	0	
K 2		*				1	0	0	0	0	0	0	0	
K 3			*			0	1	0	0	0	0	0	0	
K 4				*		1	1	0	0	0	0	0	0	
K 9	*				KI/O_2	0	0	0	1	0	0	0	0	
K10		*				1	0	0	1	0	0	0	0	
K11			*			0	1	0	1	0	0	0	0	
K12				*		1	1	0	1	0	0	0	0	
K17	*				KI/O_4	0	0	0	0	1	0	0	0	
K18		*				1	0	0	0	1	0	0	0	
K19			*			0	1	0	0	1	0	0	0	
K20				*		1	1	0	0	1	0	0	0	
K21	*				KI/O_5	0	0	1	0	1	0	0	0	
K22		*				1	0	1	0	1	0	0	0	
K23			*			0	1	1	0	1	0	0	0	
K24				*		1	1	1	0	1	0	0	0	
K25	*				KI/O_6	0	0	0	1	1	0	0	0	
K26		*				1	0	0	1	1	0	0	0	
K27			*			0	1	0	1	1	0	0	0	
K28				*		1	1	0	1	1	0	0	0	

Dual Action Key Code

KEY	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	NOTES
K21 + K22	1	0	1	0	1	1	0	0	
K21 + K23	0	1	1	0	1	1	0	0	
K21 + K24	1	1	1	0	1	1	0	0	

A data code consists of eight bits. D_0 to D_4 correspond to K1 to K28 of the key matrix. D_5 is set to 1 on dual action.

When a key is held depressed, only a leader code is sent from the second repetition to reduce the power dissipation of the infrared light emitting diode. The duty of leader code transmission dominates over the infrared light emitting diode — the average current to the diode is about 3 % of I_{peak}. At 455 kHz of oscillation, signals are modulated at 38 kHz, 1/3 duty.

Dual Action

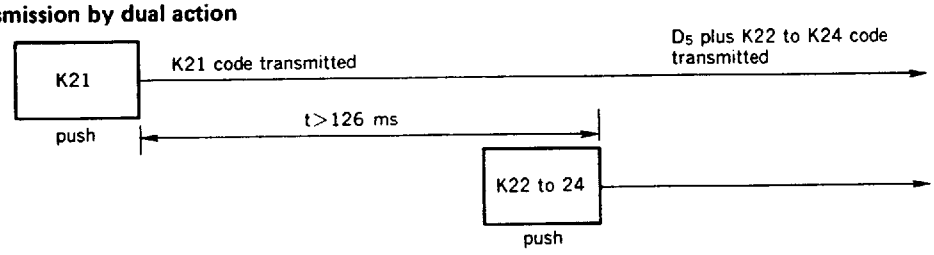
All keys are provided with a dual-action preventive circuit to prevent transmission when two or more keys are pressed together. However, when K21 and K22, K21 and K23, or K21 and K24 are pressed together, a code is transmitted with D_5 set to 1. Transmission in this mode is effective only when K21 is pressed first, then after not less than 126 ms any of K22 to K24 is pressed. This mode is suitable to prevent an error in cassette tape recording.

Dual Action Key Code

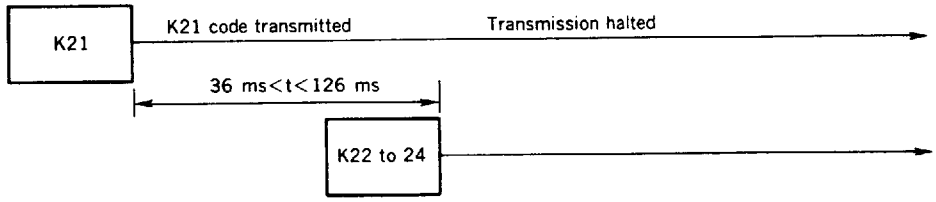
KEY	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
K21 + K22	1	0	1	0	1	1	0	0
K21 + K23	0	1	1	0	1	1	0	0
K21 + K24	1	1	1	0	1	1	0	0

Dual Action Timing

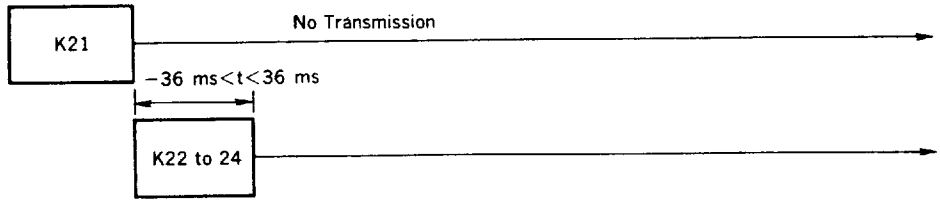
(a) Transmission by dual action



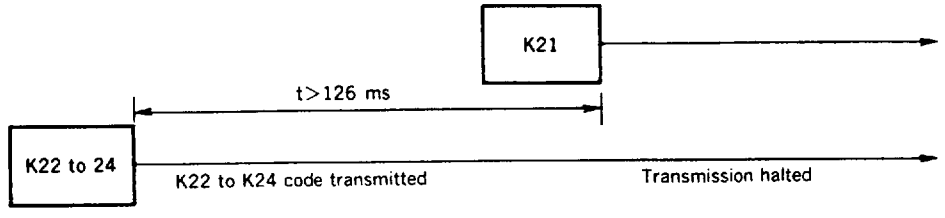
(b) No operaiton



(c) No operation



(d) No operation



Mask ROM Version

In this LSI, custom codes are written to the mask ROM to output any custom codes without using external elements. ROM configuration for custom coding is swhon below.

		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0	ROM SEL PULL UP	
Ver I or II SEL		0	0	0	0	0	0	1/0	1/0		
ROM1		1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0		
ROM2		1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	KI/O_6	KI/O_7
ROM3	0	1/0	1/0	1/0	1/0	1/0	0	0	0	Not connected	Not connected
	1	1/0	1/0	1/0	1/0	1/0	0	0	0	Not connected	Connected
	2	1/0	1/0	1/0	1/0	1/0	0	0	0	Connected	Not connected
	3	1/0	1/0	1/0	1/0	1/0	0	0	0	Connected	Connected

1) Specify 01_H to select Ver I, and 02_H, Ver II.
2) ROM1 is used to determine a pattern of C_7 to C_0 when Ver I is selected. Setting "1" sends 1, and setting "0", 0.
3) ROM2 is used in common between Ver I and Ver II to determine whether to output C_7' to C_0' inverse to corresponding C_7 to C_0. Setting '1" means an uninverted output, and "0", an inverse output.
4) ROM3 is used to select a pattern of C_7 to C_3 when Ver II is selected. A pattern of C_2 to C_0 is determined by the KI/O pin that is connected with the CCS pin; code a ROM pattern by setting 0 according to the thus determined C_2 to C_0 pattern. When Ver II is selected, ROM3 provides two pattern options which can be selected by connecting or not connecting an external pull-up resistor to KI/O_6. For μPD6120C, set ROM3-1 and ROM3-3 to all zeros because they cannot be used. This setting cannot be omitted.

How to Order Mask ROM

Use PROM in ordering custom code mask ROM.

- Medium for ordering: PROM
  (μPD2716, μPD2732A, μPD2764, μPD27128, μPD27256, and their equivalents)
- Quantity: 3
- Data writing:
  ① The selection of Ver I or Ver II is written to address 0 on PROM.
  ② The ROM1 data is written to address 1 on PROM.
  ③ The ROM2 data is written to address 2 on PROM.
  ④ The ROM3 data is written to addresses 3 to 6 on PROM.

		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
Ver I or Ver II SEL		0	0	0	0	0	0		
ROM1									
ROM2									
ROM3	0						0	0	0
	1						0	0	0
	2						0	0	0
	3						0	0	0

Hex code

C_7 to C_4	C_3 to C_0
0	

PROM

Write data		PROM address
0		0
		1
		2
		3
		4
		5
		6

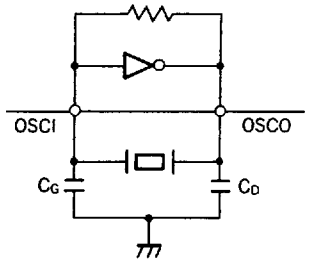
Note: • When Ver I is selected, the ROM1 and ROM2 data are written to addresses 1 and 2 on PROM respectively. 00H is written to addresses 3 to 6 on PROM as the ROM3 data.
• When Ver II is selected, the ROM2 and ROM3 data are written to address 2 and addresses 3 to 6 on PROM respectively. 00H is written to address 1 on PROM as the ROM1 data.

The oscillation circuit of the μPD6120C is designed on the assumption that a 400 to 500 kHz ceramic oscillator will be used. The interaction between the dispersion of ICs and that of ceramic oscillators may cause abnormal oscillations.

The table below gives recommended C_G and C_D values when the μPD6120C is used. These recommended values are obtained from ceramic oscillator manufacturers.

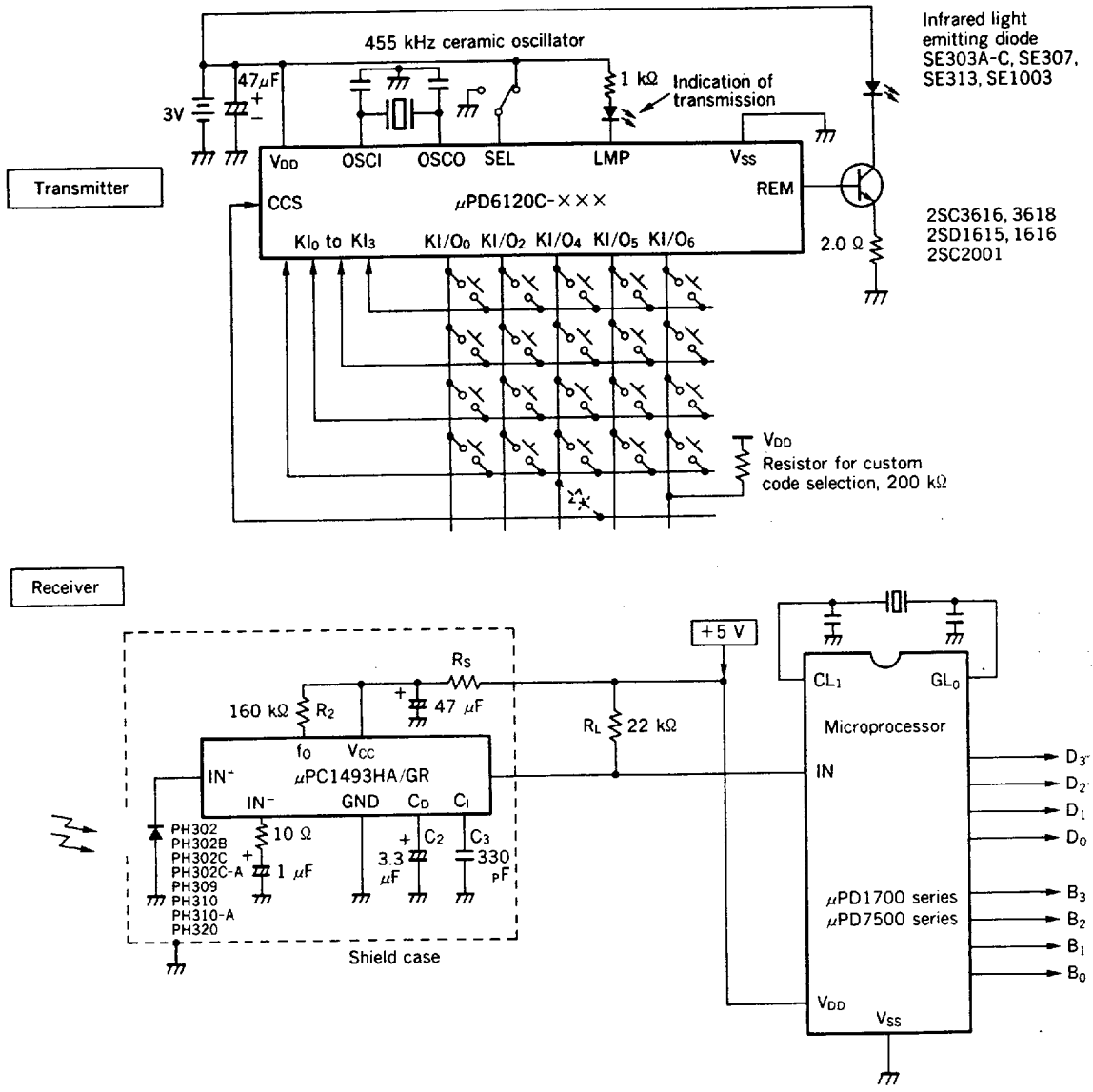
Recommended Capacitor Value (C_G, C_D)

	Designation	C_G	C_D
Kyocera Corp.	KBR-455BTLR	220 pF	220 pF
Murata Mfg. Co., Ltd.	CSB455E	220 pF	220 pF
Toko, Inc.	CRK455	120 pF	300 pF



Example of Application Circuit

This example circuit uses a 4-bit microcomputer chip as a receiver. The microcomputer can be used to perform other processes without having to be used exclusively for reception.



The application circuit and circuit constant, given as an example, are not applicable to mass production designs, taking into consideration deviations and the temperature characteristics of the components. NEC does not assume responsibility for any patent infringements in relation to the example application circuit.

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	$V_{DD} - V_{SS}$	6.0	V
Input Voltage	$V_{IN} - V_{SS}$	−0.3 to V_{DD}	V
Allowable Package Loss	P_D	250	mW
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

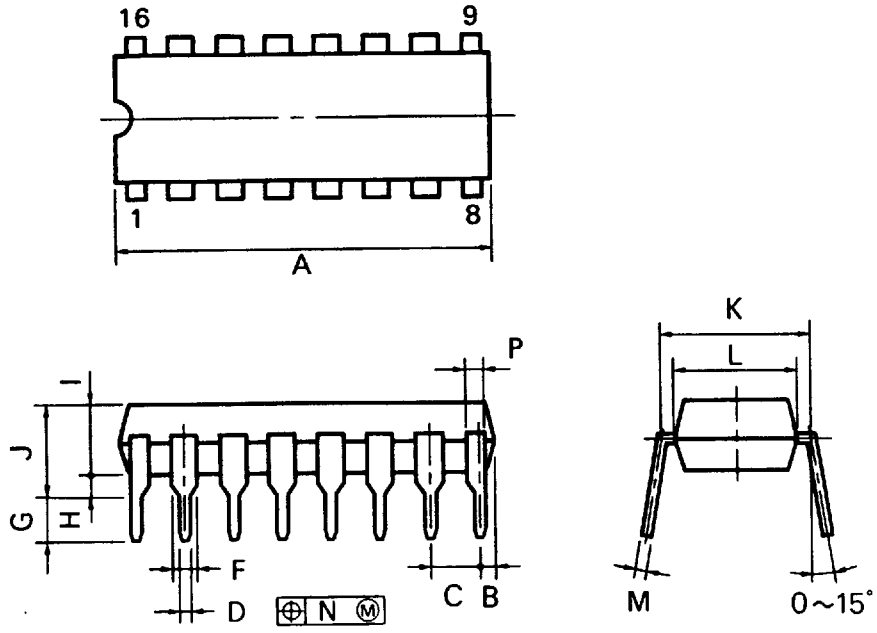
RECOMMENDED OPERATION RANGE

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	2.0	3.0	3.3	V
Oscillation Frequency	f_{osc}	400	455	500	kHz
Input Voltage	V_{IN}	0		V_{DD}	V
Pull-up Resistor for Custom Code Selection	R_{up}	160	200	240	kΩ

ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_{DD} = 3.0 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Operating Voltage Range	V_{DD}	2.0	3.0	3.3	V	
Current Consumption 1	I_{DD1}		0.1	1	mA	f_{osc} = 455 kHz
Current Consumption 2	I_{DD2}			1	μA	f_{osc} = STOP
REM OUT High Level Output Current	I_{OH1}	−5	−8		mA	V_O = 1.5 V
REM OUT Low Level Output Current	I_{OL1}	15	30		μA	V_O = 0.3 V
LMP High Level Output Current	I_{OH2}	−15	−30		μA	V_O = 2.7 V
LMP Low Level Output Current	I_{OL2}	1	1.5		mA	V_O = 0.3 V
KI High Level Input Current	I_{IH1}	10		30	μA	V_{IN} = 3.0 V
KI Low Level Input Current	I_{IL1}			−0.2	μA	V_{IN} = 0 V
KI High Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	
KI Low Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	
KI/O High Level Input Voltage	V_{IH2}	1.3			V	
KI/O Low Level Input Voltage	V_{IL2}			0.4	V	
KI/O High Level Input Current	I_{IH2}	2		7	μA	V_{IN} = 3.0 V
KI/O Low Level Input Current	I_{IL2}			−0.2	μA	V_{IN} = 0 V
KI/O High Level Output Current	I_{OH3}	1.0		2.5	mA	V_O = 2.5 V
KI/O Low Level Output Current	I_{OL3}	35		100	μA	V_O = 1.7 V
CCS High Level Input Voltage	V_{IH3}	1.1			V	
CCS High Level Input Current	I_{IH3}			0.2	μA	Pull Up V_{IN} = 3.0 V
CCS Low Level Input Current	I_{IL3}	−3		−8	μA	Pull Up V_{IN} = 0 V
CCS High Level Input Current	I_{IH4}	10		30	μA	Pull Down V_{IN} = 3.0 V
CCS Low Level Input Current	I_{IL4}			−0.2	μA	Pull Down V_{IN} = 0 V

16PIN PLASTIC DIP (300 mil)



P16C-100-300B

NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	20.32 MAX.	0.800 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.1 MIN.	0.043 MIN.
G	$3.5^{\pm 0.3}$	$0.138^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	1.1 MIN.	0.043 MIN.

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see talbe below) must be met when soldering this product. Please consuit with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF THROUGH HOLE MOUNT DEVICE
μPD6120

Soldering Process	Soldering Conditions
Wave Soldering	Solder temperature : 260 °C or below, Flow time : 10 seconds or below