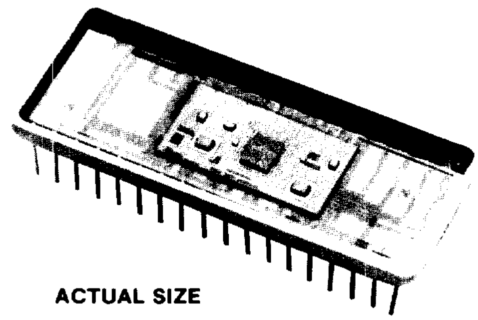
NATEL
HDSC2026

Four-Quadrant Multiplying SIN/COS DAC Microprocessor Compatible 16-bit Hybrid

Features

- **Single 36-pin hybrid DDIP package**
- **1 arc-minute accuracy**
- **0.03% radius accuracy**
- **Microprocessor compatible** (8 and 16-bit)
- **Double buffered inputs**
- **Pin-programmable gain** (0.5, 1.0, 2.0)
- **Buffered reference input**
- **dc-coupled reference and outputs**
- **Requires only ± 15-V power supplies**
- **TTL and CMOS compatible**
- **MIL-STD-883 Processing is Available**
- **Priced at $245/USA single unit price** (HDSC 2026-14S)



ACTUAL SIZE

HDSC2026

Applications

Rotating PPI sweep
Axis rotation
Vector resolution
Resolver computing circuits
Digital-to-resolver (synchro) converter
Low frequency oscillator
Radar and navigational systems
Flight instrumentation

Description

Offering both 8- and 16-bit microprocessor compatibility, the HDSC2026 is a versatile 4-quadrant multiplying digital-to-sin/cos converter. The converter accepts a digital input of 16-bits (CMOS/TTL) and multiplies it by an analog voltage to generate the trigonometric functions $V_{IN} \bullet \sin\theta$ and $V_{IN} \bullet \cos\theta$. V_{IN} is the analog input voltage and θ is the digital input angle. The analog input voltage can be an ac or dc reference with an amplitude of ± 10 V peak. The analog input is buffered through an operational amplifier to minimize loading of the input signal. In addition, the converter is pin-programmable for gains of 0.5, 1.0 and 2.0.

Angular accuracy of 1 arc-minute and radius accuracy of 0.03% make HDSC2026 an ideal choice for applications requiring small size and true sine and cosine outputs. Certain closed-loop systems, resolver computing chains, coordinate transformation and PPI (sweep) displays are examples of such applications.

Packaged in a standard 36-pin DDIP, the converter does not require a +5-V logic supply. The digital inputs are TTL and 5-V CMOS compatible, Internally derived logic thresholds are 0.8 V-dc for a logic "low" and 2.4 V-dc for a logic "high."

All data bits (B1 through B16) are actively pulled down to ground. If the converter requires less than 16-bit resolution, the unused data bit pins may be left unconnected. Control Signals LBD, HBE and LDC are actively pulled-up to logic "high." When not required by your application, these pins may also be left open.

Although designed to interface with most microprocessors, the HDSC2026 may be used in conventional applications without any external components or additional connections.

Model HDSC2026 converters are available with angular accuracies of 1, 2 and 4 arc-minutes. These accuracies are guaranteed over the specified operating temperature range. The exceptionally high accuracy of these converters is achieved by a unique design approach that uses buffer amplifier circuits to eliminate the effects of analog switch resistance instead of requiring special compensation circuits.

Matched thin-film resistors are used to scale the reference input as well as the sine and cosine outputs to assure excellent performance over the entire operating temperature range. All gain resistors are actively laser trimmed to achieve precise performance.

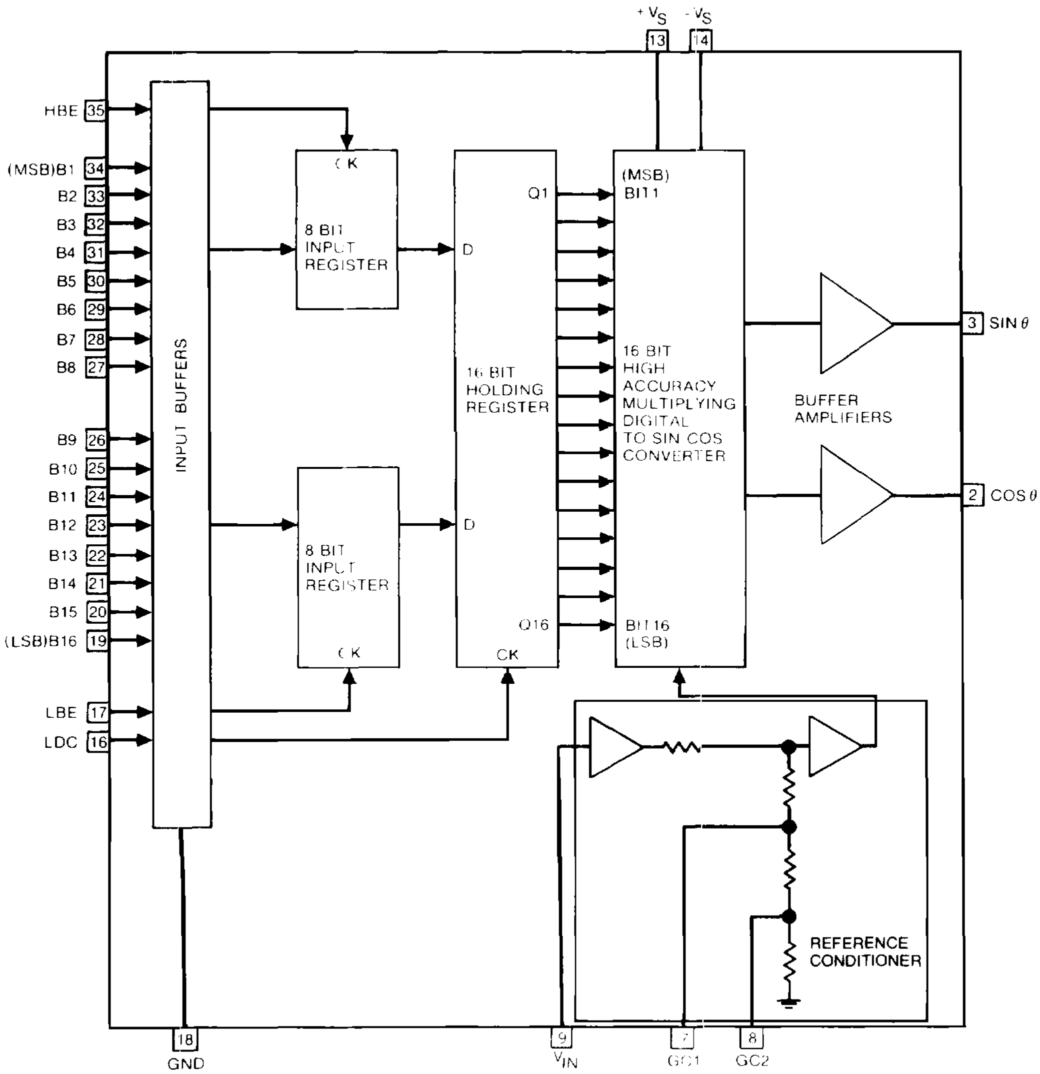


FIGURE 1 2026 Block Diagram

The operation of the Model 2026 is illustrated in the functional diagram of figure 1. The reference voltage is buffered through an operational amplifier in the reference conditioner. In addition the reference conditioner allows the user to program the gain of the converter by appropriate pin connections (see Gain Programming). The digital word representing the input angle is applied to input buffers. Two input registers accept 16-bits from the microprocessor. In conjunction with an 8-bit data bus, each input register can be independently enabled to accept the 16-bit word in two 8-bit bytes. When interfacing with 16-bit bus, both input registers are enabled simultaneously to accept a 16-bit parallel input word. The 16-bit data word is then parallel-loaded into a holding register and processed through a Multiplying Digital-to-Sin/Cos converter.

The multiplying digital-to-sin/cos converter is made up of two function generators (sin θ and cos θ) and quadrant select network. The digital input code is natural binary angle. The two most significant bits (Bit 1 = 180°, Bit 2 = 90°) determine the quadrant information. Bits 3 through 16, containing angular information together with buffered reference voltage, are applied to two function generators. The operation of the function generators is very similar to a 4-quadrant multiplying DAC. Like a conventional DAC, the 2026 uses resistive ladder networks and solid state switching to control the attenuation of the reference voltage. The ladder networks, however, are designed to attenuate the input reference proportional to the sine and cosine of the digital input angle. A unique approach is used in the design of ladder networks to obtain high accuracy in the sine and cosine generation so that they can be used as independently accurate functions. The outputs of function generators are then applied to a quadrant select network to obtain true sin θ and cos θ outputs.

Specifications

PARAMETER	VALUE	REMARKS
Digital Angular Resolution	16 bits (0.33 arc-minutes)	MSB = 180° LSB = 0.0055°
Accuracy	±4 arc-minutes (option S) ±2 arc-minutes (option H) ±1 arc-minutes (option V)	Accuracy applies over operating temp. range
Analog Input (V_{IN})	0 to ±10 V peak ac or dc	
Frequency Range Input Impedance	dc to 1000 Hz (option 4) dc to 10 kHz (option 5) 5 MΩ minimum	 Operational amplifier Buffer
Analog Outputs	$K \cdot V_{IN} \cdot \sin\theta$ and $K \cdot V_{IN} \cdot \cos\theta$	± 10 V peak ac or dc
Converter Gain (K) Radius accuracy Output current Output impedance Zero offset (dc) Offset drift	0.5 ± 0.05% 1.0 ± 0.05% 2.0 ± 0.05% ± 0.03% 2 mA-rms < 1 ohm ± 10 mV typical, ± 25 mV maximum 25 μV/°C	Pin 7 connected to GND, Pin 8 no connection Pin 8 connected to GND, Pin 7 no connection Pin 7 and Pin 8 unterminated Simultaneous amplitude variation in both outputs as a function of digital angle Short circuit proof Operational amplifier output
Output Settling time	20 μsec maximum to accuracy of the converter	For any analog or digital step change
Digital Inputs **Logic Voltage Levels**		CMOS transient protected
Logic "0" Logic "1"	−0.3 V-dc to 0.8 V-dc +2.4 V-dc to +5.5 V-dc	Does not need external logic voltage 0.1 TTL load
Input Currents		
Data Bits (B1-B16)	15 μA typical, "active" pull down to Ground (GND)	For less than 16-bits input, unused pins can be left unconnected
HBE, LBE, LDC	−15 μA typical, "active" pull up to internal logic supply	When not used pins can be left unconnected
Register Controls		
HBE	Logic "1" Logic "0"	8 MSBs enter high byte input register High byte register remains unaffected
LBE	Logic "1" Logic "0"	8 LSBs enter low byte input register Low byte register remains unaffected
LDC	Logic "1" Logic "0"	Data from input registers transferred to holding register Data in holding register remains unaffected
Pulse Width	600 nsec minimum	For guaranteed data transfer
Data Set-up time	200 nsec minimum	Before data transfer
Data Hold time	200 nsec minimum	Before input data changes
Power Supplies		
Supply voltages (±V_S) Supply Currents Supply Rejection	±15 V-dc ± 10% ±20 mA maximum 80 dB typical	For ±10 V peak output
Physical Characteristics		
Type Size Weight	36 PIN Double DIP 0.78 x 1.9 x 0.21 inch (20 x 48 x 5.3 mm) 0.6 oz (17 g) max	3 standoffs are added to the package to insulate it from printed circuit board traces. (Standoffs included in 0.21-inch height dimension)

Absolute Maximum Ratings

Reference Input .... -V_S to +V_S
Power Supply Voltages (±V_S) .... ±18 V-dc
Digital Inputs .... −0.3 V-dc to +6.5 V-dc
Storage Temperature .... -65°C to +135°C

Although Digital inputs are CMOS protected, storage in conductive foam is recommended.

When installing on or removing the converter from printed circuit boards or sockets, it is recommended that the power supply be turned off. Decoupling capacitors are recommended on the +V_S and -V_S supplies. A 1 μF tantalum capacitor in parallel with 0.01 μF ceramic capacitor should be mounted as close to the supply pins as possible.

Pin Designations

GND	Power Supply Ground Digital Ground Analog Signal Ground
B1 - B16	Parallel Data Input Bits B1 is MSB = 180 degrees B16 is LSB = 0.0055 degree
HBE	High Byte Enable - Data inputs B1 through B8 enter the input buffer register when HBE is set to a Logic "High." When HBE is set to Logic "Low" the input register is in the hold mode and is not affected by digital activity at the input data bits B1-B8 pins.
LBE	Low Byte Enable - Data inputs B9 through B16 enter the input buffer register when LBE is set to Logic "High." When LBE is set to Logic "Low" the input register is in the hold mode and is not affected by digital activity at the input data bits B9-B16 pins.
LDC	Load Converter - When LDC is set to a Logic "High," the converter will transfer the contents of the input buffer registers to the 16-bit holding register. When LDC is set to Logic "Low," the converter is in the hold mode and is not affected by digital activity in the input registers.

Note: For continuous updating HBE, LBE and LDC may be left open. Internal active pull-up will force these functions to a Logic "High"

$+V_S$, $-V_S$	Supply Voltages - Typically ±15 V-dc

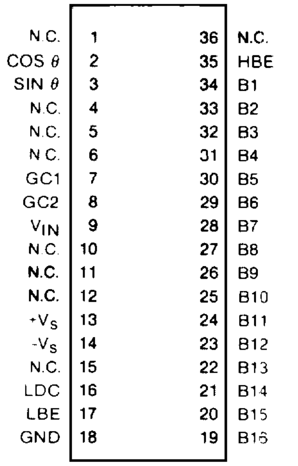


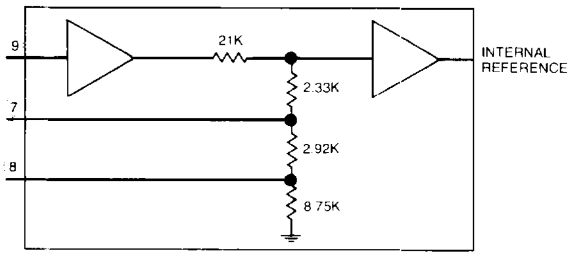
Fig. 2 HDSC2026 Pin Assignments

V_{IN}	Reference Voltage Input
GC1, GC2	Gain programming pins (see text for connections)
SIN θ, COS θ	Output Analog Signals

Caution: Reversal of $+V_S$ and $-V_S$ power supply connections will result in permanent damage to the converter.

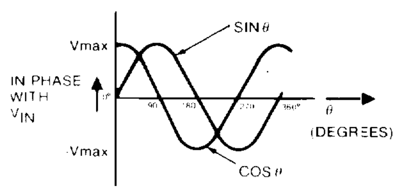
Analog Output Gain Control and Phasing

An equivalent circuit for gain control is shown in figure 3. When both gain-control pins 7 and 8 are left unconnected (OPEN), the gain of the converter is 2.0 (i.e., output analog signals are 2 x V_{IN} Sin θ and 2 x V_{IN} Cos θ). When pin 8 is connected to GND and pin 7 is left unconnected the converter gain is 1.0. When pin 7 is connected to GND and pin 8 is left unconnected the converter gain is 0.5. The accuracy of the gain resistors is 0.05%. As can be seen from the equivalent circuit, the gain of the converter can be modified by adding a resistor between pin 7 or 8 and GND. Users, however, are cautioned against using a large value resitor as the temperature coefficient of the external resistor will not be matched with TCR of internal resistor. Contact a Natel Applications Engineer, if your application requires different gain.



GC1 (PIN 7)	GC2 (PIN 8)	GAIN (K)
GND	OPEN	0.5
OPEN	GND	1.0
OPEN	OPEN	2.0

FIGURE 3 Reference Conditioner



SIN OUTPUT = K • V_{IN} • (1 + n) SIN θ
COS OUTPUT = K • V_{IN} • (1 + n) COS θ
K IS THE GAIN OF THE CONVERTER
AND n IS THE SCALE FACTOR VARIATION AS A FUNCTION OF DIGITAL ANGLE (±0.03%)

FIGURE 4 Output Phasing

Figure 4 shows the output phasing and gives mathematical relationship between reference voltage V_{IN} and output analog signals as function of digital angle θ and converter gain K.

Digital Interface

The double buffered input registers of the HDSC2026 offer the user an easily implemented interface with 8- or 16-bit microprocessor data buses. For applications not involving a microprocessor, independently controlled 8-bit latching registers give the user the flexibility of designing his own interface system. Provision has also been made for asynchronous data inputs through the use of the LDC control function. Asynchronous data inputs up to 16 bits can be accommodated.

Continuous Operation

Asynchronous converter operation, without timing controls, is shown in figure 5. Inputs LBE; HBE and LDC have internal pull-up circuitry, permitting these pins to be left open. The parallel information at the data inputs B1-B16 is continuously converted to sinθ and cosθ at the analog outputs. For applications requiring less than 16-bit resolution, unused pins can be left open. Internal pull-down circuitry applies a logic "0" to unconnected data inputs B1-B16.

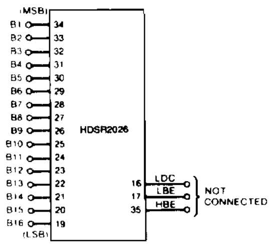


FIGURE 5 Digital Connection for Continuous Operation

Two-Byte Loading

The circuit configuration for two-byte loading of angular data from a data bus is shown in figure 6. As shown in figure 7 timing diagram, the 8 LSBs (B9-B16) are transferred to the low-byte input register when LBE is a logic "1". LBE can be "High" when data bits are changing, but must remain "High" for a minimum of 800 nsec after the data is stable. Data should be held for 200 nsec (data hold time) after LBE goes "Low." Bits B1-B8 are transferred to the high-byte input register when HBE is a logic "1." The timing requirements are the same as those for LBE. Data are transferred from the two input registers to the holding register when LDC (load converter) is at logic "1." If LDC is at logic "0", the contents of the holding register are latched and remain at their previous values unaffected by changes at the data inputs or input registers.

Note that LBE,HBE and LDC are level-actuated functions.

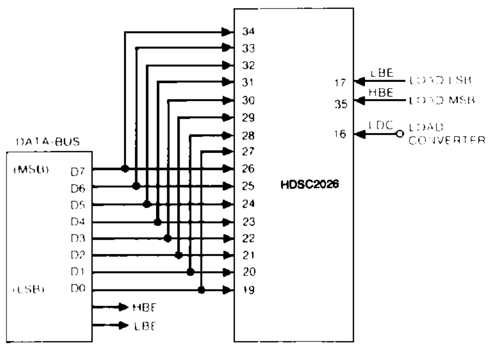


FIGURE 6 Digital Connections for Two-Byte Loading

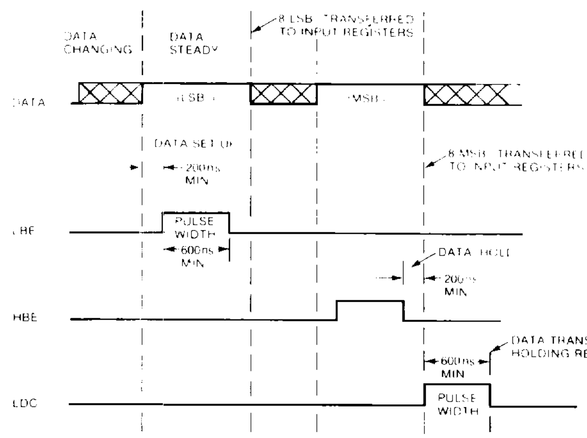


FIGURE 7 Two-Byte Loading

Single Byte Loading

Single 16-bit byte loading is illustrated in figure 8. As shown in the timing diagram (figure 9), 200 nsec after the data is stable, the input angular information is transferred to the holding register when LDC is at a logic "1." LDC is a level-actuated function and must remain high for the times specified in the timing diagram.

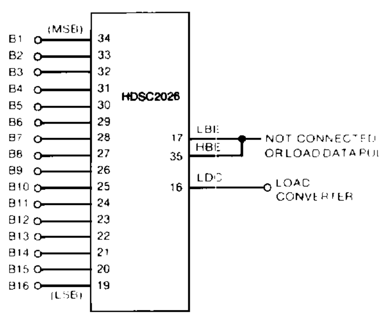


FIGURE 8 Digital Connections for One Byte (16 bits) Loading

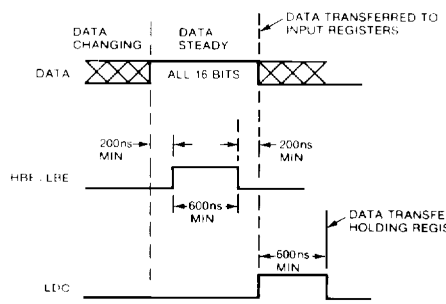


FIGURE 9 Single-Byte Loading

Burn-in Circuit

As a standard practice, all Natel hybrid synchro converters go through a power burn-in for 168 hours at maximum operating temperature. A typical burn-in circuit for digital-to-sine/cosine converter Model HDSC 2026 is shown in figure 10.

The data bits B1-B16 are continuously exercised through a 16-bit counter and a square-wave oscillator.

The enable controls, LBE and HBE, and load converter control LDC are randomly connected to GND or left open.

The reference voltage is applied by an ac source.

The gain controls GC1 and GC2 may be left open or connected to ground. The analog outputs SIN θ and COS θ are connected to passive loads of 2mA each. Test points TP1-TP6 are left unconnected.

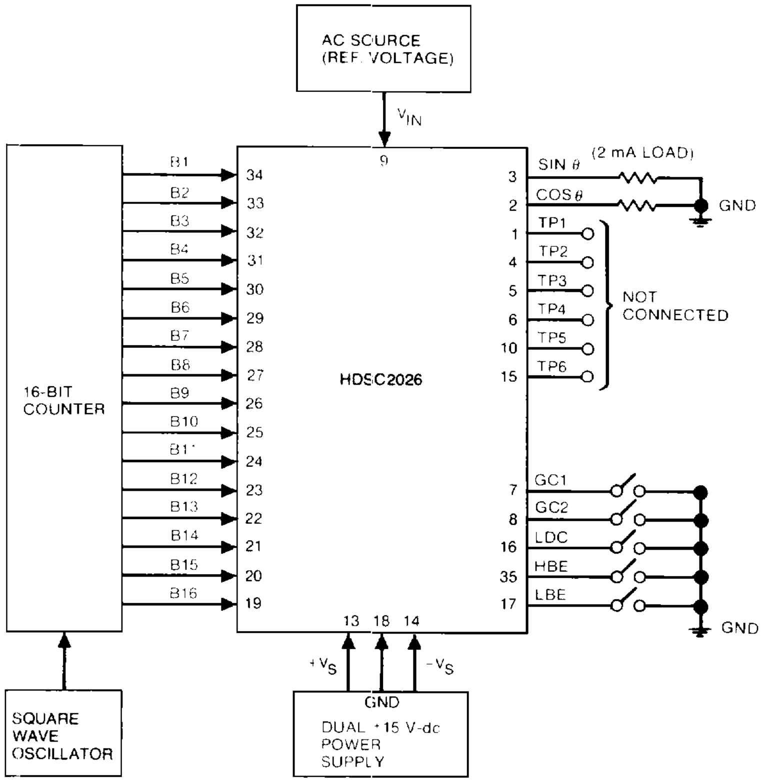


FIGURE 10 Burn-in Circuit for HDSC 2026

Applications using HDSC2026

DIGITAL TO RESOLVER/SYNCHRO CONVERTERS

Figures 11 and 12 show simple schematics for digital-to-resolver and digital-to-synchro converters. Model HDSC2026 allows the flexibility of keeping all conversions near the digital data and control signals. Power amplifiers and transformers may be mounted at a more thermally optimal location on the system chassis, thereby physically isolating heat dissipating circuits from high accuracy computing circuits. Reference input is buffered through an operational amplifier and analog outputs are operational amplifier outputs. Therefore effects of cable lengths are minimized.

Power amplifiers for D/S and D/R converter applications requiring moderate performance are easily designed from power OPAMPS such as Fairchild's μA791 and μA759. The sophistication of the modern integrated power amplifier gives the designer short-circuit protection and thermal shutdown with no increase in circuit complexity. For high power and/or high accuracy applications, more complex design procedures are required. Consult Natel for special requirements.

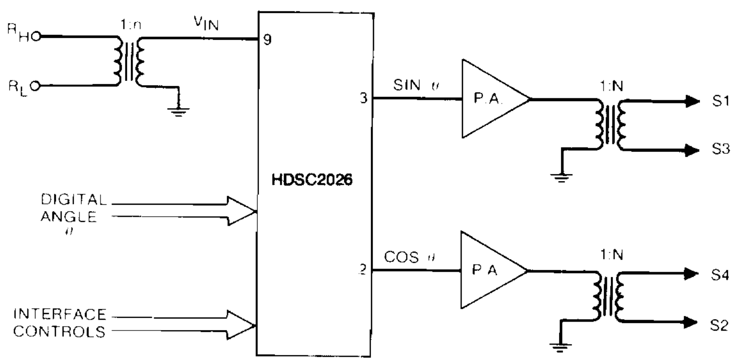


FIGURE 11 Digital-to-Resolver Converter

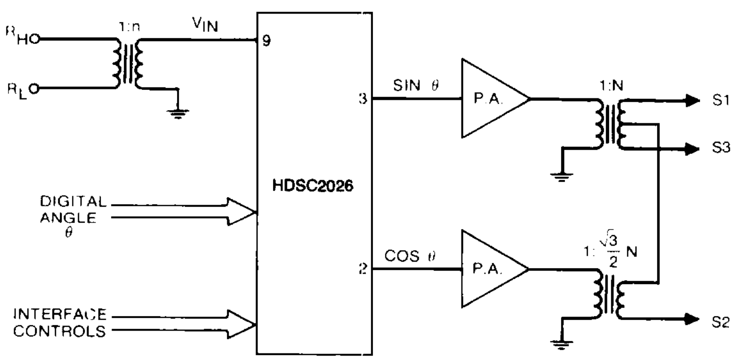
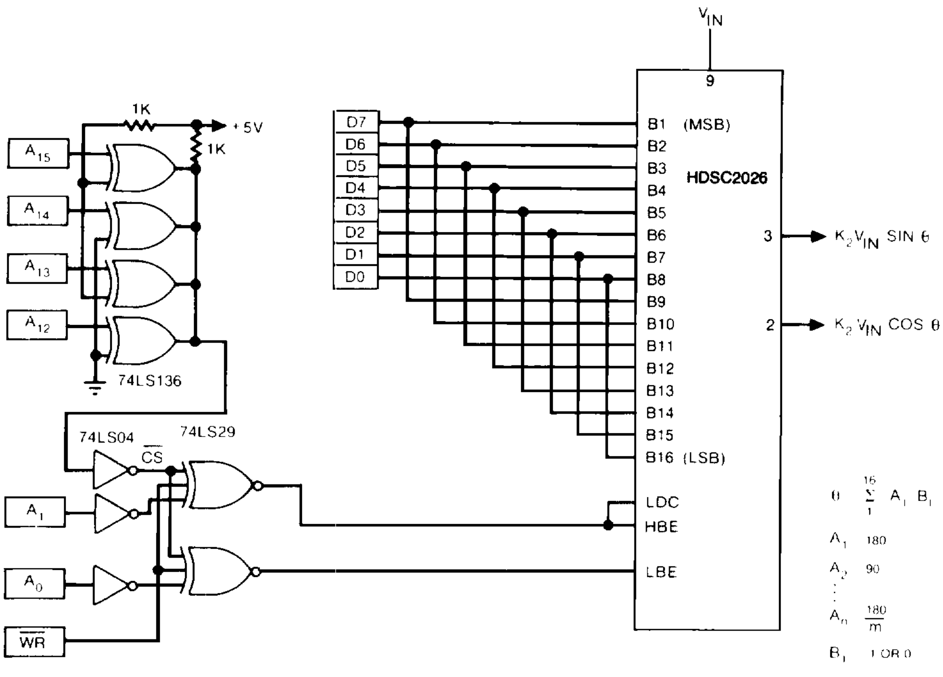


FIGURE 12 Digital-to-Synchro Converter

Memory Mapped I/O With 8080 Microprocessor



REGISTER ASSIGNMENT (SHLD INSTRUCTION)
H : HIGH BYTE (B1 THRU B8)
L : LOW BYTE (B9 THRU B16)
LOW BYTE ADDRESS 5XX1H
HIGH BYTE ADDRESS 5XX2H
NOTE ADDRESSES 5003H THROUGH 5FFFH ARE NOT AVAILABLE UNLESS EXTRA DECODERS (74LS136) ARE INCLUDED

FIGURE 13 8080μP-HDSC2026 Memory Mapped Interface Connection Diagram

A typical example of a microprocessor interface using memory mapping and an 8080-type 8-bit μP is shown in figure 13. Memory-mapped I/O enables the HDSC2026 to receive data from the μP using the same instructions that are required to transfer data to and from memory locations. This means that, in addition to the accumulator, any of the internal registers can be used to transfer data to the converter. This is a particularly attractive feature, since the use of the SHLD instruction permits transfer of a 16-bit output to the HDSC2026 with a single instruction.

As is shown in figure 13, the control signals necessary to operate the converter are provided by the external gating structure. The CS signal (Chip Select) is generated by decoding the address bus with the 74LS136 exclusive-or gates, hard-wired to the selected address. In the example, only the upper 4 address lines are decoded. When the address 5XXXH is decoded, CS goes low enabling the 74LS29 control gates. When the selected address is 5XX1H and the $\overline{WR}$ line goes low, D0-D7 are transferred to the low-byte input register. When $\overline{WR}$ returns to high, LBE goes low, latching the data. Using the SHLD instruction, the next processor cycle will increment the address to 5XX2H and output the next byte of data. When $\overline{WR}$ again goes low, HBE and LDC go high, transferring both data bytes to the converter's 16-bit holding register, at which time the conversion takes place. The data format for loading the H and L registers is shown below:

H Registers -- High Byte

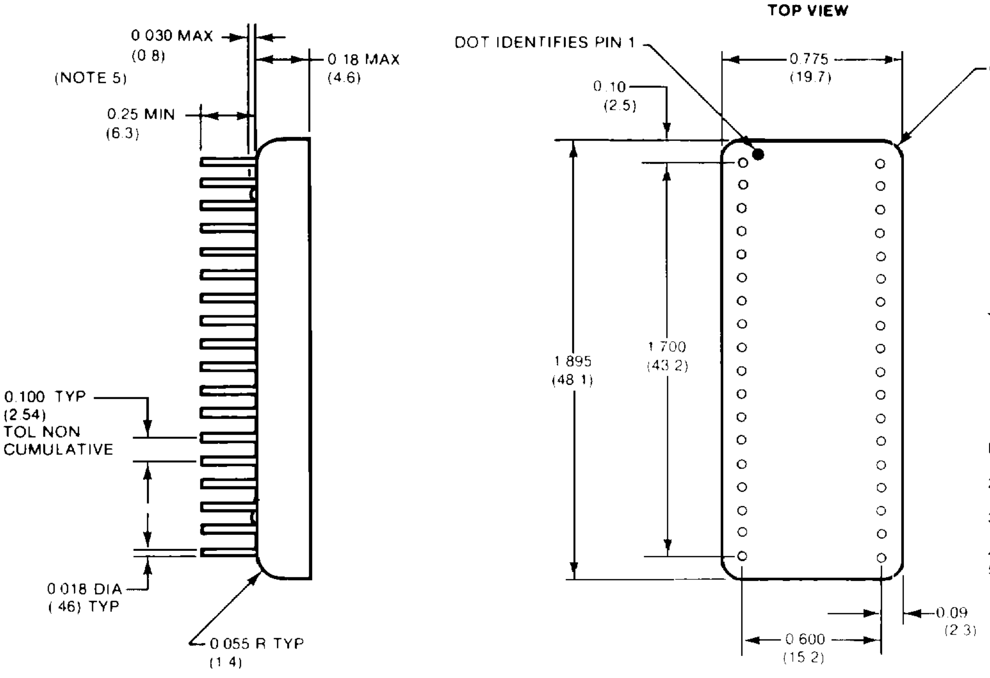
B1	B2	B3	B4	B5	B6	B7	B8
D7	D6	D5	D4	D3	D2	D1	D0
(MSB)							

L Registers -- Low Byte

B9	B10	B11	B12	B13	B14	B15	B16
D7	D6	D5	D4	D3	D2	D1	D0
							(LSB)

Other Synchro Conversion products available from NATEL

- Two-speed logic combiner with 20-bit, 3-state output, in a 1.3 x 2.6 x .35 inch size (TSL1x36)
- 14 and 16-bit Digital to Synchro/Resolver converters, with internal power amplifiers (5012, 5112, 5116)
- High power Synchro/Resolver Drivers
- 10 to 20-bit single-speed Synchro-to-Digital converters
- Hybrid synchro converters -- see page 8
- Low profile Digital-to-Synchro/Resolver converters
- Two-speed Synchro (Resolver)-to-Digital converters with 16 and 20-bit resolutions in a single package. (Models 2SD402 and 2SD412).
- Solid State control transformers (SSCT) and differential transmitters (SCDX).
- Angle position indicators and synchro instrumentation for one-speed and multi-speed applications.



TOLERANCES:

XX ± 01 (± 25)

XXX ± 005 (± 13)

NOTES:

1 CASE IS ELECTRICALLY FLOATING
2 PINS ARE KOVAR WITH GOLD PLATING (50μINCH MIN)
3 PACKAGE IS KOVAR WITH ELECTROLESS NICKEL PLATING
4 DIMENSIONS SHOWN IN INCHES AND (MM)
5 STANDOFFS (3) CERAMIC OR GLASS

MECHANICAL OUTLINE (36 PIN DOUBLE DIP)

Ordering Information

HDSC2026 - T F A

Temperature Range	Accuracy
1 = 0°C to +70°C	S = ±4 arc-minutes
2 = -25°C to +85°C	H = ±2 arc-minutes
3 = -55°C to +125°C	V = ±1 arc-minute

Frequency Range
4 = dc to 1000 Hz
5 = dc to 10 kHz

MIL-STD-883 COMPLIANT HYBRIDS AVAILABLE
Contact Natel Engineering for Delivery

A wide range of applications assistance is available from Natel. Application Notes can be requested when available . . . and Natel's applications engineers are at your disposal for specific problems.

Other Hybrid products in 36 pin DDIP size:

- 16-bit microprocessor-compatible synchro/resolver-to-digital converter, with 3 state output, operating from a single +5-V power supply (HSRD1006)
- 16-bit microprocessor-compatible digital to synchro/resolver converter with double buffered inputs and 1 arc-minute accuracy (HDSR2006).
- 14-bit synchro(resolver)-to-digital converters pin-compatible with existing designs, but with superior performance (HSD/HRD1014)
- 10-bit synchro (resolver)-to-digital converters that are pin compatible with existing designs (HSD/HRD1510)
- 14/16-bit synchro (resolver) control transformer with 1 arc minute accuracy (HSCT/HRCT3006)
- 14-bit Digital-to-Synchro/Resolver converter that is pin-compatible with existing designs, with transformation and angular accuracy improvement of a factor of 2 to 4 (HDSR2504).

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