Signetics

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Status	Product Specification
FAST Products	

FAST 74F323
Register

8-Bit Universal Shift/Storage Register With Synchronous Reset and Common I/O pins (3-State)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F323	115 MHz	55mA

FEATURES

- **Common parallel I/O for reduced pin count**
- **Additional serial inputs and outputs for expansion**
- **Four operating modes: Shift left, shift right, load and store**
- **3-state outputs for bus oriented applications**

DESCRIPTION

The 74F323 is an 8-bit universal shift /storage register with 3-state outputs. Its function is similar to the 74F299 with the exception of synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin counts. Separate serial inputs and outputs are provided for flip-flops Q_0 and Q_7 to allow easy serial cascading. Four modes of operation are possible: Hold (store), shift left, shift right and parallel load.

The 74F323 contains eight edge-triggered D-type flip-flops and the interstage logic

ORDERING INFORMATION

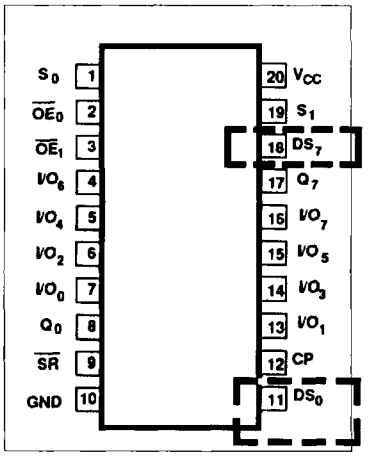
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F323N
20-Pin Plastic SOL	N74F323D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

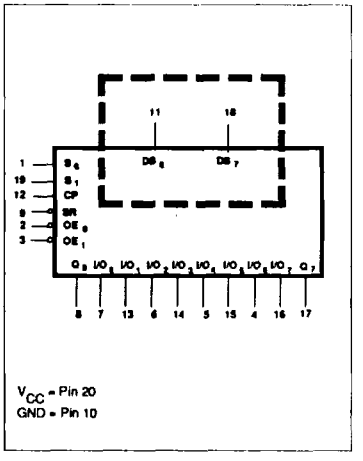
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
DS_0	Serial data input for right shift	1.0/1.0	20µA/0.6mA
DS_7	Serial data input for left shift	1.0/1.0	20µA/0.6mA
S_0, S_1	Mode select inputs	1.0/2.0	20µA/1.2m
CP	Clock Pulse input (Active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{SR}$	Synchronous Reset input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}_0$, $\overline{OE}_1$	Output enable input (active Low)	1.0/1.0	20µA/0.6mA
Q_0, Q_7	Serial outputs	50/33	20µA/20mA
I/O_n	Multiplexed parallel data inputs or	3.5/1.0	70µA/0.6mA
	3-state parallel outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

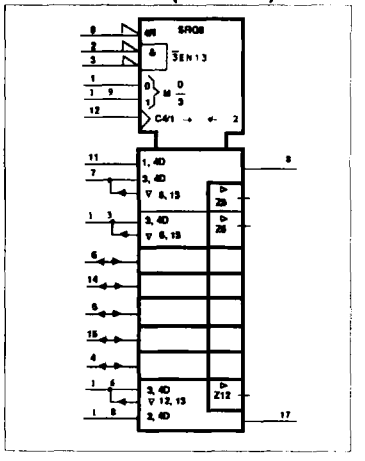
PIN CONFIGURATION



LOGIC SYMBOL

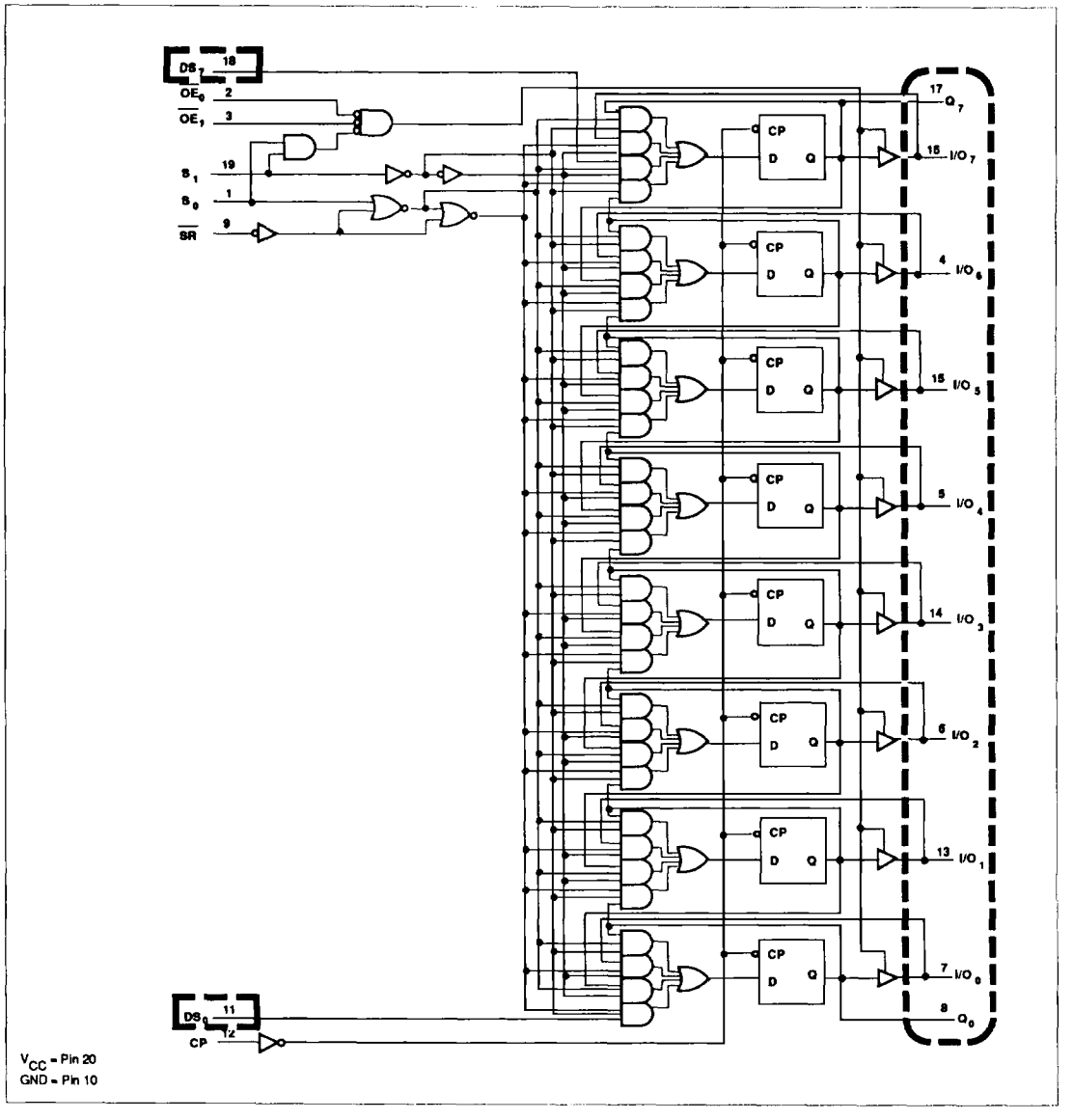


LOGIC SYMBOL(IEEE/IEC)



necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operations is determined by S_0 and S_1, as shown in the Function Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words. A Low signal on $\overline{SR}$ overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of clock. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended set up and hold times, relative to the rising edge of clock are observed. A high signal on either $\overline{OE}_0$ or $\overline{OE}_1$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by High signals on both S_0 and S_1 in preparation for a parallel load operation.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OPERATING MODE
$\overline{OE}_n$	$\overline{SR}$	S_1	S_0	CP	
L	L	X	X	↑	Synchronous Reset; Q_0-Q_7=Low
L	H	H	H	↑	Parallel load ; $I/O_n \rightarrow Q_n$
L	H	L	H	↑	Shift right ; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc
L	H	H	L	↑	Shift left ; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
L	H	L	L	X	Hold
H	X	X	X	X	Outputs disabled (3-state)

H = High voltage level
L = Low voltage level
NC = No change
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	Q_0, Q_7	40	mA
		I/O_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Q_0, Q_7			-1	mA
		I/O_n			-3	mA
I_{OL}	Low-level output current	Q_0, Q_7			20	mA
		I/O_n			24	mA
T_A	Operating free-air temperature range		0		70	°C