SSI 32D4660
Time Base Generator

Advance Information

June, 1990

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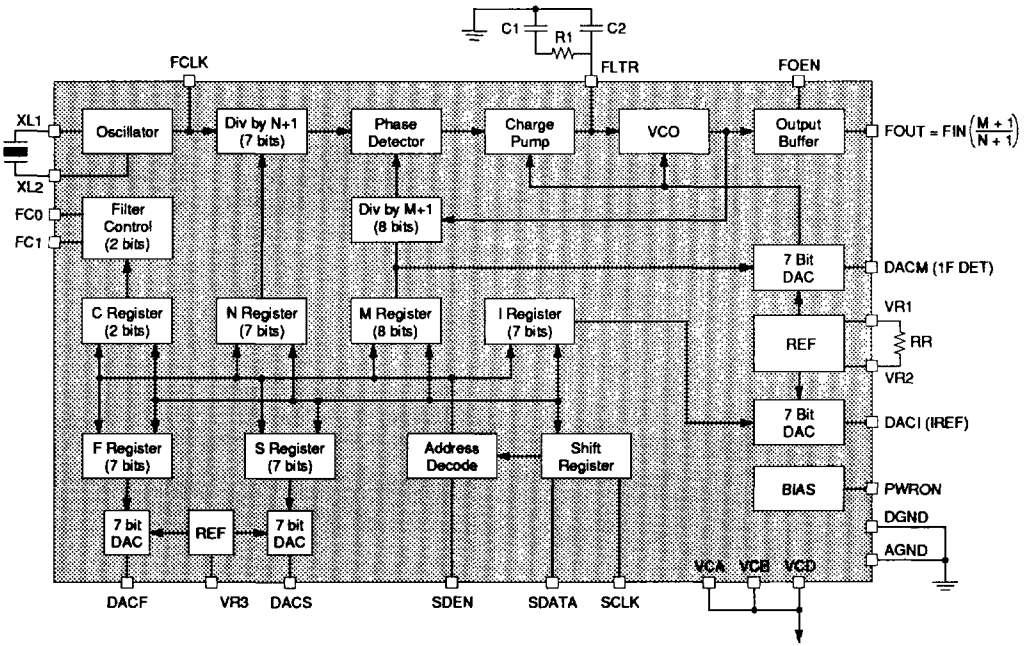
DESCRIPTION

The SSI 32D4660 Time Base Generator provides a programmable reference generator, channel filter control and data rate control for constant density recording applications. It is optimized to operate with the 32D53xx series data separators and contains a high performance programmable PLL for 1% reference frequency control. A 7-bit DAC is provided to program the IREF current which sets the data separator PLL operating center frequency. A 7-bit DAC is provided to program the 1FDET current which sets the timing for the data separator synch field detect. Two additional 7-bit DAC's are provided for programmable electronic filter (slimmer) control. Two latched TTL outputs are provided to control filter multiplexers. A serial microprocessor interface reduces pin count and provides convenient access to the internal program storage registers. The 32D4660 only requires a +5V supply and will be available in 24-pin DIP and SO packages.

FEATURES

- **For constant density recording applications**
- **Reference frequency control**
- **Channel filter control**
- **Internal DAC available to program data separator data rate**
- **Internal DAC available to program data separator sync field detect timing**
- **Up to 24 Mbit/s operation**
- **1% frequency resolution**
- **No external active components required**
- **+5V only operation**
- **Low power mode**
- **24-pin DIP and SOL package**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

PIN DESCRIPTIONS

INPUT PINS

NAME	DESCRIPTION
SDATA	Serial Data. Data input for an 8-bit control shift register. The data packet is transmitted MSB (D7) first. The first four bits are the register address and the last four are its data bits. Registers larger than 4-bits must be loaded with two 8-bit data packets. These packets should be loaded sequentially in less than 10 µs since the loading operation will cause output transients. With proper loop filter design, the output transients will recover within 1 ms. The data packet fields are given in Table 1.
SCLK	Serial Data Clock. Negative edge triggered clock input for the serial data.
SDEN	Serial Data Enable. A high level input enables data loading. The data is latched when the input is low.
PWRON	Power On. A high level input enables the chip. A low level puts the chip in a low power idle state.
FOEN	Frequency Output Enable. A high level input enables the FOUT output. A low level disables the output and minimizes the driven data separator jitter.

OUTPUT PINS

FOUT	Frequency Output. An ECL output with internal current source. The low voltage swing which minimizes data separator jitter must be AC coupled to the data separator XLT1 input. FOUT = [(M +1)/(N +1)]FIN where M = M Register number and N must be set to approximately [(FIN) (256) / 72MHz] - 1
DAC M	DAC Output. 7-bit DAC current sink output used to program timing current to the data separator sync field detect SDS pin. The current magnitude is controlled by the 7 MSB's of the M Register and is compensated to minimize the sensitivity to power supply and temperature variations. If this output isn't required, the pin must be connected to VCC.
DAC I	DAC Output. 7-bit DAC current source output used to program timing current for the data separator VCO center frequency. The current magnitude is controlled by the I Register and is compensated to minimize the sensitivity to power supply and temperature variations.
DAC F	DAC Output. 7-bit DAC voltage output used for electronic filter control. The output voltage is set by the voltage at VR3 and the F Register number.
DAC S	DAC Output. Similar to DAC F except controlled by the S Register number.
FC0	Filter Control 1. TTL output used to control an external filter multiplexer. C0 = H sets FC0 = H.
FC1	Filter Control 2. TTL output used to control an external filter multiplexer. C1 = H sets FC1 = H.

OUTPUT PINS (Continued)

NAME	DESCRIPTION
FCLK	Clock Output. Optional TTL output that may be used for a system clock. The output frequency is the same as the oscillator output frequency. For minimum FOUT jitter, parts with FCLK disabled should be used. FCLK remains active when PWR ON is low.

ANALOG PINS

XTL1, XTL2	Crystal Oscillator Connections. The circuit is designed to be used with an 8 MHz to 20 MHz crystal. If a crystal is not desired, XTL1 may be driven by a TTL source with XTL2 left open.
VR1, VR2	Current Setting Resistor Connections. An external resistor RR connected between VR1 and VR2 sets the DACM and DACI currents.
VR3	Reference Voltage Input. An external 2.2V supply sets the reference for the DACF and DACS currents.
FLTR	PLL Loop Filter Connection. Connection for loop filter components R1, C1 and C2.
DGND, AGND	Digital and Analog Ground
VCA, VCB	Analog +5V Supplies
VCD	Digital +5V Supply

TABLE 1: Data Packet Fields

ADDRESS BITS				USAGE	DATA BITS			
D7	D6	D5	D4		D3	D2	D1	D0
0	1	1	0	I REGISTER	X	I6	I5	I4
0	1	1	1	I REGISTER	I3	I2	I1	I0
1	0	0	0	F, C, REGISTER	C1	F6	F5	F4
1	0	0	1	F REGISTER	F3	F2	F1	F0
1	0	1	0	S, C, REGISTER	C0	S6	S5	S4
1	0	1	1	S REGISTER	S3	S2	S1	S0
1	1	0	0	M REGISTER	M7	M6	M5	M4
1	1	0	1	M REGISTER	M3	M2	M1	M0
1	1	1	0	N REGISTER	X	N6	N5	N4
1	1	1	1	N REGISTER	N1	N2	N1	N0

X = Don't care bit.

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING	UNITS
Storage Temperature	–65 to +150	°C
Junction Operating Temperature, Tj	+150	°C
Supply Voltage, VCA, VCB, VCD	–0.5 to 7	V
Voltage Applied to Logic Inputs	–0.5 to 5.5	V
Maximum Power Dissipation	0.6	mW

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING	UNITS
Supply voltage, VCA = VCB = VCD	4.65<VCC<5.25	V
Junction Temperature, Tj	0<Tj<135	°C
Ambient Temperature, Ta	0<Ta<70	°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified: 4.65V<VCC<5.25, 0°C<Ta<70°C

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIH	High Level Input Voltage		2.0			V
VIL	Low Level Input Voltage				0.8	V
IIH	High Level Input Current	VIH = 2.7V			20	µA
IIL	Low Level Input Current	VIL = 0.4V			–1.5	mA
VOH	High Level Output Voltage	IOH = -400 µA	2.6			V
VOL	Low Level Output Voltage	IOL = 2 mA			0.5	V
VOH	FOUT ECL High Level	VCD = 5V, VOH-VCD	–1.02			V
VOL	FOUT ECL Low Level	VCD = 5V, VOL-VCD			–1.45	V
ICC	Power Supply Current	PWRON = 2.0V		77	103	mA
		PWRON = 0.8V		25		mA
IO	FOUT Output Current			±4		mA
VO	FOUT Output Swing		0.6			V

INPUT/OUTPUT CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
FIN	FIN Frequency		8		20	MHz
FO	FOUT Frequency				75	MHz
JFO	FOUT Jitter	TO = 1/FO; FCLK active			±400	ps(pk)
DFO	FOUT Duty Cycle	50% Amplitude FOUT = 72 MHz	42		58	%
M	M Divide Number		80		255	
N	N Divide Number		25		127	
I	I Register Number		50		127	
RR	External Resistor		4.50		5.25	KΩ
TVCO	VCO Center Frequency Period	1V<FLTR< VCC – 0.5V TO=(6.17 E-10)(RR/M)+2.4 ns VCC = 5V, RR = 4.75K	0.77TO		1.23TO	ns
	VCO Frequency Dynamic Range	1V < FLTR < VCC – 0.5V, VCC = 5V	±25		±45	%
KVCO	VCO Control Gain	Wi = 2π(FO)	0.14Wi		0.26Wi	rad/s V
KD	Phase Detector	KD = (4.16E – 3)/RR	0.83KD		1.17KD	A/rad
IOM	DACM Current	IO = (1.641 E-2) M/RR VCC = 5V, TA = 25°C, RR = 4.75K	0.97IO –1LSB		1.03IO +1LSB	A
IOI	DACI Current	IO = (7.41 E-2)I/RR VCC = 5V, TA = 25°C, RR = 4.75K	0.95IO –3/4LSB		1.05IO +3/4LSB	A
VOF	DACF Voltage	VOF = 0.98 F*VR3/127, VCC = 5V	0.97VOF –3/4LSB +15 mV		1.03VOF +3/4LSB +60 mV	V
VOS	DACS Voltage	VOS = 0.98 S*VR3/127 VCC = 5V	0.97VOS –3/4LSB +15 mV		1.03VOS +3/4LSB +60 mV	V
VR3	DAC Reference		2.0		2.4	V
IVR3	VR3 Input Current	VR3 = 2.4V			0.5	mA

INPUT/OUTPUT CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
VODH	DACM Output Voltage		0.5	VCC	V
VODL	DACI Output Voltage			2	V
VOFL	DACF, DACS Output Voltage		0.1	2.4	V
ROUT	DACF, DACS Output Resistance			3.7	kΩ
SCLK	Data Clock Period, TC		100		ns
TDD	Data Set Up/Hold Time		25		ns
TDE	Data Enable Delay Time	Delay from data clock rising edge	– TC	TC/4	ns

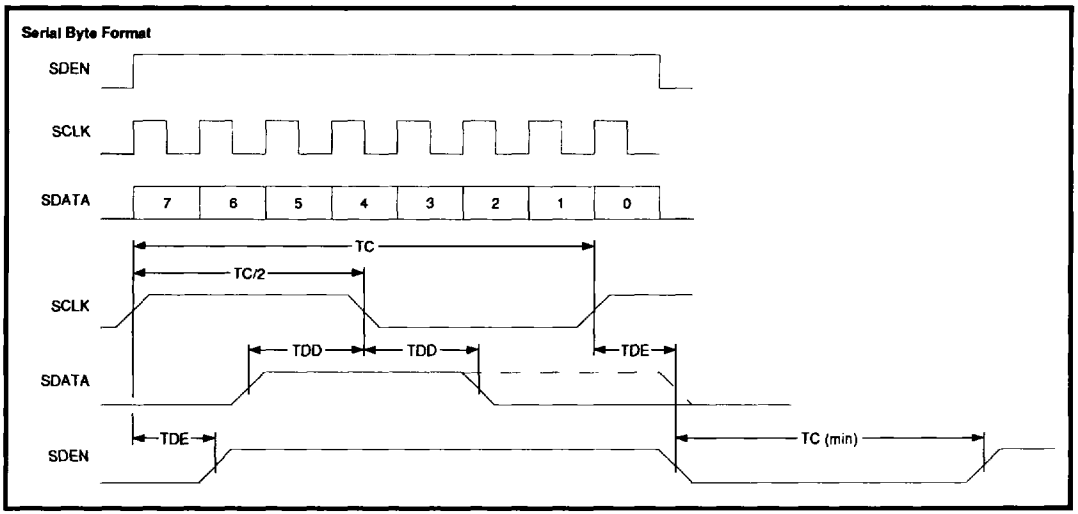
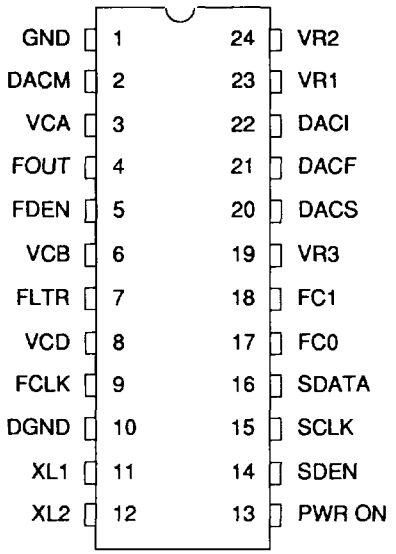


FIGURE 1: Serial Port Timing

PIN DIAGRAM
(Top View)



24 Pin PDIP, SOL

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Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only.

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