Large Air Gap, Vibration-Immune, GMR Transmission Speed and Direction Sensor IC

FEATURES AND BENEFITS

- **GMR technology** integrates high sensitivity MR (magnetoresistive) sensor elements and high precision BiCMOS circuits on a single silicon integrated circuit offering high accuracy, low magnetic field operation
- **Integrated capacitor** in a single overmolded miniature package provides greater EMC robustness
- **SolidSpeed Digital Architecture** supports advanced algorithms, maintaining performance in the presence of extreme system-level disturbances, including vibration immunity capability over the full target pitch
- **Flexible orientation for xMR or Hall** replacement and application installation flexibility
- **ASIL B** rating based on integrated diagnostics and certified safety design process
- **Two-wire current source output** pulse-width protocol supporting speed, direction, and ASIL
- **EEPROM** offers device traceability throughout the production process

PACKAGE:

2-Pin SIP
(suffix UB)

Not to scale

DESCRIPTION

The A19570 is a giant magnetoresistance (GMR) integrated circuit (IC) that provides a user-friendly two-wire solution for applications where speed and direction information is required. The small integrated package includes an integrated capacitor and GMR IC in a single overmolded design with an additional molded lead stabilizing bar for robust shipping and ease of assembly.

The GMR-based IC is designed for use in conjunction with front-biased ring magnet encoders. State-of-the-art GMR technology with industry-leading signal processing algorithms accurately switch in response to low-level differential magnetic signals. The high sensitivity of GMR combined with differential sensing offers inherent rejection of interfering common-mode magnetic fields and valid speed and direction sensing over larger air gaps, commonly required in transmission applications.

Patented GMR technology allows the same IC orientation as other MR technologies or the IC can be rotated for Hall-effect compatibility as a drop-in solution in the application.

Integrated diagnostics are used to detect an IC failure that would impact the output protocol's accuracy, providing coverage compatible with ASIL B compliance. Built-in EEPROM scratch memory offers traceability of the device throughout the IC's production process.

The IC is offered in the UB package, which integrates the IC and a high temperature ceramic capacitor in a single overmolded SIP package for enhanced EMC performance. The 2-pin SIP package is lead (Pb) free, with tin leadframe plating.

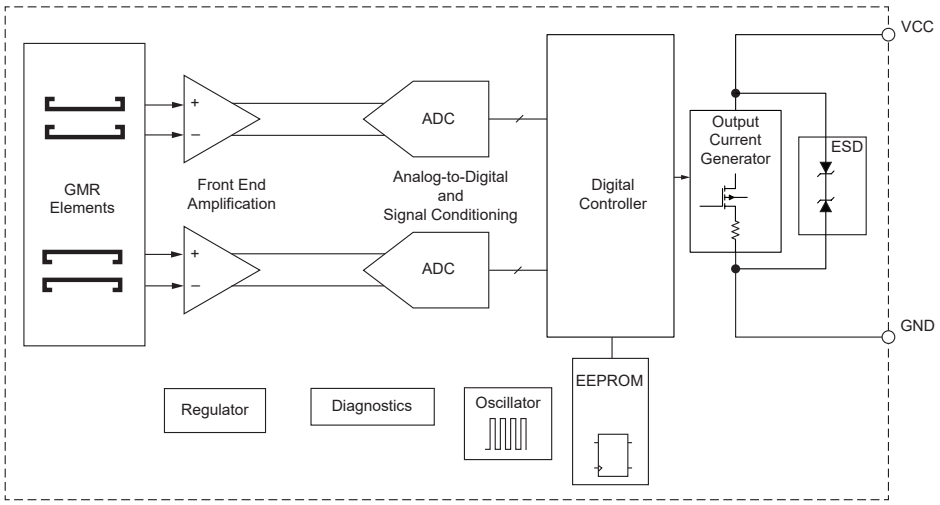
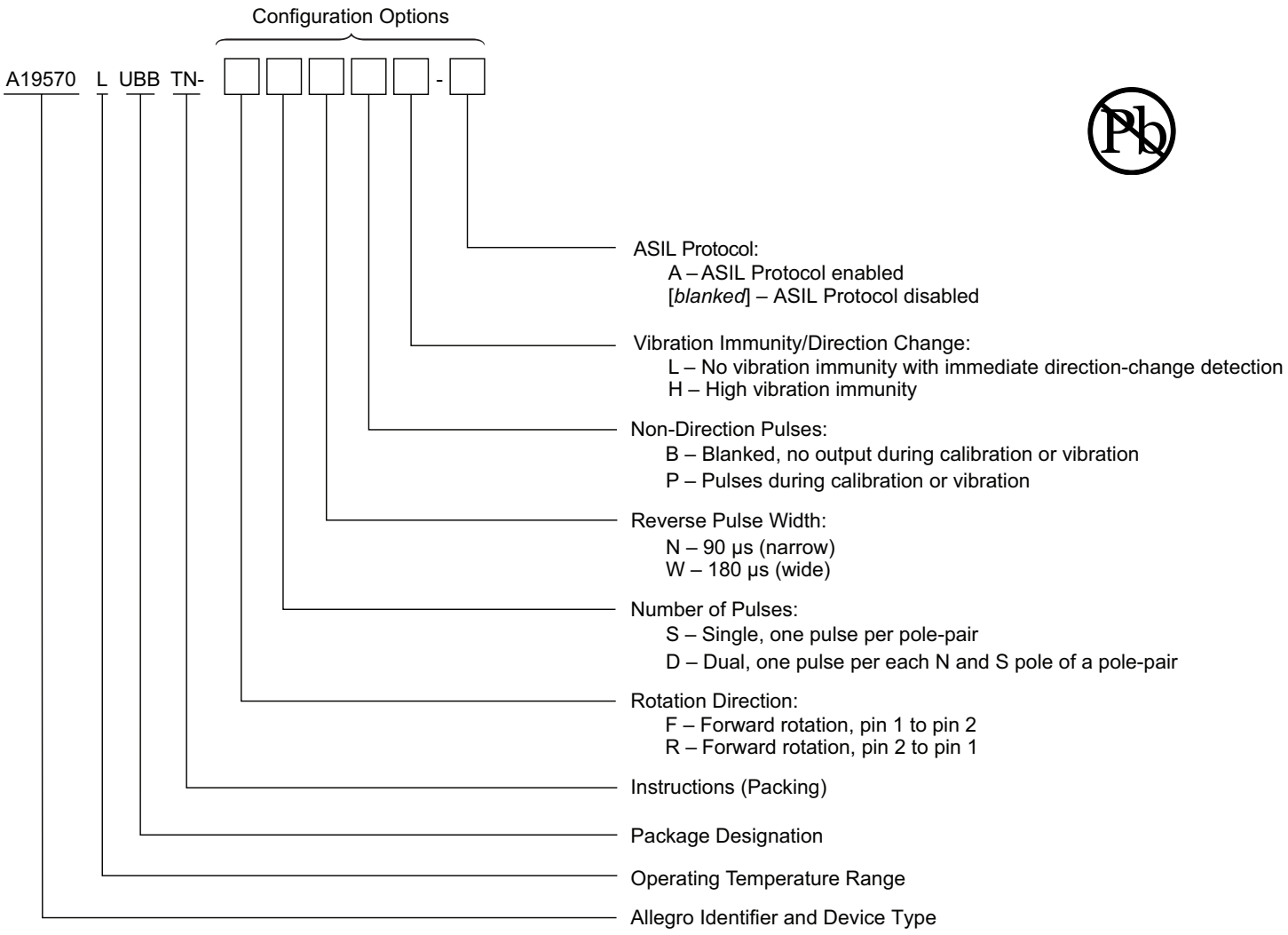


Figure 1: Functional Block Diagram

SELECTION GUIDE



SELECTION GUIDE*

Part Number	Packing
A19570LUBBTN-FSWPH	Tape and Reel, 4000 pieces per reel
A19570LUBBTN-RSWPH	

* Not all combinations are available. Contact Allegro sales for availability and pricing of custom programming options.

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SPECIFICATIONS

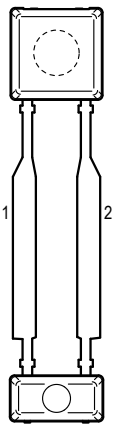
ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}	Refer to Power Derating section; Potential between pin 1 and pin 2	28	V
Reverse Supply Voltage	V_{RCC}		–18	V
Operating Ambient Temperature	T_A		–40 to 150	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C
Applied Magnetic Flux Density	B	In any direction	500	G

INTERNAL DISCRETE CAPACITOR RATINGS

Characteristic	Symbol	Test Conditions	Value	Unit
Nominal Capacitance	C_{SUPPLY}	Connected between pin 1 and pin 2 (refer to Figure 2)	10	nF

PINOUT DIAGRAM AND TERMINAL LIST



Package UB, 2-Pin SIP Pinout Diagram

Terminal List Table

Pin Name	Pin Number	Function
VCC	1	Supply Voltage
GND	2	Ground

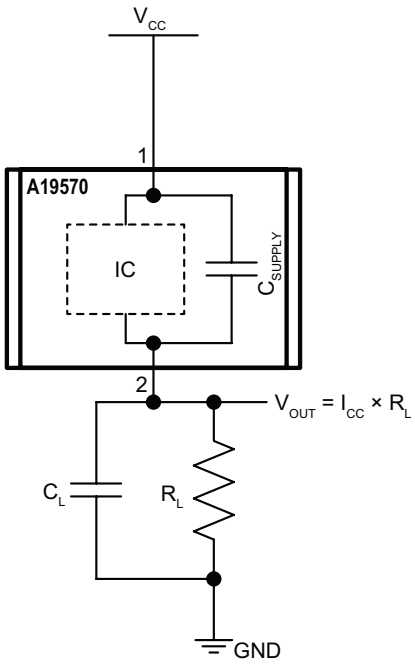


Figure 2: Application Circuit

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OPERATING CHARACTERISTICS: Valid throughout full operating voltage and ambient temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage [2]	V_{CC}	Potential between pin 1 and pin 2	4	–	24	V
Reverse Supply Current [3]	I_{RCC}	$V_{CC} = V_{RCC(MAX)}$	–10	–	–	mA
Supply Zener Clamp Voltage	$V_{Zsupply}$	$I_{CC} = I_{CC(MAX)} + 3$ mA, $T_A = 25°C$; Potential between pin 1 and pin 2	28	–	–	V
Supply Current	$I_{CC(LOW)}$	Low-current state	5.9	7	8.4	mA
	$I_{CC(HIGH)}$	High-current state	12	14	16	mA
Supply Current Ratio [4]	$I_{CC(HIGH)}/I_{CC(LOW)}$	Measured as a ratio of high current to low current (isothermal)	1.9	–	–	–
ASIL Safe State Current	I_{RESET}	Refer to Figure 12 (-xxxxx-A variant)	1.5	3.5	3.9	mA
ASIL Safe State Current Time	$t_{RESET(EP1)}$	Refer to Figure 12 (-xxxxx-A variant) (Error Protocol 1)	–	90	–	µs
	$t_{RESET(EP2)}$	Refer to Figure 12 (-xxxxx-A variant) (Error Protocol 2)	3	–	6	ms
Output Rise/Fall Time	t_r, t_f	Voltage measured at terminal 2 in Figure 2; $R_L = 100\ \Omega$, $C_L = 10$ pF, measured between 10% and 90% of $I_{CC(LOW)}$ and $I_{CC(HIGH)}$	–	2	4	µs
POWER-ON CHARACTERISTICS						
Power-On State	POS	$V_{CC} > V_{CC(min)}$, as connected in Figure 2	$I_{CC(LOW)}$			mA
Power-On Time	t_{PO}	$V_{CC} > V_{CC(min)}$, as connected in Figure 2 [5]	–	–	1	ms
OUTPUT PULSE-WIDTH PROTOCOL [6]						
Forward Pulse Width	$t_{w(FWD)}$	-xxNxx variant and -xxWxx variant	38	45	52	µs
Reverse Pulse Width	$t_{w(REV)}$	-xxNxx variant	76	90	104	µs
		-xxWxx variant	153	180	207	µs
Nondirection Pulse Width	$t_{w(ND)}$	-xxNPx variant	153	180	207	µs
		-xxWPx variant	306	360	414	µs

[1] Typical values are at $T_A = 25°C$ and $V_{CC} = 12$ V. Performance may vary for individual units, within the specified maximum and minimum limits.
[2] Maximum voltage must be adjusted for power dissipation and junction temperature; see representative Power Derating section.
[3] Negative current is defined as conventional current coming out of (sourced from) the specified device terminal.
[4] Supply current ratio is taken as a mean value of $I_{CC(HIGH)} / I_{CC(LOW)}$.
[5] Time between power-on to I_{CC} stabilizing. Transitions prior to t_{PO} should be ignored.
[6] Pulse width measured at threshold of $(I_{CC(HIGH)} + I_{CC(LOW)}) / 2$. ASIL Safe State Current Time is measured at the threshold of $(I_{RESET} + I_{CC(LOW)}) / 2$.

Continued on the next page…

OPERATING CHARACTERISTICS (continued): Valid throughout full operating voltage and ambient temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
INPUT CHARACTERISTICS AND PERFORMANCE						
Operating Frequency, Forward Rotation [7]	f_{FWD}	-xSxxx variant	0	–	12	kHz
Operating Frequency, Reverse Rotation [7]	f_{REV}	-xSNxx variant	0	–	7	kHz
		-xSWxx variant	0	–	4	kHz
Operating Frequency, Nondirection Pulses [7]	f_{ND}	-xSNPx variant	0	–	4	kHz
		-xSWPx variant	0	–	2.2	kHz
Operating Differential Magnetic Input [8]	$B_{DIFF(pk-pk)}$	Minimum allowable for switching in Parallel Orientation (refer to Figure 8)	5	–	–	G
		Minimum allowable for switching in Perpendicular Orientation (refer to Figure 9)	11	–	–	G
Operating Differential Magnetic Range [8]	B_{DIFF}	Refer to Figure 6	–50	–	50	G
Allowable Differential Sequential Signal Variation	$B_{SEQ(n+1)}/B_{SEQ(n)}$	Signal period-to-period variation (refer to Figure 3)	60	–	200	%
	$B_{SEQ(n+i)}/B_{SEQ(n)}$	Overall signal variation (run-out) (refer to Figure 3)	40	–	200	%
Operate Point	B_{OP}	% of peak-to-peak IC-processed signal	–	70	–	%
Release Point	B_{RP}	% of peak-to-peak IC-processed signal	–	30	–	%
Target Pitch	T_{PITCH}	Arc length of each pole-pair (at 0 mm air gap)	1.4	–	8	mm
Switch Point Separation	$B_{DIFF(SP-SEP)}$	Required amount of amplitude separated between channels at each B_{OP} and B_{RP} occurrence. (refer to Figure 5)	20	–	–	%pk-pk
THERMAL CHARACTERISTICS						
Magnetic Temperature Coefficient [9]	TC	Valid for full temperature range based on ferrite	–	0.2	–	%/°C
Package Thermal Resistance	$R_{\theta JA}$	Single-layer PCB with copper limited to solder pads	–	213	–	°C/W

[7] Maximum Operating Frequency is determined by satisfactory separation of output pulses: $I_{CC(LOW)}$ of $t_{w(FWD)(min)}$. If the customer can resolve shorter low-state durations, maximum f_{REV} and f_{ND} may be increased.

[8] Differential magnetic field is measured for the Channel A (E1-E3) and Channel B (E2-E4). Each channel's differential magnetic field is measured between two GMR elements spaced by 1.4 mm. Magnetic field is measured in the By direction (Refer to Figure 7). To maintain optimal performance, it is recommended that the |Bx| field be less than 80 G.

[9] Ring magnet decreases strength with rising temperature, and the device compensates. Note that $B_{DIFF(pk-pk)}$ requirement is not influenced by this.

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OPERATING CHARACTERISTICS (continued): Valid throughout full operating voltage and ambient temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
PERFORMANCE CHARACTERISTICS						
Vibration Immunity Startup	$Err_{VIB(SU)}$	-xSxxH variant	2 × T_{CYCLE}	–	–	–
		-xSxxL variant	0.06 × T_{CYCLE}	–	–	–
Vibration Immunity Running Mode	Err_{VIB}	-xSxxH variant	2 × T_{CYCLE}	–	–	–
		-xSxxL variant	0.03 × T_{CYCLE}	–	–	–
First Direction Output Pulse [10]		-xSxxH variant	–	–	4 × T_{CYCLE}	–
		-xSxxL variant	–	–	4 × T_{CYCLE}	–
First Direction-Pulse Output Following Direction Change [10]		-xSxxH variant	–	–	4 × T_{CYCLE}	–
		-xSxxL variant	–	–	1.75 × T_{CYCLE}	–
First Direction-Pulse Output Following Startup Mode Vibration [10]		-xSxxH variant	–	–	4.25 × T_{CYCLE}	–
		-xSxxL variant	–	–	3.75 × T_{CYCLE}	–
First Direction-Pulse Output Following Running Mode Vibration [10]		-xSxxH variant	–	–	4.25 × T_{CYCLE}	–
		-xSxxL variant	–	–	3.75 × T_{CYCLE}	–

[10] Power-up frequencies ≤ 1 kHz. Rotational frequencies above 1 kHz may require more input magnetic cycles until output edges are achieved.

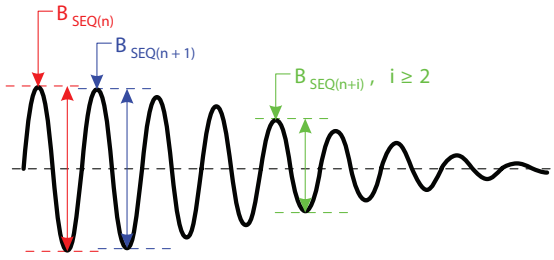
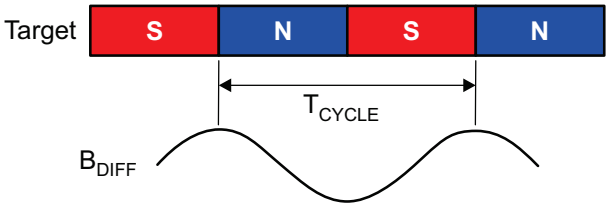


Figure 3: Differential Signal Variation



T_{CYCLE} = Target Cycle; the amount of rotation that moves one north pole and one south pole across the sensor

B_{DIFF} = Differential Input Signal; the differential magnetic flux density sensed by the sensor

Figure 4: Definition of T_{CYCLE}

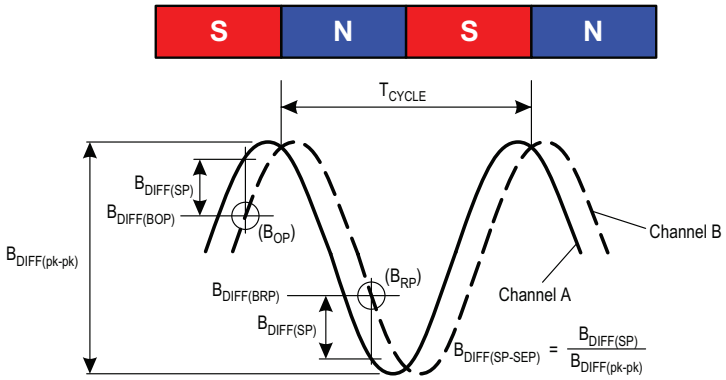


Figure 5: Definition of Switch Point Separation

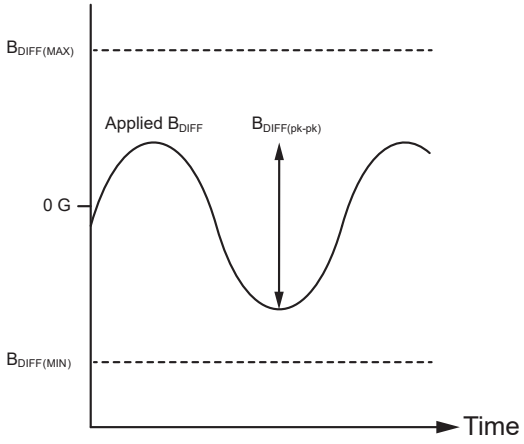


Figure 6: Input Signal Definition

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FUNCTIONAL DESCRIPTION

The A19570 sensor IC contains a single-chip GMR circuit that uses spaced elements. These elements are used in differential pairs to provide electrical signals containing information regarding speed and direction of target rotation. The A19570 is intended for use with ring magnet targets.

The IC detects the peaks of the magnetic signals and sets dynamic thresholds based on these detected signals.

Installation Orientation Flexibility

The A19570 can be installed in a parallel, perpendicular, or any orientation in between with respect to the ring magnet. Refer to Figure 7, Figure 8, and Figure 9 for parallel and perpendicular orientations of the sensor.

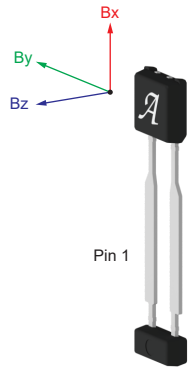

Figure 7: Package Orientation

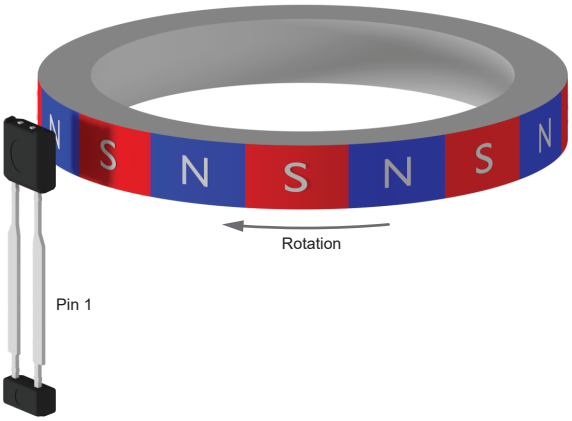

Figure 8: Parallel Orientation

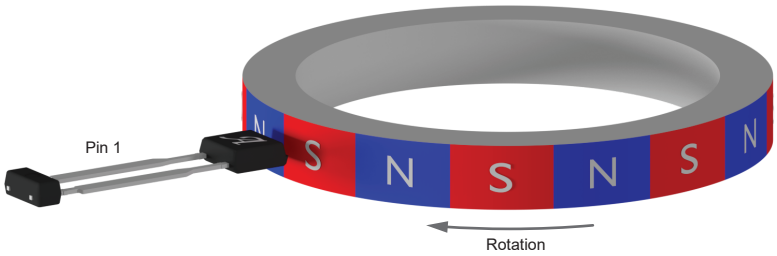

Figure 9: Perpendicular Orientation

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Data Protocol Description

When a target passes in front of the device (opposite the branded face of the package case), the A19570 generates an output pulse for each magnetic pole-pair (-xSxxx variant) of the target. Speed information is provided by the output pulse rate, while direction of target rotation is provided by the duration of the output pulses. The sensor IC can sense target movement in both the forward and reverse directions.

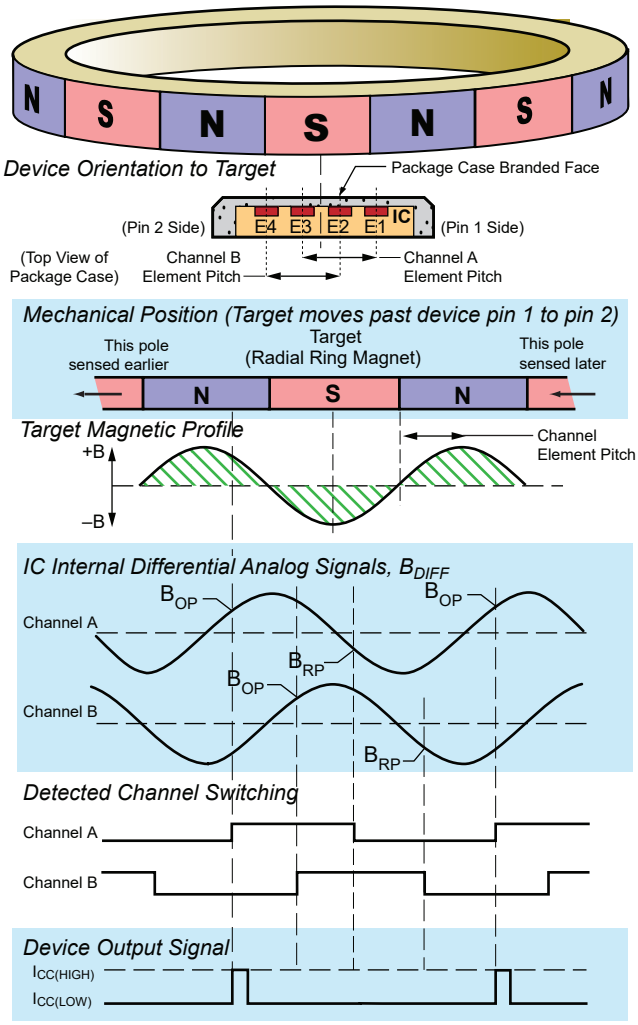

Figure 10: Basic Operation

Forward Rotation. For the -Fxxxx variant, when the target is rotating such that a target feature passes from pin 1 to pin 2, this is referred to as forward rotation. This direction of rotation is indicated on the output by a $t_{W(FWD)}$ pulse width. For the -Rxxxx variant, forward direction is indicated for target rotation from pin 2 to 1.

Reverse Rotation. For the -Fxxxx variant, when the target is rotating such that a target feature passes from pin 2 to pin 1, this is referred to as reverse rotation. This direction of rotation is indicated on the output by a $t_{W(REV)}$ pulse width. For the -Rxxxx variant, reverse direction is indicated for target rotation from pin 1 to 2.

Output edges are triggered by B_{DIFF} transitions through the switchpoints. On a crossing, the output pulse of $I_{CC(HIGH)}$ is present for $t_{w(FWD)}$ or $t_{w(REV)}$.

The IC is always capable of properly detecting input signals up to the defined operating frequency. At frequencies beyond the operational frequency specifications (refer to Operational Frequency specifications noted on page 5), the $I_{CC(HIGH)}$ pulse duration will collide with subsequent pulses.

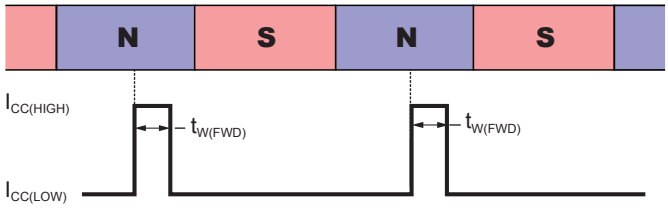

Figure 11: Output Timing Example (-xSxxx variant)

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ASIL Safe State Output Protocol

The A19570 sensor IC contains diagnostic circuitry that will continuously monitor occurrences of failure defects within the IC. Refer to Figure 12 for the output protocol of the ASIL safe state after an internal defect has been detected. Error Protocol 1 will result from faults due to overfrequency conditions from the input signal. Error Protocol 2 will result from hard failures detected within the A19570 such as a regulator and front end fault.

Note: If a fault exists continuously, the device will stay in permanent safe state. Refer to the A19570 Safety Manual for additional details on the ASIL Safe State Output Protocol.

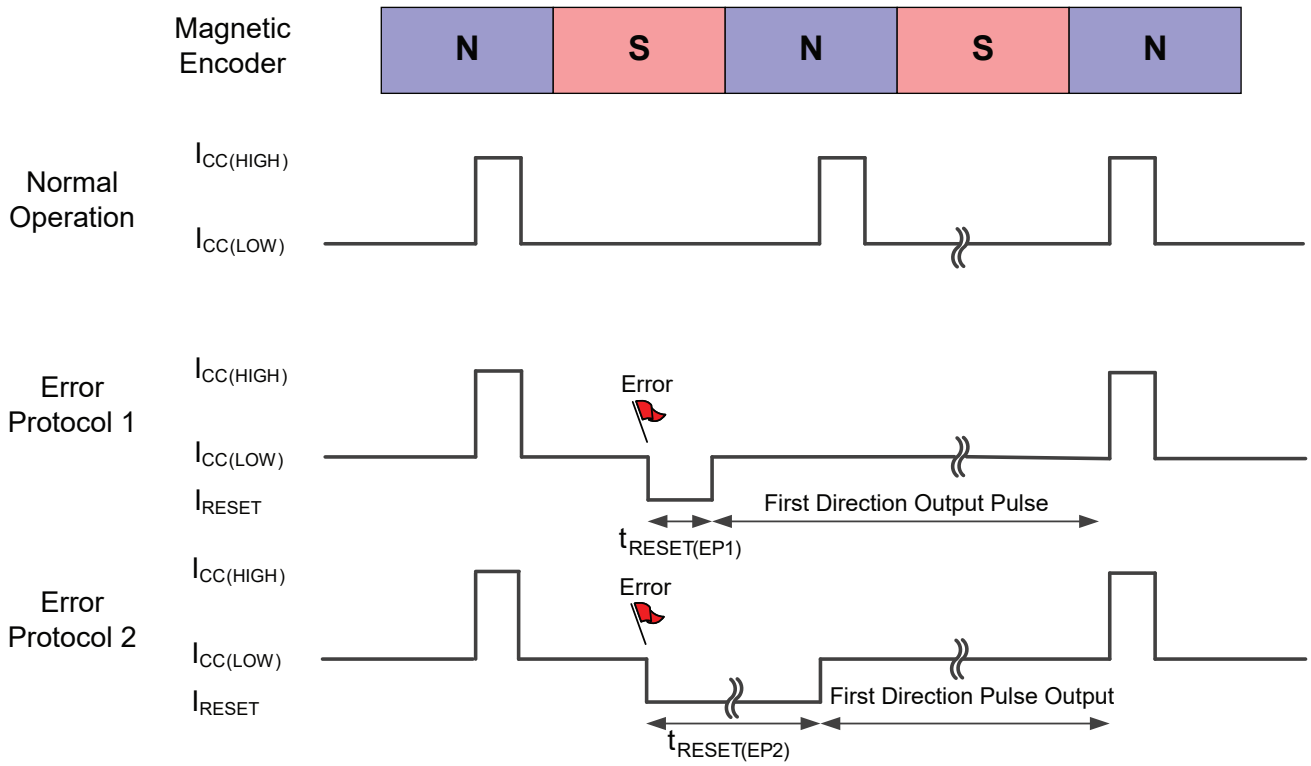

Figure 12: Output Protocol of the -xxxBx-A Variant (ASIL Safe State)

Calibration and Direction Validation

When power is applied to the A19570, the built-in algorithm performs an initialization routine. For a short period after power-on, the device calibrates itself and determines the direction of target rotation. For the -xxxPx variant, the output transmits nondirection pulses during calibration (Figure 13). For the -xxxBx variant, the output does not transmit any pulses during calibration.

Once the calibration routine is complete, the A19570 will transmit accurate speed and direction information.

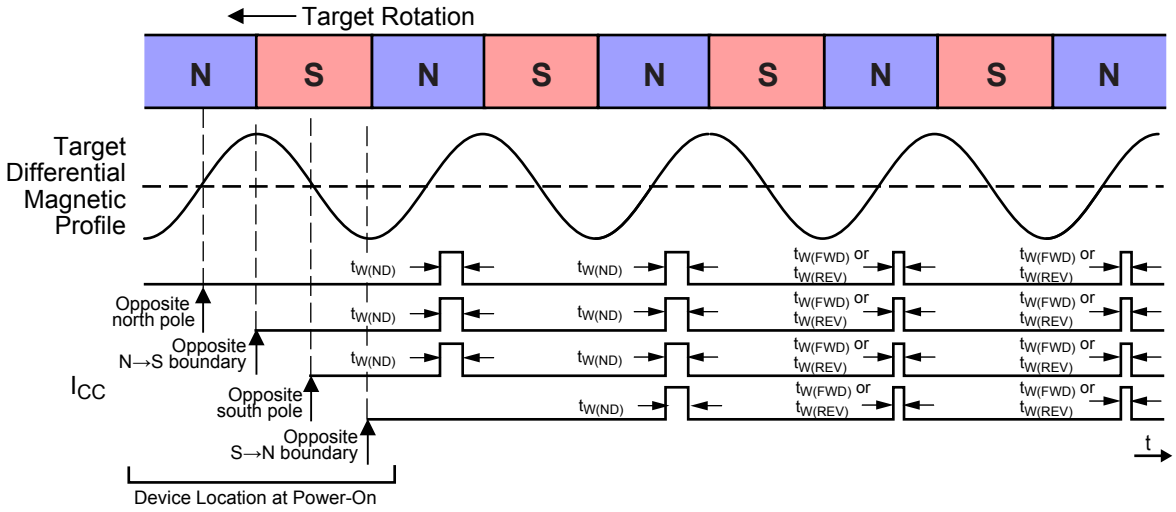

Figure 13: Calibration Behavior of the -xSxPH Variant

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Direction Changes, Vibrations, and Anomalous Events

During normal operation, the A19570 will be exposed to changes in the direction of target rotation (Figure 14), vibrations of the target (Figure 15), and anomalous events such as sudden air gap changes. These events cause temporary uncertainty in the A19570's internal direction detection algorithm.

The -xxxPx variant may transmit non-direction pulses during vibrations, and the -xxxBx variant will not transmit any pulses during vibrations.

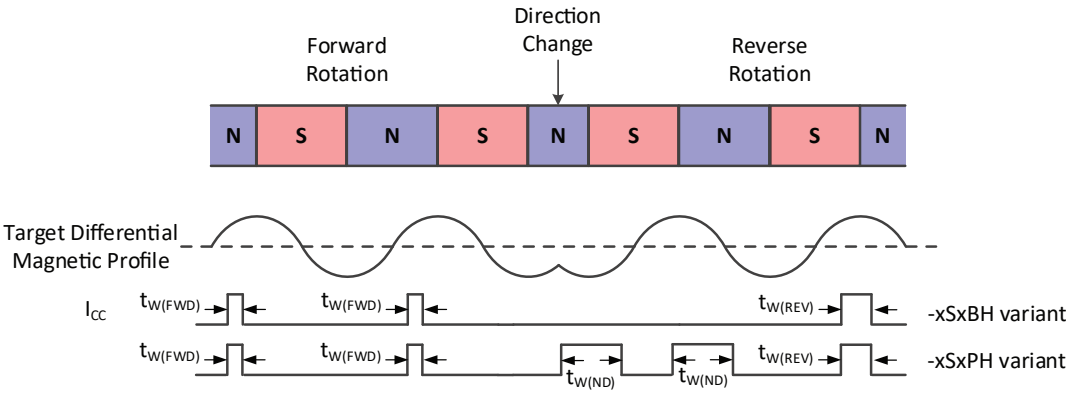

Figure 14: Direction Change Behavior

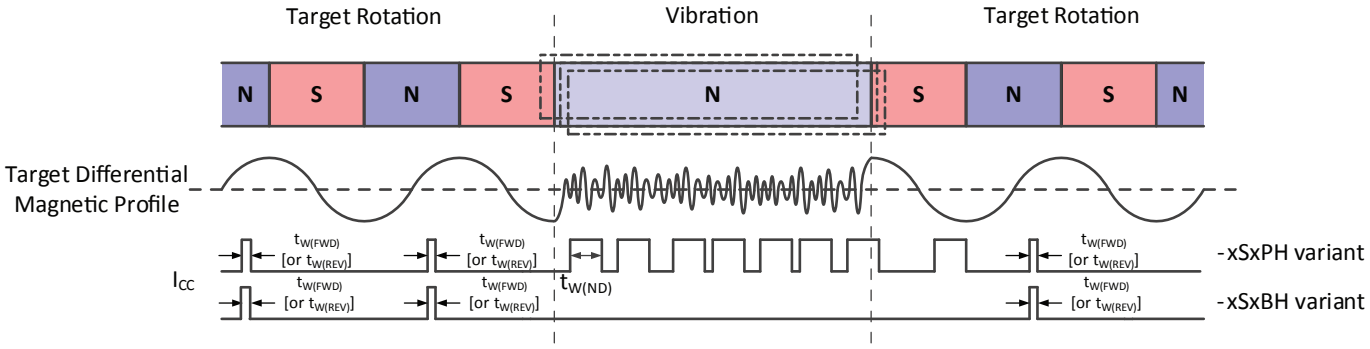

Figure 15: Vibration Behavior

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POWER DERATING

The device must be operated below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is a relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D) can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as:

T_A= 25°C, V_{CC} = 12 V, $R_{\theta JA}$ = 213°C/W, and I_{CC} = 7.15 mA,

then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 7.15\ mA = 85.8\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 85.8\ mW \times 213°C/W = 18.3°C$$

$$T_J = T_A + \Delta T = 25°C + 18.3°C = 43.3°C$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)}$, $I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A = 150°C.

Observe the worst-case ratings for the device, specifically:

$R_{\theta JA}$ = 213°C/W (subject to change), $T_{J(max)}$ = 165°C, $V_{CC(max)}$ = 24 V, and $I_{CC(AVG)}$ = 15.4 mA. $I_{CC(AVG)}$ is computed using $I_{CC(HIGH)(max)}$ and $I_{CC(LOW)(max)}$, with a duty cycle of 92% computed from $t_{w(ND)(max)}$ on-time and $t_{w(FWD)(min)}$ off-time (pulse-width protocol). This condition happens at a select limited frequency.

Calculate the maximum allowable power level, $P_{D(max)}$. First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165°C - 150°C = 15\ °C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 213°C/W = 70.4\ mW$$

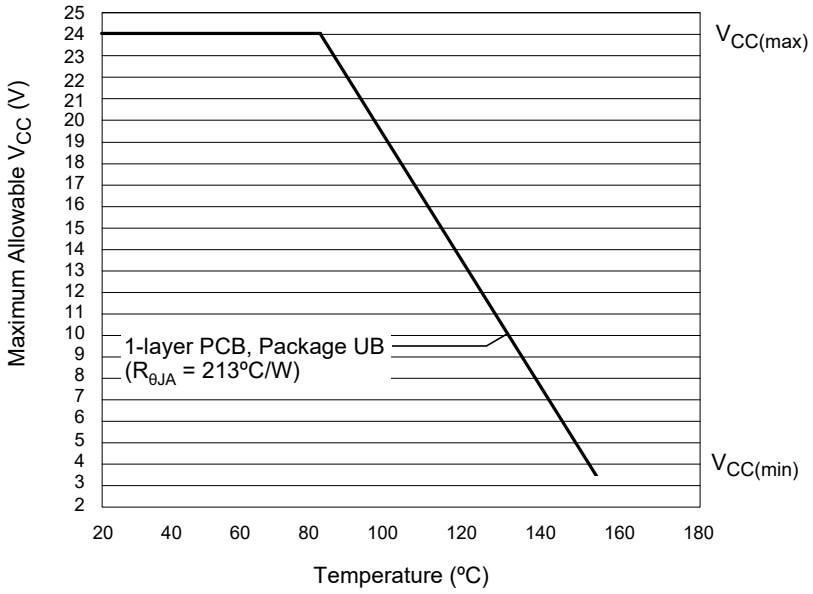
Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 70.4\ mW \div 15.4\ mA = 4.6\ V$$

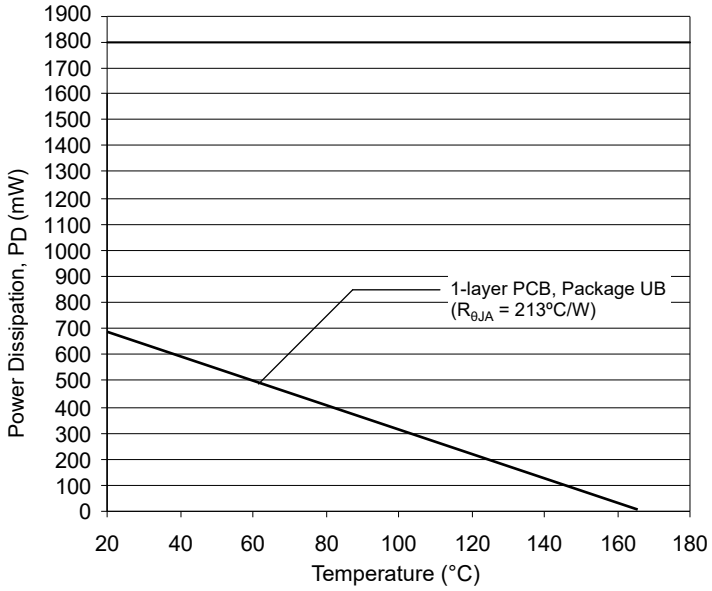
The result indicates that, at T_A , the application and device can dissipate adequate amounts of heat at voltages ≤ $V_{CC(est)}$.

Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \leq V_{CC(max)}$, then reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these conditions.

Power Derating Curve



Power Dissipation versus Ambient Temperature



PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-0000408, Rev. 3)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

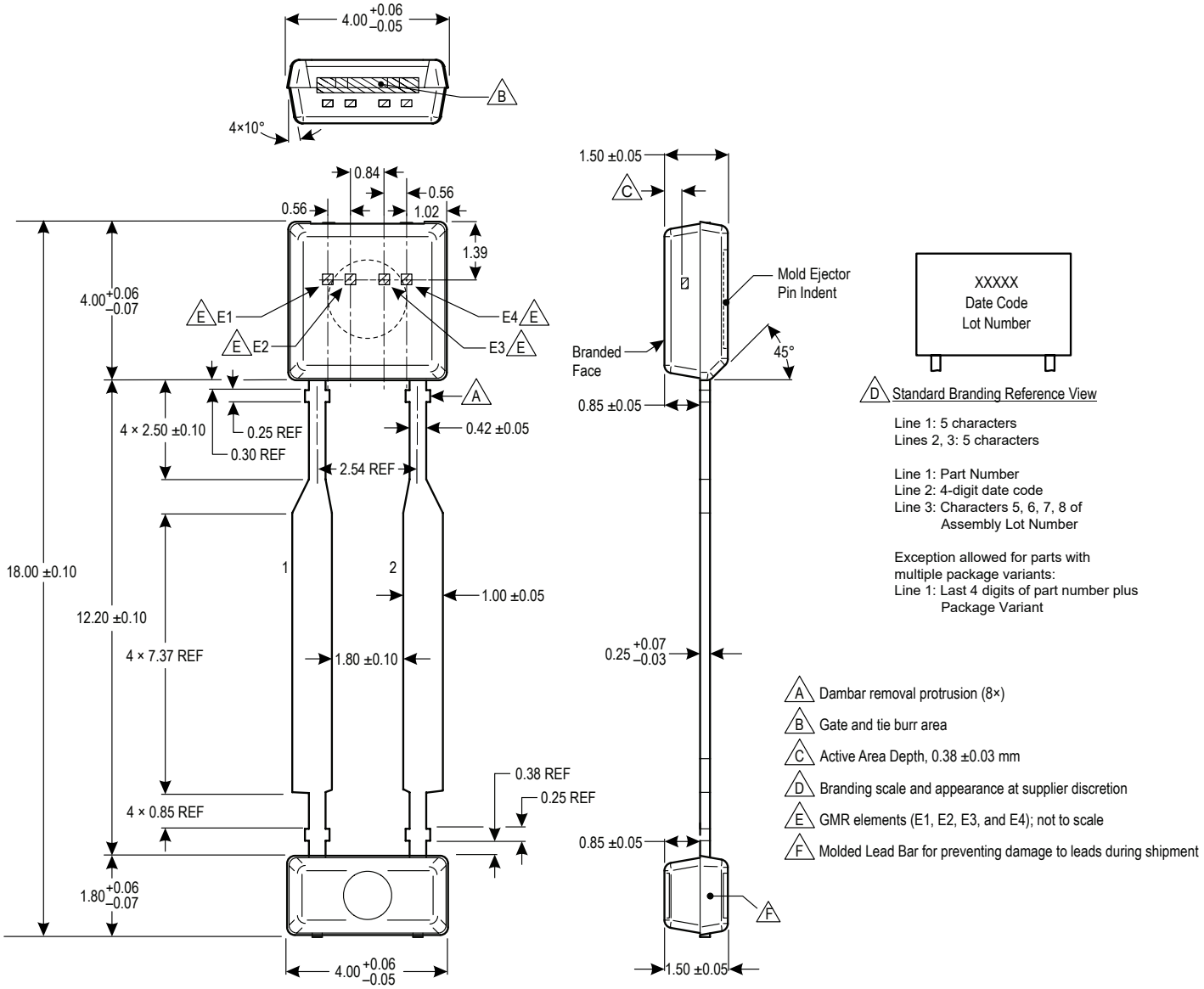


Figure 16: Package UB, 2-Pin SIP

Revision History

Number	Date	Description
–	November 14, 2018	Initial release

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