

MN74HC76/MN74HC76S

Dual J-K Flip-Flop with Preset and Clear

■ Outline

The MN74HC76/MN74HC76S consists of J-K flip-flop with preset inputs and clear inputs, and has two built-in circuits in one chip.

The respective flip-flop has independent J input, K input, preset input, clear input, clock input, and complementary outputs Q and \bar{Q} . Each input data is transmitted to the output at the falling edge of the clock pulse. The preset input and the clear input are independent of the clock input, and their active level is "L".

Owing to the silicon gate CMOS process, these flip-flop have realized low power consumption and high noise immunity equivalent to those of a standard CMOS and the operation speed as high as of an LS TTL. The MN74HC76/MN74HC76S can directly drive ten LS TTL inputs.

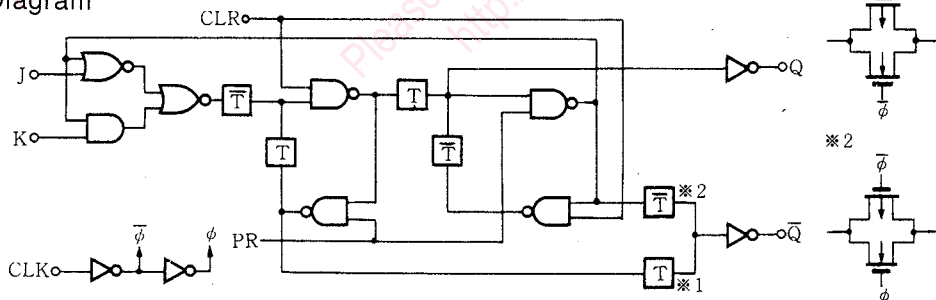
To protect the input and output against electrostatic breakdown, a resistor and a diode are used for the V_{CC} and the GND. The pin configuration and the function are the same as those of the standard 54LS/74LS logic family.

■ Truth Table

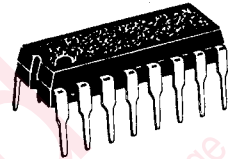
Input					Output	
PR	CLR	CLK	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	\simeq	L	L	Q0	$\bar{Q}0$
H	H	\simeq	H	L	H	L
H	H	\simeq	L	H	L	H
H	H	\simeq	H	H	Toggle	
H	H	H	X	X	Q0	$\bar{Q}0$

- Note) 1. X : "H" or "L" either will do.
 2. \simeq : Trailing in negative direction
 3. Q0 : Q level before input conditions in table are confirmed.
 4. $\bar{Q}0$: \bar{Q} level before input conditions in table are confirmed.
 5. Toggle : Each output becomes complement of previous state by change of \simeq .
 6. H* : When preset, clear are "L", Q, \bar{Q} are H but when preset clear are "H" simultaneously state of Q, \bar{Q} can not be predicted.

■ Logic Diagram



P-3



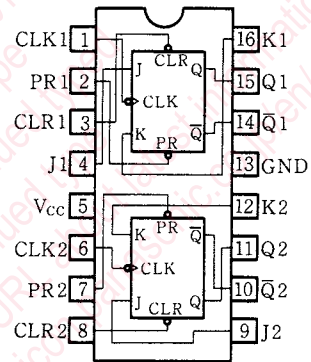
16-pin plastic DIL package

P-4



16-pin PANAFLAT package (SO-16D)

Pin Configuration



■ Absolute Maximum Ratings

Item		Symbol	Rating	Unit
Supply voltage		V_{CC}	-0.5~+7.0	V
Input output voltage		V_I, V_O	-0.5~ $V_{CC}+0.5$	V
Input protective diode current		I_{IK}	±20	mA
Output parasitic diode current		I_{OK}	±20	mA
Output current		I_O	±25	mA
Supply current		I_{CC}, I_{GND}	±50	mA
Storage temperature		T_{stg}	-65~+150	°C
Power dissipation	MN74HC76	$T_a = -40 \sim +60^\circ\text{C}$	400	mW
		$T_a = +60 \sim +85^\circ\text{C}$	Decrease to 200mW at the rate of 8mW/°C	
	MN74HC76S	$T_a = -40 \sim +60^\circ\text{C}$	275	mW
		$T_a = +60 \sim +85^\circ\text{C}$	Decrease to 200mW at the rate of 3.8mW/°C	

■ Recommended Operating Conditions

Item	Symbol	$V_{CC}(V)$	Rating	Unit
Operating power supply voltage	V_{CC}		1.4~6.0	V
Input output voltage	V_I, V_O		0~ V_{CC}	V
Operating temperature	T_A		-40~+85	°C
Input rise, fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

Item	Symbol	V_{CC} (V)	Test Condition			Temperature					Unit
			V_I	V_O	Unit	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim +85^\circ\text{C}$		
						min.	typ.	max.	min.	max.	
Input voltage high level	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input voltage low level	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output voltage high level	V_{OH}	2.0		-20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	-20.0	μA	4.4	4.5		4.4		
		6.0	or	-20.0	μA	5.9	6.0		5.9		
		4.5	V_{IL}	-4.0	mA	3.92			3.84		
		6.0		-5.2	mA	5.48			5.34		
Output voltage low level	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	
		6.0	or	20.0	μA		0.0	0.1		0.1	
		4.5	V_{IL}	4.0	mA			0.26		0.33	
		6.0		5.2	mA			0.26		0.33	
Input leakage current	I_I	6.0	$V_I = V_{CC}$ or GND					±0.1		±1.0	μA
Static supply current	I_{CC}	6.0	$V_I = V_{CC}$ or GND, $I_O = 0$					4.0		40.0	μA

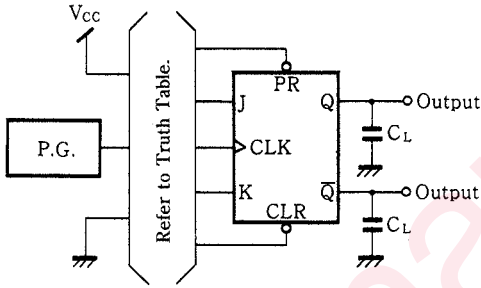
■ AC Characteristics (GND=0V, Input transition time ≤ 6 ns, $C_L=50$ pF)

Item	Symbol	V _{CC} (V)	Test Condition	Temperature					Unit
				Ta=25°C			Ta=-40~+85°C		
				min.	typ.	max.	min.	max.	
Output rise time	t _{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t _{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time CLK→Q, \bar{Q} (L→H)	t _{PLH}	2.0			44	150		190	ns
		4.5			17	30		38	
		6.0			14	26		33	
Propagation time CLK→Q, \bar{Q} (H→L)	t _{PHL}	2.0			38	150		190	ns
		4.5			15	30		38	
		6.0			12	26		30	
Propagation time PR, CLR→Q, \bar{Q} (L→H)	t _{PLH}	2.0			51	175		220	ns
		4.5			19	35		44	
		6.0			15	30		37	
Propagation time PR, CLR→Q, \bar{Q} (H→L)	t _{PHL}	2.0			42	175		220	ns
		4.5			16	35		44	
		6.0			13	30		37	
Minimum pulse width PR, CLR	t _w	2.0			24	75		95	ns
		4.5			11	15		19	
		6.0			7	13		16	
Minimum set-up time	t _{su}	2.0			28	100		125	ns
		4.5			12	20		25	
		6.0			9	17		21	
Minimum hold time	t _h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum recovery time	t _{rem}	2.0			3	75		95	ns
		4.5			2	15		19	
		6.0			1	13		16	
Maximum clock frequency	f _{max}	2.0			6	15		4	MHz
		4.5			30	39		24	
		6.0			35	46		28	

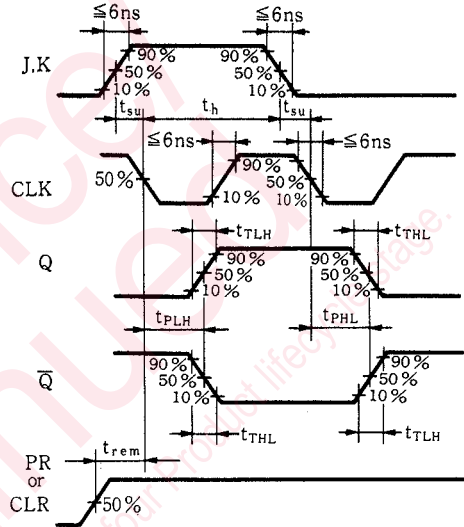
• Switching time measuring circuit and waveforms

(1) t_{TLH} , t_{THL} , t_{su} , f_{max} , t_{PLH}/t_{PHL} (CLK \rightarrow Q, \bar{Q})

1. Measuring circuit

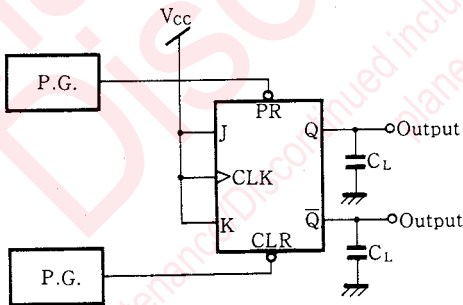


2. Switching waveforms

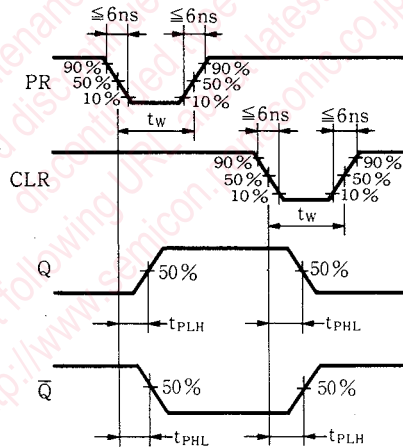


(2) t_{PLH}/t_{PHL} (PR, CLR \rightarrow Q, \bar{Q}), t_w (PR, CLR)

1. Measuring circuit



2. Switching waveforms



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