TS 68882

CMOS ENHANCED FLOATING-POINT COPROCESSOR

DESCRIPTION

The TS 68882 enhanced floating-point coprocessor is a full implementation of the IEEE Standard for Binary Floating-Point Arithmetic (754) for use with the THOMSON TS 68000 Family of microprocessors. It is a pin and software compatible upgrade of the TS 68881 with an optimized MPU interface that provides over 1.5 times the performance of the TS 68881. It is implemented using VLSI technology to give systems designers the highest possible functionality in a physically small device.

Intended primarily for use as a coprocessor to the TS 68020/68030 32-bit microprocessor units (MPUs), the TS 68882 provides a logical extension to the main MPU integer data processing capabilities. It does this by providing a very high performance floating-point arithmetic unit and a set of floating-point data registers that are utilized in a manner that is analogous to the use of the integer data registers. The TS 68882 instruction set is a natural extension of all earlier members of the TS 68000 Family, and supports all of the addressing modes of the host MPU. Due to the flexible bus interface of the TS 68000 Family, the TS 68882 can be used with any of the MPU devices of the TS 68000 Family, and it may also be used as a peripheral to non-TS 68000 processors.

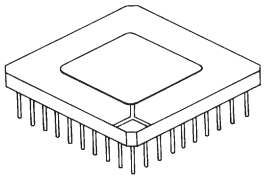
MAIN FEATURES

- Eight general purpose floating-point data registers, each supporting a full 80-bit extended precision real data format (a 64-bit mantissa plus a sign bit, and a 15-bit signed exponent).
- A 67-bit arithmetic unit to allow very fast calculations, with intermediate are precision greater than the extended precision format.
- A 67-bit barrel shifter for high-speed shifting operations (for normalizing etc.).
- Special purpose hardware for high-speed conversion between single, double, and extended formats and the internal extended format.
- An independent state machine to control main processor communication for pipelined instruction processing.
- Forty-six instructions, including 35 arithmetic operations.
- Full conformation to the IEEE 754 standard, including all requirements and suggestions.
- Support of functions not defined by the IEEE standard, including a full set of trigonometric and transcendental functions.
- Seven data types : byte, word and long integers ; single, double, and extended precision real numbers ; and packed binary coded decimal string real numbers.
- Twenty-two constants available in the on-chip ROM, including π, e, and powers of 10.
- Virtual memory / machine operations.
- Efficient mechanisms for procedure calls, context switches, and interrupt handling.
- Fully concurrent instruction execution with the main processor.
- Fully concurrent instruction execution of multiple floating-point instructions.
- Use with any host processor, on an 8-, 16- or 32-bit data bus.
- Available in 16.67, 20, 25 and 33 MHz for T_C from $-55°C$ to $+125°C$.
- $V_{CC} = 5\ V \pm 10\ \%$.

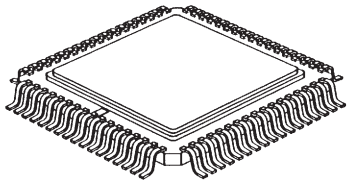
SCREENING / QUALITY

This product could be manufactured in full compliance with either :

- CECC 90110-024 (class B, assessment level Y).
- MIL-STD-883 class B.
- DESC 5962-89436.
- or according to TCS standards.



R suffix
PGA 68
Ceramic Pin Grid Array



F suffix
CQFP 68
Ceramic Quad Flat Pack

SUMMARY

A · GENERAL DESCRIPTION

1 · INTRODUCTION

The TS 68882 is a high performance floating-point device designed to interface with the TS 68020 or TS 68030 as a coprocessor. This device fully supports the TS 68000 virtual machine architecture, and is implemented in HCMOS, THOMSON's low power, small geometry process. This process allows CMOS and HMOS (high-density NMOS) gates to be combined on the same device. CMOS structures are used where speed and low power is required, and HMOS structures are used where minimum silicon area is desired. The HCMOS technology enables the TS 68882 to be very fast while consuming less power than comparable HMOS, and still have a reasonably small die size.

With some performance degradation, the TS 68882 can also be used as a peripheral processor in systems where the TS 68020 or TS 68030 is not the main processor (e.g., TS 68000, TS 68008, TS 68010). The configuration of the TS 68882 as a peripheral processor or coprocessor may be completely transparent to user software (i.e., the same object code may be executed in either configuration).

The architecture of the TS 68882 appears to the user as a logical extension of the TS 68000 Family architecture. Coupling of the coprocessor interface, allows the TS 68020 / TS 68030 programmer to view the TS 68882 registers as though the registers are resident in the TS 68020 / TS 68030. Thus, a TS 68020 or TS 68030 / TS 68882 device pair appears to be one processor that supports seven floating-point and integer data types, and has eight integer data registers, eight address registers, and eight floating-point data registers.

As shown in Figure 1, the TS 68882 is internally divided into four processing elements ; the bus interface unit (BIU), the conversion control unit (CCU), the execution control unit (ECU), and the microcode control unit (MCU). The BIU communicates with the main processor, the CCU controls the main processor communications dialog and performs some data conversions, and the ECU and MCU execute most floating-point calculations.

The BIU contains the coprocessor interface registers, and the 32-bit control, status, and instruction address registers. In addition to these registers, the register select and DSACK timing control logic is contained in the BIU. Finally, the status flags used to monitor the status of communications with the main processor are contained in the BIU.

The CCU contains special purpose hardware that performs conversions between the single, double, and extended precision memory data formats and the internal data format used by the ECU. It also contains a state machine that controls communications with the main processor during coprocessor interface dialogs.

The eight 80-bit floating-point data registers (FP0-FP7) are located in the ECU. In addition to these registers, the ECU contains a high-speed 67-bit arithmetic unit used for both mantissa and exponent calculations, a barrel shifter that can shift from 1 bit to 67 bits in one machine cycle, and ROM constants (for use by the internal algorithms or user programs).

The MCU contains the clock generator, a two-level microcoded sequencer that controls the ECU, the microcode ROM, and self-test circuitry. The built-in self-test capabilities of the TS 68882 enhance reliability and ease manufacturing requirements ; however, these diagnostic functions are not available to the user.

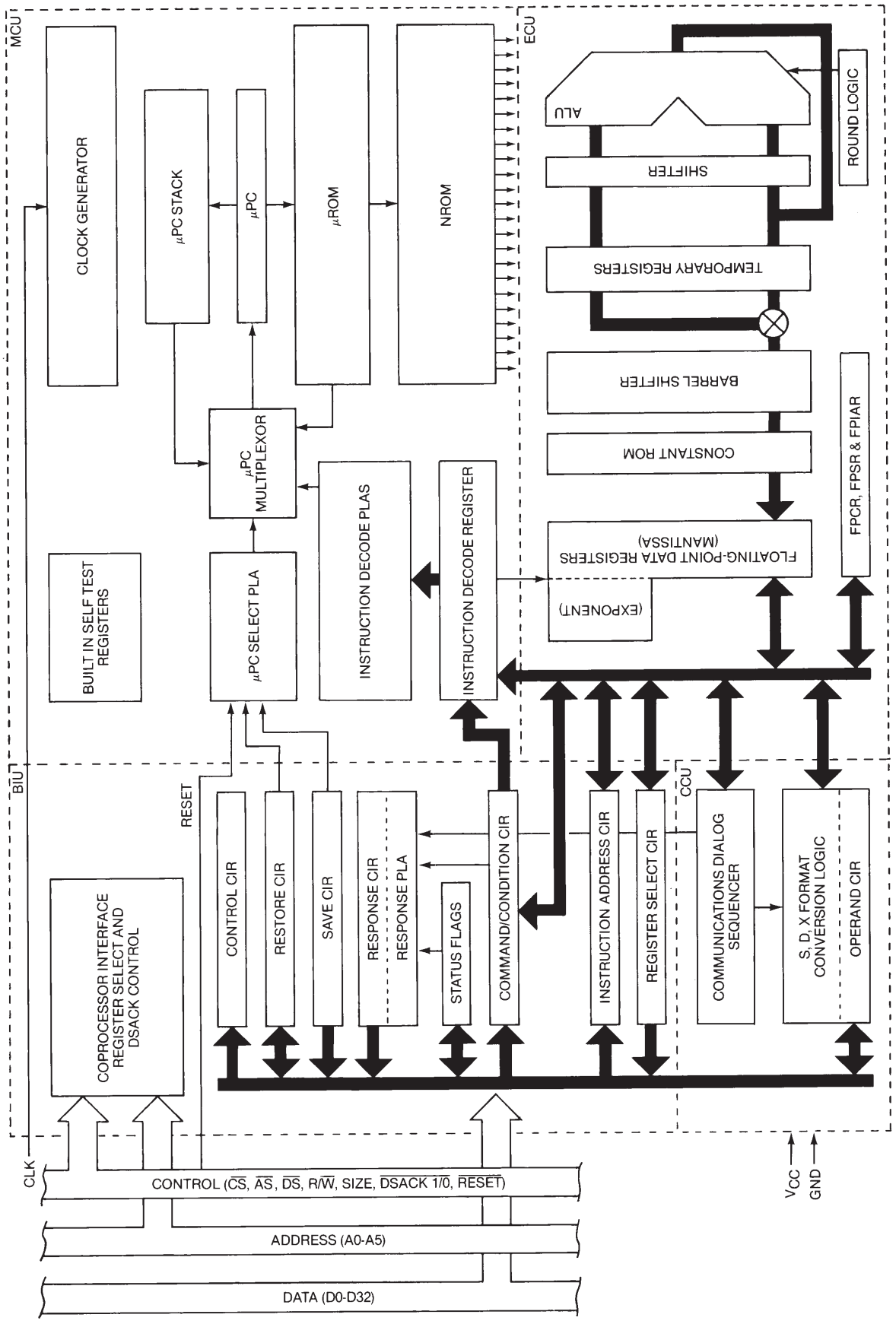
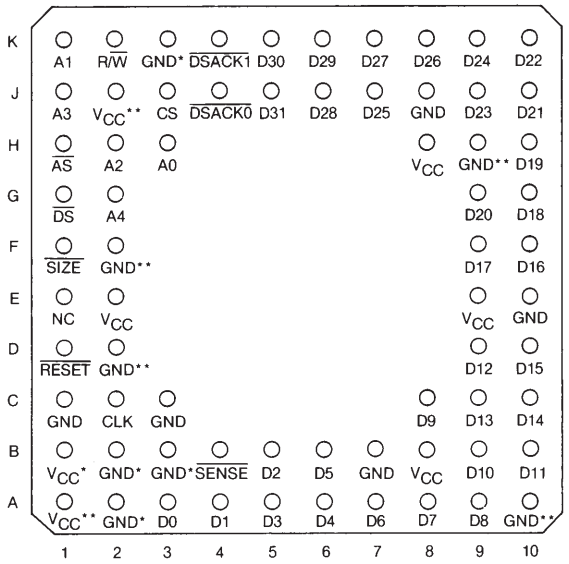


Figure 1 : TS 68882 simplified block diagram.

2 - PIN ASSIGNMENTS



Pin group	V_{CC}	GND
D31-D16	H8	J8
D15-D00	B8	B7
Internal logic $\overline{DSACK1}$, $\overline{DSACK0}$	E2, E9	A2, B2, B3, B4 (note), C3, E10, K3
Separate	—	C1
Extra	A1, B1, J2	A10, D2, F2, H9
Note : $\overline{SENSE}$ pin, may be used as an additional GND pin.		

* Reserved for future THOMSON use.

Figure 2.1. : PGA terminal designation.

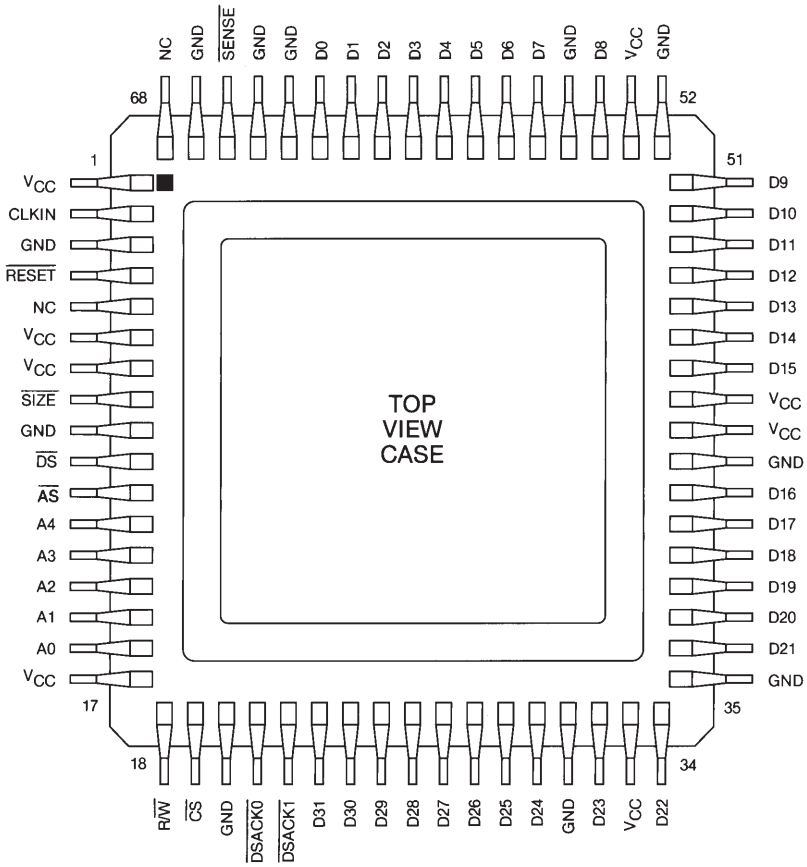
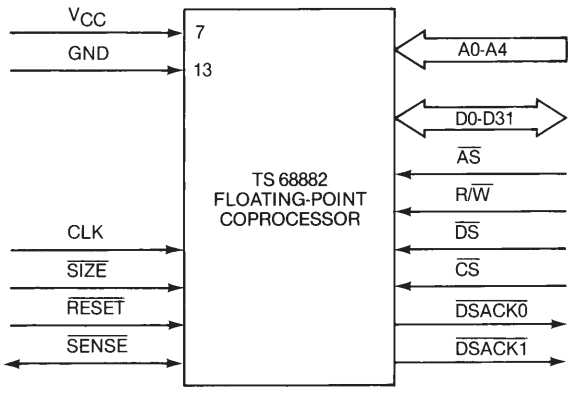


Figure 2.2. : CQFP terminal designation.

3 - FUNCTIONAL SIGNAL DESCRIPTIONS

This section contains a brief description of the input and output signals for the TS 68882 floating-point coprocessor. The signals are functionally organized into groups as shown in Figure 3.



Note : The terms assertion and negation are used extensively. This is done to avoid confusion when describing «active-low» and «active-high» signals. The term assert or assertion is used to indicate that a signal is active or true, independent of whether that level is represented by a high or low voltage. The term negate or negation is used to indicate that a signal is inactive or faise.

Figure 3 : TS 68882 input/output signals.

4 - SIGNAL SUMMARY

Table 1 provides a summary of all the TS 68882 signals described in this section.

Table 1 - Signal summary

Signal name	Mnemonic	Input / Output	Active state	Three state
Address bus	A0-A4	Input	High	
Data bus	D0-D13	Input / Output	High	Yes
Size	$\overline{SIZE}$	Input	Low	
Address strobe	$\overline{AS}$	Input	Low	
Chip select	$\overline{CS}$	Input	Low	
Read/Write	R/$\overline{W}$	Input	High / Low	
Data strobe	$\overline{DS}$	Input	Low	
Data transfer and size acknowledge	$\overline{DSACK0}$, $\overline{DSACK1}$	Output	Low	Yes
Reset	$\overline{RESET}$	Input	Low	
Clock	CLK	Input		
Sense device	$\overline{SENSE}$	Input / Output	Low	No
Power input	V_{CC}	Input		
Ground	GND	Input		

B - DETAILED SPECIFICATIONS

1 - SCOPE

This drawing describes the specific requirements for the microprocessor 68882, 16.67, 20 MHz and 25 MHz, in compliance with MIL-STD-883 class B or CECC 90000.

2 - APPLICABLE DOCUMENTS

2.1 - MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics.
2) MIL-PRF-38535 appendix A : general specifications for microcircuits.
3) Desc Drawing 5962 - 89436xxx.

2.2 - CECC 90000

1) CECC 90000.
2) Specification CECC 90110-024 for 16, 20 and 25 MHz.

3 - REQUIREMENTS

3.1 - General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 - Design and construction

3.2.1 - Terminal connections

Depending on the package, the terminal connections shall be is shown in Figures 2.1 and 2.2.

3.2.2 - Lead material and finish

Lead material and finish shall be any option of MIL-STD-1835.

3.2.3 - Package

The macrocircuits are packaged in hermetically sealed ceramic packages which are conform to case outlines of MIL-STD-1835 (when defined) :

- 68-PIN SQ.PGA UP PAE outline,
- 68-PIN Ceramic Quad Flat Pack CQFP.

The precise case outlines are described on Figures § 9.1 and 9.2.

3.3 · Electrical characteristics

3.3.1 · Absolute maximum ratings (see Table 2)

Table 2

Symbol	Parameter	Test conditions	Min	Max	Unit
V_{CC}	Supply voltage		−0.3	+7.0	V
V_I	Input voltage		−0.3	+7.0	V
P_{dmax}	Max Power dissipation	T_{case} = −55°C		2.0	W
		T_{case} = +125°C		1.9	W
T_{case}	Operating temperature	M suffix	−55	+125	°C
		V suffix	−40	+85	°C
T_{stg}	Storage temperature		−55	+150	°C
T_j	Junction temperature			160	°C
T_{leads}	Lead temperature	Max 5 sec. soldering		+270	°C

3.3.2 · Recommended condition of use

Unless otherwise stated, all voltages are referenced to the reference terminal (see Table 1).

Table 3 · DC electrical characteristics

V_{CC} = 5.0 V_{dc} ±10 % ; GND = 0 V_{dc} ; T_c = −55°C to +125°C

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply voltage		4.5	5.5	V
T_{case}	Operating temperature		−55	+125	°C
V_{IH}	Input high voltage		2.0	V_{CC}	V
V_{IL}	Input low voltage		GND −0.3	0.8	V
I_{IN}	Input leakage current @ 5.5 V	$\overline{CLK}$, $\overline{RESET}$, R/$\overline{W}$, A0-A4, $\overline{CS}$, $\overline{DS}$, $\overline{AS}$, $\overline{SIZE}$		10	µA
I_{TSI}	HI-Z (Off state) input current @ 2.4 V / 0.4 V	$\overline{DSACK0}$, $\overline{DSACK1}$, D0-D31		20	µA
V_{OH}	Output high voltage (I_{OH} = −400 µA) - Note 1	$\overline{DSACK0}$, $\overline{DSACK1}$, D0-D31	2.4		V
V_{OL}	Output low voltage (I_{OL} = 5.3 mA) - Note 1	$\overline{DSACK0}$, $\overline{DSACK1}$, D0-D31		0.5	V
I_{OL}	Output low current (V_{OL} = GND)	SENSE		500	µA
P_D	Power dissipation			0.75	W
C_{in}	Capacitance (V_{IN} = 0, T_A = 25°C, f = 1 MHz) - Note 2			20	pF
C_L	Output load capacitance			130	pF

Note 1 : Test load, see Figure 5.
Note 2 : Capacitance is periodically sampled rather than 100 % tested.

3.4 - Thermal characteristics

Table 4

Package	Symbol	Parameter	Value	Rating
PGA 68	θ_{JA}	Thermal resistance - Ceramic junction to ambient	33	°C/W
	θ_{JC}	Thermal resistance - Ceramic junction to case	4	°C/W
CQFP 68	θ_{JA}	Thermal resistance - Ceramic junction to ambient	33	°C/W
	θ_{JC}	Thermal resistance - Ceramic junction to case	3	°C/W

Power considerations

The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts – Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins – User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives :

$$K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θJ_C. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

3.5 - Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or CECC 90000 devices.

3.6 - Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

3.6.1 - Thomson logo

3.6.2 - Manufacturer's part number

3.6.3 - Class B identification

3.6.4 - Date-code of inspection lot

3.6.5 - ESD identifier if available

3.6.6 - Country of manufacturing

4 - QUALITY CONFORMANCE INSPECTION

4.1 - DESC / MIL-STD-883

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

4.2 - CECC

Is in accordance with CECC 90000. Group A and B inspection are performed on each production lot as specified in CECC 90110-024. Group C inspection is performed on a periodic basis in accordance with CECC 90110-024.

5 - ELECTRICAL CHARACTERISTICS

5.1 - General requirements

All static and dynamic electrical characteristics specified and the relevant measurement conditions are given below. For inspection purpose, refer to relevant specification :

- DESC see § 4.1
- CECC see § 4.2

Table 5 : Static electrical characteristics for all electrical variants. See § 5.2.

Table 6 : Dynamic electrical characteristics for 68882-16 (16.67 MHz), 68882-20 (20 MHz), 68882-25 (25 MHz) and 68882-33 (33 MHz). See § 5.3.

For static characteristics, test methods refer to clause 5.4.1 hereafter of this specification (Table 5).

For dynamic characteristics (Tables 6 and 7), test methods refer to IEC 748-2 method number, where existing, see § 5.4.2.

5.2 · Static characteristics

Table 5

V_{CC} = 5.0 V_{dc} ± 10 % ; GND = 0 V_{dc} ; T_C = −55 / +125°C or −40 / +85°C (see Figure 5)

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input high voltage	2.0	V_{CC}	V
V_{IL}	Input low voltage	GND −0.3	0.8	V
I_{IN}	Input leakage current @ 5.5 V CLK, $\overline{RESET}$, R/$\overline{W}$, A0-A4, $\overline{CS}$, $\overline{DS}$, $\overline{AS}$, $\overline{SIZE}$		10	µA
I_{TSI}	HI-Z (Off state) input current @ 2.4 V / 0.4 V $\overline{DSACK0}$, $\overline{DSACK1}$, D0-D31		20	µA
V_{OH}	Output high voltage (I_{OH} = −400 µA) - Note 1 $\overline{DSACK0}$, $\overline{DSACK1}$, D0-D31	2.4		V
V_{OL}	Output low voltage (I_{OL} = 5.3 mA) - Note 1 $\overline{DSACK0}$, $\overline{DSACK1}$, D0-D31		0.5	V
I_{OL}	Output low current (V_{OL} = GND) $\overline{SENSE}$		500	µA
P_D	Power dissipation		0.75	W
C_{in}	Capacitance (V_{IN} = 0, T_A = 25°C, f = 1 MHz) - Note 2		20	pF
C_L	Output load capacitance		130	pF

Note 1 : Test load, see Figure 5.
Note 2 : Capacitance is periodically sampled rather than 100 % tested.

5.3 · Dynamic (switching) characteristics

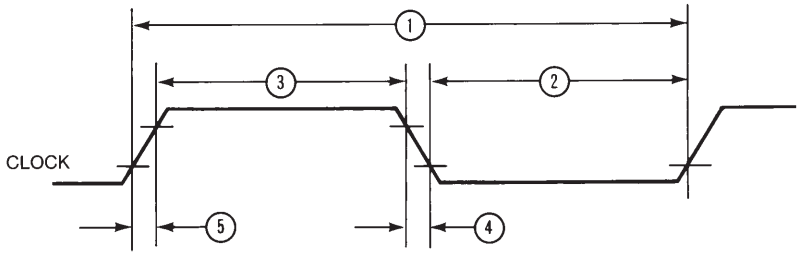
The limits and values given in this section apply over the full case temperature range −55°C to +125°C and V_{CC} in the range 4.5 V to 5.5 V, see § 5.4.2.

The numbers (N°) refer to the timing diagrams. See Figures 4, 6, 7, 8, and 9.

Table 6 · AC electrical characteristics · Clock input

V_{CC} = 5.0 V_{dc} ± 10 % ; GND = 0 V_{dc} ; T_C = −55°C to +125°C (see Figure 4)

N°	Parameter	16.67 MHz		20 MHz		25 MHz		33.33 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
	Frequency of operation	8	16.67	12.5	20	12.5	25	16.7	33.33	MHz
1	Clock time	60	125	50	80	40	80	30	60	ns
2, 3	Clock pulse width	24	95	20	54	15	59	14	66	ns
4, 5	Rise and fall times		5		5		4		3	ns



Note : Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside, and pass through, the range such that the rise or fall will be linear between 0.8 volts and 2.0 volts.

Figure 4 : Clock input timing diagram.

Table 7 - AC electrical characteristics - Read and write cycles
V_{CC} = 5.0 V_{dc} ± 10 % ; GND = 0 V_{dc} ; T_C = −55°C / +125°C or T_C = −40°C / +85°C (see Figures 7, 8, 9)

N°	Parameter	16.67 MHz		20 MHz		25 MHz		33.33 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
6	Address valid to $\overline{AS}$ asserted (see Note 5)	15		10		5		5		ns
6a	Address valid to $\overline{DS}$ asserted (read) (see Note 5)	15		10		5		5		ns
6b	Address valid to $\overline{DS}$ asserted (write) (see Note 5)	50		50		35		26		ns
7	$\overline{AS}$ negated to address invalid (see Note 6)	10		10		5		5		ns
7a	$\overline{DS}$ negated to address invalid (see Note 6)	10		10		5		5		ns
8	$\overline{CS}$ asserted to $\overline{AS}$ asserted or $\overline{AS}$ asserted to $\overline{CS}$ asserted (see Note 9)	0		0		0		0		ns
8a	$\overline{CS}$ asserted to $\overline{DS}$ asserted or $\overline{DS}$ asserted to $\overline{CS}$ asserted (read) (see Note 9)	0		0		0		0		ns
8b	$\overline{CS}$ asserted to $\overline{DS}$ asserted (write) (see Note 9)	30		25		20		15		ns
9	$\overline{AS}$ negated to $\overline{CS}$ negated	10		10		5		5		ns
9a	$\overline{DS}$ negated to $\overline{CS}$ negated	10		10		5		5		ns
10	R/$\overline{W}$ high to $\overline{AS}$ asserted (read)	15		10		5		5		ns
10a	R/$\overline{W}$ high to $\overline{DS}$ asserted (read)	15		10		5		5		ns
10b	R/$\overline{W}$ low to $\overline{DS}$ asserted (write)	35		30		25		25		ns
11	$\overline{AS}$ negated to R/$\overline{W}$ low (read) or $\overline{AS}$ negated to R/$\overline{W}$ high (write)	10		10		5		5		ns
11a	$\overline{DS}$ negated to R/$\overline{W}$ low (read) or $\overline{DS}$ negated to R/$\overline{W}$ high (write)	10		10		5		5		ns
12	$\overline{DS}$ width asserted (write)	40		38		30		23		ns
13	$\overline{DS}$ width negated	40		38		30		23		ns
13a	$\overline{DS}$ negated to $\overline{AS}$ asserted (see Note 4)	30		30		25		18		ns
14	$\overline{CS}$, $\overline{DS}$ asserted to data-out valid (read) (see Note 2)		80		45		45		30	ns
15	$\overline{DS}$ negated to data-out invalid (read)	0		0		0		0		ns
16	$\overline{DS}$ negated to data-out high impedance (read)		50		35		35		30	ns
17	Data-in valid to $\overline{DS}$ asserted (write)	15		10		5		5		ns
18	$\overline{DS}$ negated to data-in invalid (write)	15		10		5		5		ns
19	$\overline{START}$ true to $\overline{DSACK0}$ and $\overline{DSACK1}$ asserted (see Note 2)		50		35		25		20	ns
19a	$\overline{DSACK0}$ asserted to $\overline{DSACK1}$ asserted (skew) (see Note 7)	− 15	15	− 10	10	− 10	10		5	ns
20	$\overline{DSACK0}$ or $\overline{DSACK1}$ asserted to data-out valid		50		43		32		17	ns
21	$\overline{START}$ false to $\overline{DSACK0}$ and $\overline{DSACK1}$ negated (see Note 8)		50		30		40		30	ns

Table 7 - AC electrical characteristics - Read and write cycles (continued)
V_{CC} = 5.0 V_{dc} ± 10 % ; GND = 0 V_{dc} ; T_C = −55°C / +125°C or T_C = −40°C / +85°C (see Figures 7, 8, 9)

N°	Parameter	16.67 MHz		20 MHz		25 MHz		33.33 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
22	$\overline{START}$ false to $\overline{DSACK0}$ and $\overline{DSACK1}$ high impedance (see Note 8)		70		55		55		40	ns
23	$\overline{START}$ true to clock high (synchronous read) (see Notes 3 and 8)	0		0		0		0		ns
24	Clock low to data-out valid (synchronous read) (see Note 3)		105		80		60		45	ns
25	$\overline{START}$ true to data-out valid (synchronous read) (see Notes 3 and 8)	0 1.5	105 + 2.5	1.5	80 + 2.5	1.5	60 + 2.5	1.5	45 − 2.5	ns Clks
26	Clock low to $\overline{DSACK0}$ and $\overline{DSACK1}$ asserted (synchronous read) (see Note 3)		75		55		45		30	ns
27	$\overline{START}$ true to $\overline{DSACK0}$ and $\overline{DSACK1}$ asserted (synchronous read) (see Notes 3 and 8)	1.5	75 + 2.5	1.5	55 + 2.5	1.5	45 + 2.5	1.5	30 − 2.5	ns Clks

NOTES

Note 1 : Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside, and pass through, the range such that the rise or fall will be linear between 0.8 volts and 2.0 volts.

Note 2 : These specifications only apply if the TS 68882 has completed all internal operations initiated by the termination of the previous bus cycle when $\overline{DS}$ was negated.

Note 3 : Synchronous read cycles occur *only* when the save or response CIR locations are read.

Note 4 : This specification only applies to systems in which back-to-back accesses (read-write or write-write) of the operand CIR can occur. When the TS 68882 is used as a coprocessor to the TS 68020 / 68030, this can occur when the addressing mode is immediate.

Note 5 : If the $\overline{SIZE}$ pin is *not* strapped to either V_{CC} or GND, it must have the same setup times as do addresses.

Note 6 : If the $\overline{SIZE}$ pin is *not* strapped to either V_{CC} or GND, it must have the same hold times as do addresses.

Note 7 : This number is reduced to 5 nanoseconds if $\overline{DSACK0}$ and $\overline{DSACK1}$ have equal loads.

Note 8 : $\overline{START}$ is not an external signal ; rather, it is the logical condition that indicates the start of an access. The logical equation for this condition is $\overline{START}$, $\overline{CS}$, $\overline{AS}$, R/$\overline{W}$-$\overline{DS}$.

Note 9 : If a subsequent access is not a FPCP access, $\overline{CS}$ must be negated before the assertion of $\overline{AS}$ and or $\overline{DS}$ on the non-FPCP access. These specifications replace the old specifications 8 and 8A (the old specifications implied that in all cases, transitions in $\overline{CS}$ must not occur simultaneously with transitions of $\overline{AS}$ or $\overline{DS}$. This is not a requirement of the TS 68882).

5.4 · Test conditions specific to the device

5.4.1 · Test load

The applicable loading network shall be as defined in column «Test conditions» of Table 6, refering to the loading network number as shown in Figure 5.

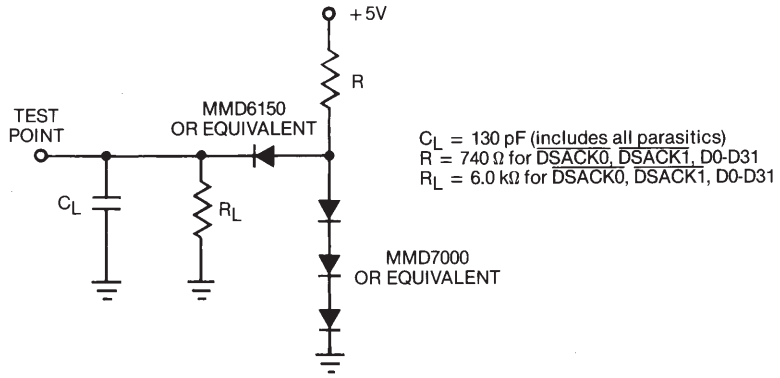


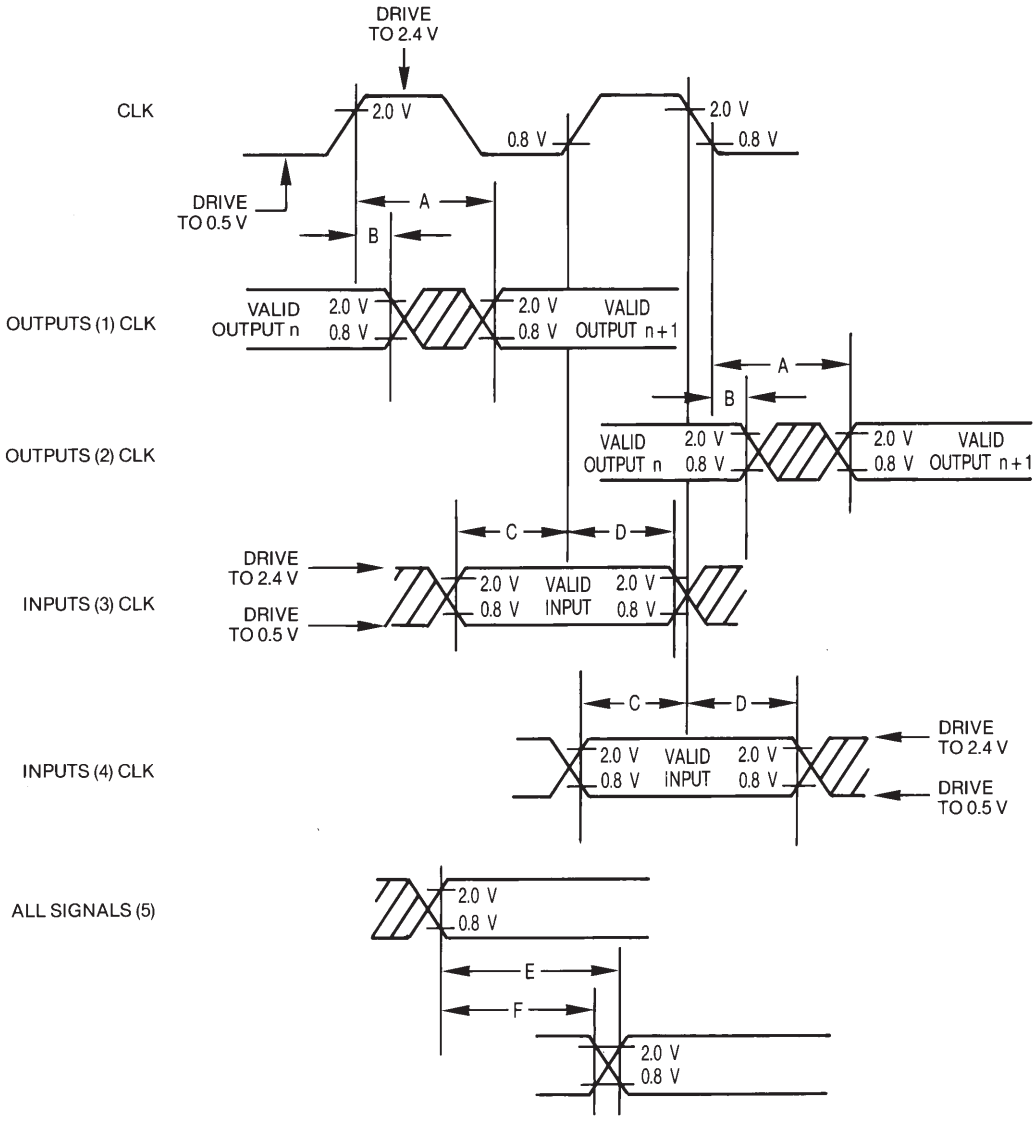
Figure 5 : Test loads.

5.4.2 · AC electrical specification definitions

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the clock input and, possibly, relative to one or more other signals.

The measurement of the AC specfifications is defined by the waveforms shown in Figure 6. In order to test the parameters guaranteed by THOMSON inputs must be driven to the voltage levels specified in Figure 6. Outputs are specified with minimum and/or maximum limits, as appropriate, and are measured as shown. Inputs are specified with minimum and, ans appropriate maximum setup and hold times, and are measured as shown. Finally, the measurement for signal-to-signal specifications are also shown.

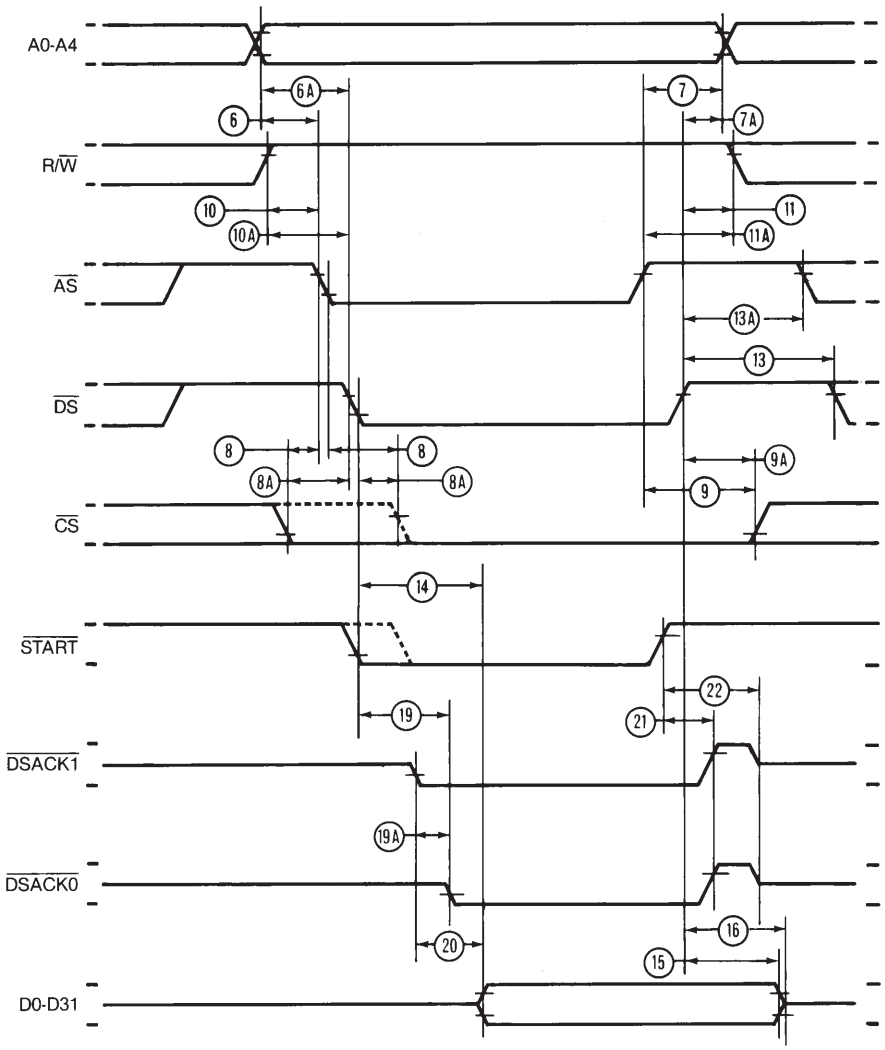
Note that the testing levels used to verify conformance to the AC specifications does not affect the guaranteed DC operation of the device as specified in the DC electrical characteristics.



Legend : A. Maximum output delay specification.
B. Minimum output hold time.
C. Minimum input setup time specification.
D. Minimum input hold time specification.
E. Signal valid to signal valid specification (maximum or minimum).
F. Signal valid to signal invalid specification (maximum or minimum).

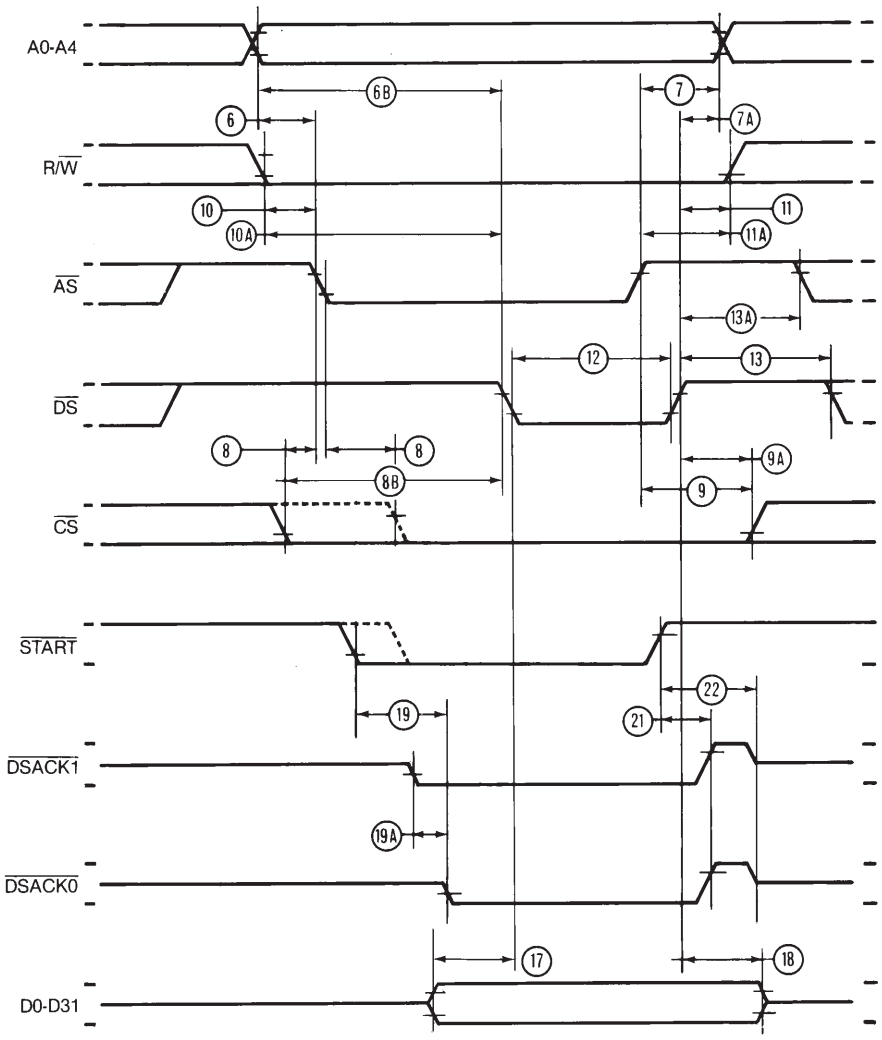
Notes : 1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This output timing is applicable to all parameters specified relative to the failing edge of the clock.
3. This input timing is applicable to all parameters specified relative to the raising edge of the clock.
4. This input timing is applicable to all parameters specified relative to the failing edge of the clock.
5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

Figure 6 : Drive levels and test points for AC specifications.



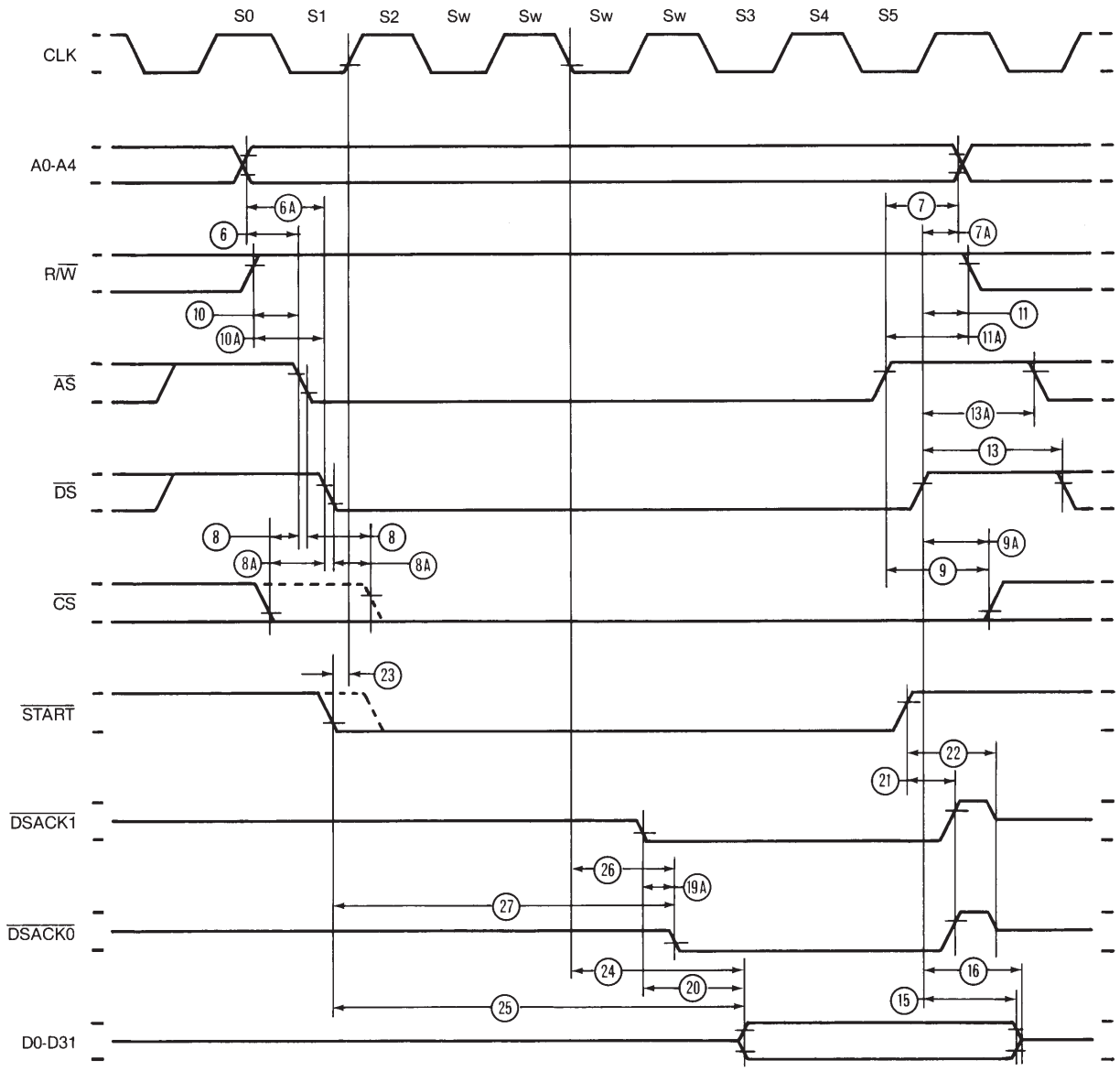
Note : $\overline{START}$ is actually a logical condition, but is shown as an active signal for clarity. The logical equation for this signal is :
$\overline{START} = \overline{CS} + \overline{AS} + (R/\overline{W} \bullet \overline{DS})$.

Figure 7 : Asynchronous read cycle timing diagram.



Note : $\overline{START}$ is actually a logical condition, but is shown as an active signal for clarity. The logical equation for this signal is :
$\overline{START} = \overline{CS} + \overline{AS} + (R/\overline{W} \bullet \overline{DS})$.

Figure 8 : Asynchronous write cycle timing diagram.



Note : $\overline{START}$ is actually a logical condition, but is shown as an active signal for clarity. The logical equation for this signal is :
$\overline{START} = \overline{CS} + \overline{AS} + (R/\overline{W} \bullet \overline{DS})$.

Figure 9 : Synchronous read cycle timing diagram.

5.5 - Additional information

Additional information shall not be for any inspection purposes.

5.5.1 - Power considerations (see § 3.4)

5.5.2 - Capacitance (Not for inspection purposes)

Symbol	Parameter	Test conditions	Min	Max	Unit
C_{in}	Input capacitance	$V_{in} = 0$ $T_{amb} = 25°C$ $f = 1$ MHz		20	pF

6 - FUNCTIONNAL DESCRIPTION

The coprocessor concept

The TS 68882 functions as a coprocessor in systems where the TS 68020 or TS 68030 is the main processor via the TS 68000 coprocessor interface. It functions as a peripheral processor in systems where the main processor is the TS 68000, TS 68010

The TS 68882 utilizes the TS 68000 Family coprocessor interface to provide a logical extension of the TS 68020 / TS 68030 registers and instruction set in a manner which is transparent to the programmer. The programmer perceives the MPU / FPCP execution model as if both devices are implemented on one chip.

A fundamental goal of the TS 68000 Family coprocessor interface is to provide the programmer with an execution model based upon sequential instruction execution by the TS 68020 / TS 68030 and the TS 68882. For optimum performance, however, the coprocessor interface allows concurrent operations in the TS 68882 with respect to the TS 68020 / TS 68030 whenever possible. In order to simplify the programmer's model, the coprocessor interface is designed to emulate, as closely as possible, non-concurrent operation between the TS 68020 / TS 68030 and the TS 68882.

The TS 68882 is a non-DMA type coprocessor which uses a subset of the general purpose coprocessor interface supported by the TS 68020 / TS 68030. Features of the interface implemented in the TS 68882 are as follows :

- The main processor(s) and TS 68882 communicate via standard TS 68000 bus cycles.
- The main processor(s) and TS 68882 communications are not dependent upon the instruction sets or internal details of the individual devices (e.g., instruction pipes or caches, addressing modes).
- The main processor(s) and TS 68882 may operate at different clock speeds.
- TS 68882 instructions utilize all addressing modes provided by the main processor ; all effective addresses are calculated by the main processor at the request of the coprocessor.
- All data transfers are performed by the main processor at the request of the TS 68882 ; thus memory management, bus errors, address errors, and bus arbitration function as if the TS 68882 instructions are executed by the main processor.
- Overlapped (concurrent) instruction execution enhances throughput while maintaining the programmer's model of sequential instruction execution.
- Coprocessor detection of exceptions which require a trap to be taken are serviced by the main processor at the request of the TS 68882 thus exception processing functions as if the TS 68882 instructions were executed by the main processor.
- Support of virtual memory / virtual machine systems is provided via the FSAVE and FRESTORE instructions.
- Up to eight coprocessors may reside in a system simultaneously ; multiple coprocessors of the same type are also allowed.
- Systems may use software emulation of the TS 68882 without reassembling or relinking user software.

The TS 68882 programming model is shown in Figures 10 through 15, and consists of the following :

- Eight 80-bit floating-point data registers (FP0-FP7). These registers are analogous to the integer data registers (D0-D7) and are completely general purpose (i.e., any instruction may use any register).
- A 32-bit control register that contains enable bits for each class of exceptions trap, and mode bits to set the user-selectable rounding and precision modes.
- A 32-bit status register that contains floating-point condition codes, quotient bits, and exception status information.
- A 32-bit instruction address register that contains the main processor memory address of the last floating-point instruction that was executed. This address is used in exception handling to locate the instruction that caused the exception.

The connection between the TS 68020 / TS 68030 and the TS 68882 is a simple extension of the TS 68000 bus interface. The TS 68882 is connected as a coprocessor to the TS 68020 / TS 68030, and the selection of the TS 68882 is based upon a chip select (CS), which is decoded from the TS 68020 / TS 68030 function codes and address bus. Figure 16 illustrates the TS 68882 / TS 68020 or TS 68030 configuration.

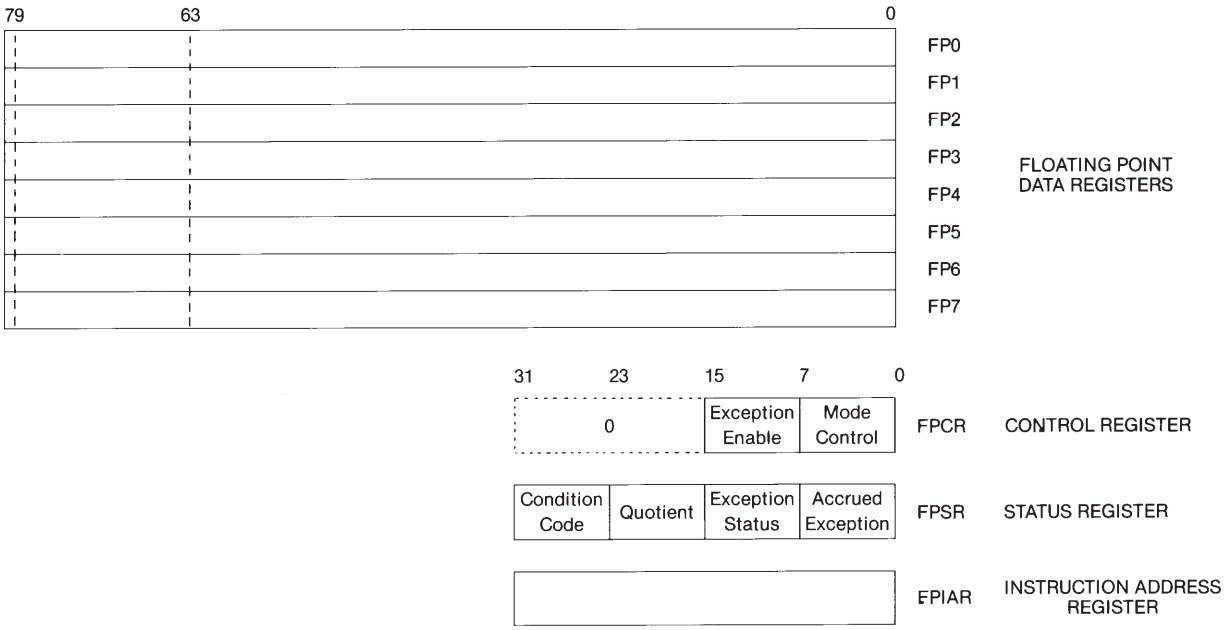


Figure 10 : TS 68882 programming model.

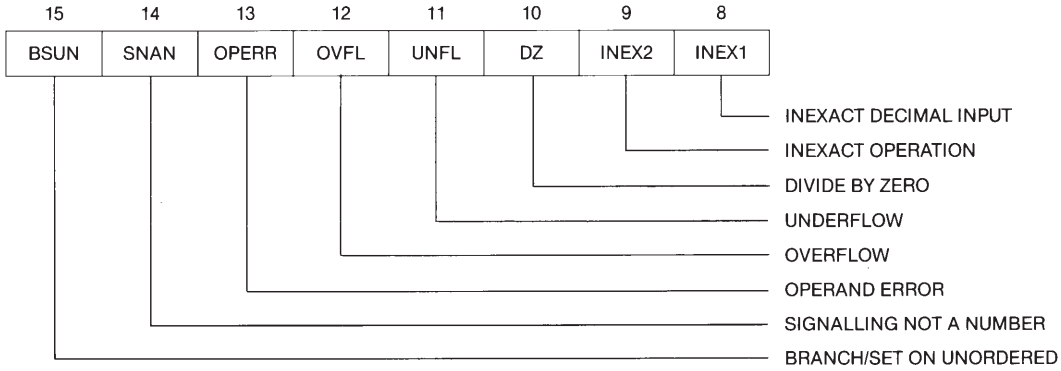


Figure 11 : Exception status/enable byte.

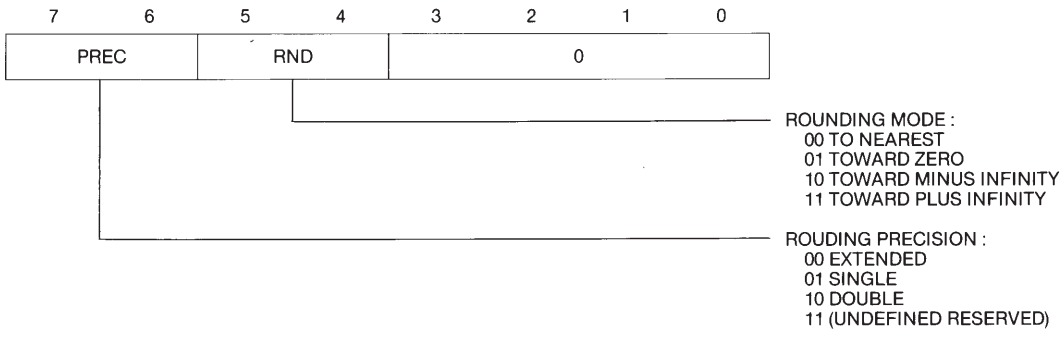


Figure 12 : Mode control byte.

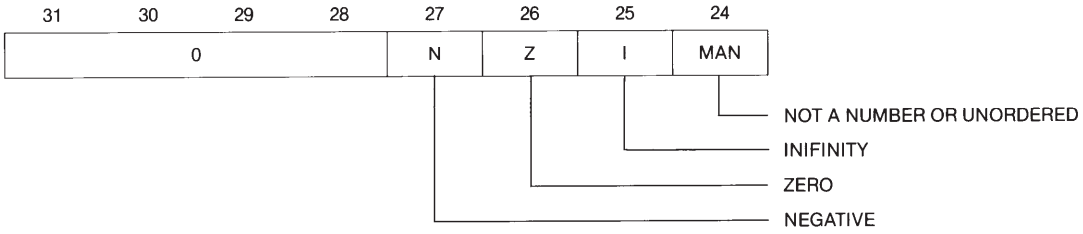


Figure 13 : Condition code byte.

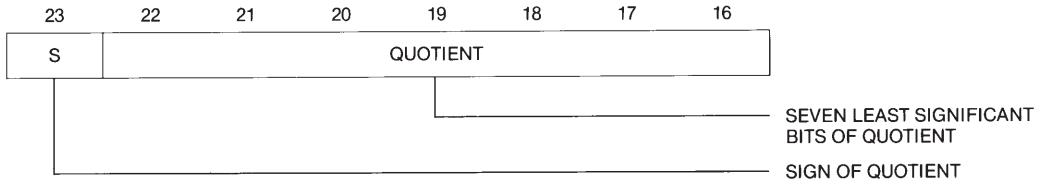


Figure 14 : Quotient byte.

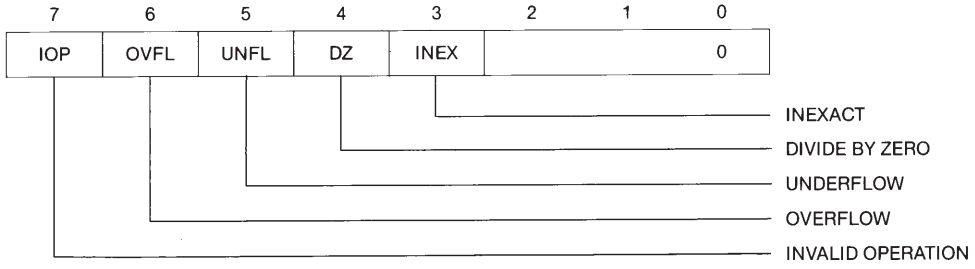


Figure 15 : Accrued exception byte.

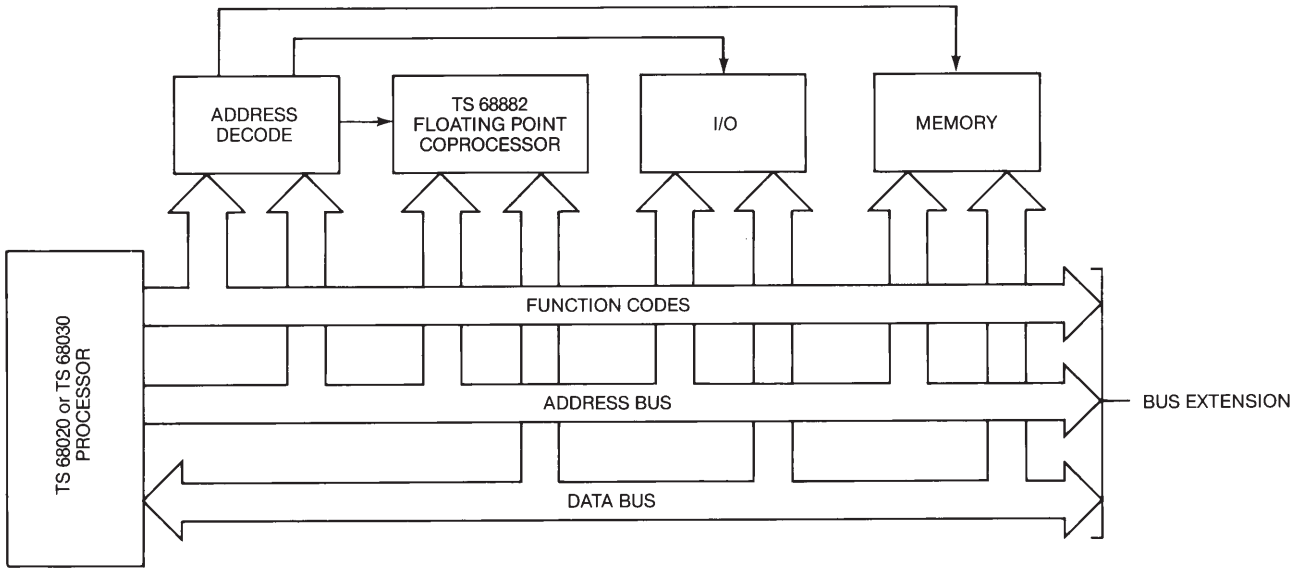


Figure 16 : Typical coprocessor configuration.

Bus interface unit

All communications between the TS 68020 / TS 68030 and the TS 68882 occur via standard TS 68000 Family bus transfers. The TS 68882 is designed to operate on 8-, 16-, or 32-bit data buses.

The TS 68882 contains a number of coprocessor interface registers (CIRs) which are addressed in the same manner as memory by the main processor. The TS 68000 Family coprocessor interface is implemented via a protocol of reading and writing to these registers by the main processor. The TS 68020 and TS 68030 implements this general purpose coprocessor interface protocol in hardware and microcode.

When the TS 68020 / TS 68030 detects a typical TS 68882 instruction, the MPU writes the instruction to the memorymapped command CIR, and reads the response CIR. In this response, the BIU encodes requests for any additional action required of the MPU on behalf of the TS 68882. For example, the response may request that the MPU fetch an operand from the evaluated effective address and transfer the operand to the operand CIR. Once the MPU fulfills the coprocessor request(s), it is free to fetch and execute subsequent instructions.

A key concern in a coprocessor interface that allows concurrent instruction execution is synchronization during main processor and coprocessor communication. If a subsequent instruction is written to the TS 68882 before the CCU has passed the operands for the previous instructions to the ECU, the response instructs the TS 68020 / TS 68030 to wait. Thus, the choice of concurrent or nonconcurrent instruction execution is determined on an instruction-by-instruction basis by the coprocessor.

The only difference between a coprocessor bus transfer and any other bus transfer is that the TS 68020 / TS 68030 issues a function code to indicate the CPU address space during the cycle (the function codes are generated by the TS 68000 Family processors to identify eight separate address spaces). Thus, the memory-mapped coprocessor interface registers do not infringe upon instruction or data address spaces. The TS 68020 / TS 68030 places a coprocessor ID field from the coprocessor instruction onto three of the upper address lines during coprocessor accesses. This ID, along with the CPU address space function code, is decoded to select one of eight coprocessors in the system.

Since the coprocessor interface protocol is based solely on bus transfers, the protocol is easily emulated by software when the TS 68882 is used as a peripheral with any processor capable of memory-mapped I/O over on TS 68000 style bus. When used as a peripheral processor with the 8-bit TS 68008 or the 16-bit TS 68000, or TS 68010, all TS 68882 instructions are trapped by the main processor to an exception handler at execution time. Thus, the software emulation of the processor interface protocol can be totally transparent to the user. The system can be quickly upgraded by replacing the main processor with an TS 68020 TS 68030 without changes to the user software.

Since the bus is asynchronous, the TS 68882 need not run at the same clock speed as the main processor. Total system performance may therefore be customized. For example, a system requiring very fast floating-point arithmetic with relatively slow integer arthmetic can be designed with an inexpensive main processor and a fast TS 68882.

Coprocessor interface

The TS 68000 Family coprocessor interface is an integral part of the TS 68882 and TS 68020 TS 68030 designs, with the interface tasks shared between the two. The interface is fully compatible with all present and future TS 68000 Family products. Tasks are partitioned such that the TS 68020 TS 68030 does not have to decode coprocessor instructions and, the TS 68882 does not have to duplicate main processor functions such as effective address evaluation.

This partitioning provides an orthogonal extension of the instruction set by permitting TS 68882 instructions to utilize all TS 68020 / TS 68030 addressing modes and to generate execution time exception traps. Thus, from the programmer's view, the CPU and coprocessor appear to be integrated onto a single chip. While the execution of the majority of TS 68882 instructions may be overlapped with the execution of TS 68020 / TS 68030 instructions, concurrency is completely transparent to the programmer. The TS 68020 / TS 68030 single-step and program flow (trace) modes are fully supported by the TS 68882 and the TS 68000 Family coprocessor interface.

While the TS 68000 Family coprocessor interface permits coprocessors to be bus masters, the TS 68882 is never a bus master. The TS 68882 requests that the TS 68020 / TS 68030 fetch all operands and store all results. In this manner, the TS 68020 / TS 68030 32-bit data bus provides high speed transfer of floating-point operands and results while simplifying the design of the TS 68882.

Since the coprocessor interface is based solely upon bus cycles and the TS 68882 is never a bus master, the TS 68882 can be placed on either the locical or physical side of the system memory management unit. This provides a great deal of flexibility in the system design.

The virtual machine architecture of the TS 68000 Family is supported by the coprocessor interface and the TS 68882 through the FSAVE and FRESTORE instructions. If the TS 68020 / TS 68030 detects a page fault and/or task time out, it can force the TS 68882 to stop whatever operation is in process at any time (even in the middle of the execution of an instruction) and save the TS 68882 internal state in memory.

The size of the saved internal state of the TS 68882 is dependent upon what the CCU and ECU are doing at the time that the FSAVE is executed. If the TS 68882 is in the reset state when the FSAVE instruction is received, only one word of state is transferred to memory, which may be examined by the operating system to determine that the coprocessor programmer's model is empty. If the coprocessor is idle when the save instruction is received, only a few words of internal state are transferred to memory. If the TS 68882 is in the middle of performing a calculation, it may be necessary to save the entire internal state of the machine. Instructions that can complete execution in less time than it would take to save the larger state in mid-instruction are allowed to complete execution and then save the idle state. Thus the size of the saved internal state is kept to a minimum. The ability to utilize several internal state sizes greatly reduces the average context switching time.

The FRESTORE instruction permits reloading of an internal state that was saved earlier, and continues any operation that was previously suspended. Restoring of the reset internal state functions just like a hardware reset to the TS 68882 in that defaults are re-established.

Note : Though the TS 68882 is instruction set compatible with the TS 68881, the idle and busy state frames are both 32 bytes larger on the TS 68882 than on the TS 68881. A unique format word is generated by the TS 68882 so that system software can detect this difference.

Operand data formats

The TS 68882 supports the following data formats :

Byte Integer (B)

Word Integer (W)

Long Word Integer (L)

Single Precision Real (S)

Double Precision Real (D)

Extended Precision Real (X)

Packed Decimal String Real (P)

The capital letters contained in parenthesis denote suffixes added to instructions in the assembly language source to specify the data format to be used.

Integer data formats

The three integer data formats (byte, word, and long word) are the standard data formats supported in the TS 68000 Family architecture. Whenever an integer is used in a floating-point operation, the integer is automatically converted by the TS 68882 to an extended precision floating-point number before being used. For example, to add an integer constant of five to the number contained in floating-point data register 3 (FP3), the following instruction can be used :

FADD.W #5.FP3

The ability to effectively use integers in floating-point operations saves user memory since an integer representation of a number, if respresentable, is usually smaller than the equivalent floating-point representation.

Floating-point data formats

The floating-point data formats single precision (32-bits) and double precision (64-bits) are as defined by the IEEE standard. These are the main floating-point formats and should be used for most calculations involving real numbers. Table 8 lists the exponent and mantissa size for single, double, and extended precision. The exponent is biased, and the mantissa is in sign and magnitude form. Since single and double precision require normalized numbers, the most significant bit of the mantissa is implied as one and is not included, thus giving one extra bit of precision.

Table 8 - Exponent and Mantissa sizes

Data Format	Exponent bits	Mantissa bits	Bias
Single	8	23 (+ 1)	127
Double	11	52 (+ 1)	1023
Extended	15	64	16383

The extended precision data format is also in conformance with the IEEE standard, but the standard does not specify this format to the bit level as it does for single and double precision. The memory format on the TS 68882 consists of 96 bits (three long words). Only 80 bits are actually used, the other 16 bits are for future expandability and for long-word alignment of floating-point data structures. Extended format has a 15-bit exponent, a 64-bit mantissa, and a 1-bit mantissa sign.

Extended precision numbers are intended for use as temporary variables, intermediate values, or in places where extra precision is needed. For example, a compiler might select extended precision arithmetic for evaluation of the right side of an equation with mixed sized data and then convert the answer to the data type on the left side of the equation. It is anticipated that extended precision data will not be stored in large arrays, due to the amount of memory required by each number.

Packed decimal string real data format

The packed decimal data format allows packed BCD strings to be input to and output from the TS 68882. The strings consist of a 3-digit base 10 exponent and 17-digit base 10 mantissa. Both the exponent and mantissa have a separate sign bit. All digits are packed BCD, such that an entire string fits in 96 bits (three long words). As is the case with all data formats, when packed BCD strings are input to the TS 68882, the strings are automatically converted to extended precision real values. This allows packed BCD numbers to be used as inputs to any operation. For example :

FADD.P # − 6.023E + 24, FP5

BCD numbers can be output from the TS 68882 in a format readily used for printing by a program generated by a high-level language compiler. For example :

FMOVE.P FP3.BUFFER (# – 5)

instructs the TS 68882 to convert the floating-point data register 3 (FP3) contents into a packed BCD string with five digits to the right of the decimal point (FORTRAN F format).

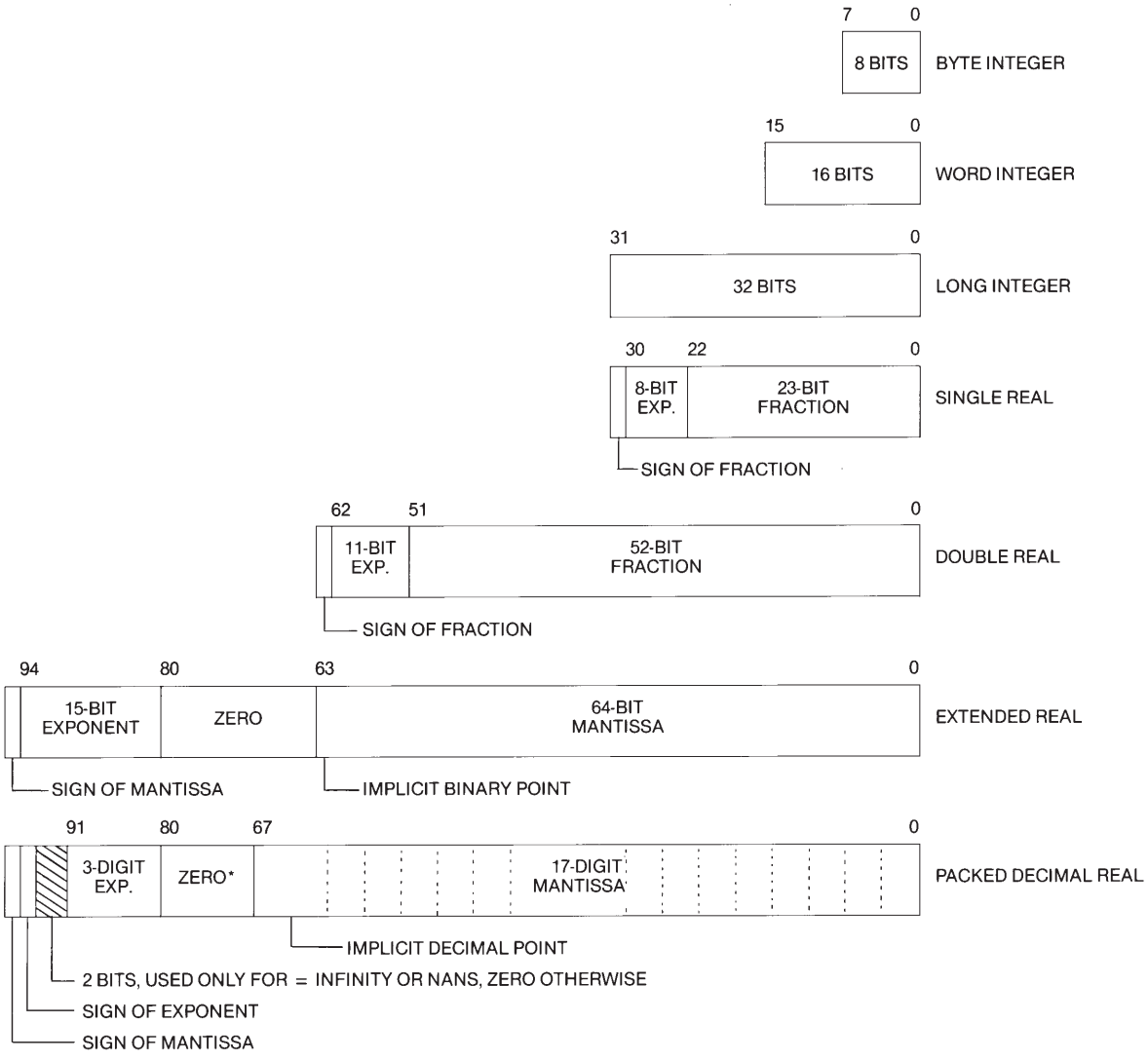
Data format summary

All data formats described above are supported ortrhogonally by all arithmetic and transcendental operations, and by all appropriate TS 68000 Family addressing modes. For example, all of the following are legal instructions :

```
FADD.B    #3.FP0
FADD.W    D2.FP3
FADD.L    BIGINT.FP7
FADD.S    #3.14159.FP5
FADD.D    (SP)+.FP6
FADD.X    [(TEMP – PTR.A7)].FP3
FADD.P    #1.23E25.FP0
```

On-chip calculations are performed to extended precision format, and the eight floating point data registers always contain extended precision values. All data used in an operation is converted to extended precision by the TS 68882 before the specific operation is performed, and all results are in extended precision. This ensures maximum accuracy without sacrificing performance.

Refer to Figure 17 for a summary of the memory formats for the seven data formats supported by the TS 68882.



* Unless a binary-to-decimal conversion overflow occurs.

Figure 17 : TS 68882 data format summary.

Instruction set

The TS 68882 instruction set is organized into six major classes :

1. Moves between the TS 68882 and memory or the MPU (in and out).
2. Move multiple registers (in and out).
3. Monadic operations.
4. Dyadic operations.
5. Branch, set, or trap conditionally, and
6. Miscellaneous.

Moves

All moves from memory (or from an MPU data register) to the TS 68882, cause data conversion from the source data format to the internal extended precision format.

All moves from the TS 68882 to memory (or to an MPU data register), cause data conversion from the internal extended precision format to the destination data format.

Note that data movement instructions perform arithmetic operations, since the result is always rounded to the precision selected in the FPCR mode control byte. The result is rounded using the selected rounding mode, and is checked for overflow and underflow.

The syntax for the move is :

FMOVE.(fmt)	(ea).FPn	Move to TS 68882
FMOVE.(fmt)	FPm.(ea)	Move from TS 68882
FMOVE.X	FPm.FPn	Move within TS 68882

where :

(ea) is an TS 68000 Family effective address operand and (fmt) is the data format size. FPm and FPn are floating-point data registers.

Move multiples

The floating-point move multiple instructions on the TS 68882 are much like the integer counterparts on the TS 68000 Family processors. Any set of the floating-point registers FP0 through FP7 can be moved to or from memory with one instruction. These registers are always moved as 96-bit extended data with no conversion (hence no possibility of conversion errors). Some move multiple examples are as follows :

FMOVEM	(ea),FP0-FP3/FP7
FMOVEM	FP2/FP4/FP6,(ea)

Move multiples are useful during context switches and interrupts to save or restore the state of a program. These moves are also useful at the start and end of a procedure to save and restore the calling routine's register set. In order to reduce procedure call overhead, the list of registers to be saved or restored can be contained in a data register. This allows run-time iptimization by allowing a called routine to save as few registers as possible. Note that no rounding or overflow/underflow checking is performed by these operations.

Monadic operations

Monadic operations have one operand. This operand may be in a floating-point data register, memory, or in an MPU data register. The result is always stored in a floating-point data register. For example, the synthax for square root is :

FSQRT.(fmt)	(ea),FPN or,
FSQRT.X	FPm,FPn or,
FSQRT.X	FPn

The TS 68882 monadic operations available are as follows :

FABS	Absolue Value
FACOS	Arc Cosine
FASIN	Arc Sine
FATAN	Arc Tangent
FATANH	Hyperbolic Arc Tangent
FCOS	Cosine
FCOSH	Hyperbolic Cosine
FETOX	e to the x Power
FETOXM1	e to the x Power – 1
FGETEXP	Get Exponent
FGETMAN	Get Mantissa
FINT	Integer Part
FINTRZ	Integer Part (Truncated)
FLOG10	Log Base 10
FLOG2	Log Base 2
FLOGN	Log Base e
FLOGNP1	Log Base e of(x + 1)
FNEG	Negate
FSIN	Sine
FSINCOS	Simultaneous Sine and Cosine
FSINH	Hyperbolic Sine
FSQRT	Square Root
FTAN	Tangent
FTANH	Hyperbolic Tangent
FTENTOX	10 to the x Power
FTST	test
FTWOTOX	2 to the x Power

Dyadic operations

Dyadic operations have two input operands. The first input operand comes from a floating-point data register, memory, or MPU data register. The second input operand comes from a floating-point data register. The destination is the same floating-point data register used for the second input. For example, the syntax for add is :

FADD.(fmt)	(ea).FPn or,
FADD.X	FPm.FPn

The TS 68882 dyadic operations available are as follows :

FADD	Add
FCMP	Compare
FDIV	Divide
FMOD	Modulo Remainder
FMUL	Multiply
FREM	IEEE Remainder
FSCALE	Scale Exponent
FSGLDIV	Single Precision Divide
FSGLMUL	Single Precision Multiply
FSUB	Subtract

Branch, set, and trap-on condition

The floating-point branch, set, and trap-on condition instructions implemented by the TS 68882 are similar to the equivalent integer instructions of the TS 68000 Family processors, except that more conditions exist due to the special values in IEEE floating-point arithmetic. When a conditional instruction is executed, the TS 68882 performs the necessary condition checking and tells the MPU whether the condition is true or faise ; the MPU then takes the appropriate action. Since the TS 68882 and TS 68020 / TS 68030 are closely coupled, the floating-point branch operations executed by the pair are very fast.

The TS 68882 conditional operations are :

FBcc	Branch
FDBcc	Decrement and Branch
FScc	Set Byte According to Condition
FTRAPcc	Trap-on Condition (with an Optional Parameter)

where :

cc is one of the 32 floating-point conditional test specifiers as shown in Table 9.

Table 9 - Floating-point conditional test specifiers

Mnemonic	Definition
Note : The following conditional tests do not set the BSUN bit in the status register exception byte under any circumstances.	
F	False
EQ	Equal
OGT	Ordered Greater Than
OGE	Ordered Greater Than or Equal
OLT	Ordered Less Than
OLE	Ordered Less Than or Equal
OGL	Ordered Greater or Less Than
OR	Ordered
UN	Unordered
UEQ	Unordered or Equal
UGT	Unordered or Greater Than
UGE	Unordered or Greater or Equal
ULT	Unordered or Less Than
ULE	Unordered or Less or Equal
NE	Not Equal
T	True
Note : The following conditional tests set the BSUN bit in the status register exception byte if the NAN condition code bit is set when a conditional instruction is executed.	
SF	Signaling False
SEQ	Signaling Equal
GT	Greater Than
GE	Greater Than or Equal
LT	Less Than
LE	Less Than or Equal
GL	Greater or Less Than
GLE	Greater Less or Equal
NGLE	Not (Greater, Less or Equal)
NGL	Not (Greater or Less)
NLE	Not (Less or Equal)
NLT	Not (Less Than)
NGE	Not (Greater or Equal)
NGT	Not (Greater Than)
SNE	Signaling Not Equal
ST	Signaling True

Miscellaneous instructions

Miscellaneous instructions include moves to and from the status, control, and instruction address registers and a no operation function that can be used to «flush» exceptions. Also included are the virtual memory/machine FSAVE and FRESTORE instructions that save and restore the internal state of the TS 68882.

FMOVE	(ea), FPcr	Move to Control Register(s)
FMOVE	FPcr, (ea)	Move from Control Register(s)
FNOP		No Operation
FSAVE	(ea)	Virtual Machine State Save
FRESTORE	(ea)	Virtual Machine State Restore

Addressing modes

The TS 68882 does not perform address calculations. This satifies the criterion that an TS 68000 Family coprocessor must not depend on certain features or capabilities that may or may not be implemented by a given main processor. Thus, when the. TS 68882 instructs the TS 68020 / TS 68030 to transfer an operand via the coprocessor interface, the MPU performs the addressing mode calculations requested in the instruction. In this case, the instruction is encoded specifically for the TS 68020 / TS 68030, and the execution of the TS 68882 is not dependent on that encoding, but only on the value of the command word written to the TS 68882 by the main processor.

This interface is quite flexible and allows any addressing mode to be used with floating-point instructions. For the TS 68000 Family, these addressing modes includ immediate, postincrement, predecrement, data or address register direct, and the indexed/indirect addressing modes of the TS 68020 / TS 68030. Some addressing modes are restricted for some instructions in keeping with the TS 68000 Family architectural definitions (e.g. PC relative addressing is not allowed for a destination operand).

The orthogonal instruction set of the TS 68882, along with the flexible branches and addressing modes, allows a programmer writing assembly language code, or a compiler writer generating object or source code for the MPU / TS 68882 device pair, to think of the TS 68882 as though it is part of the MPU. There are no special restrictions imposed by the coprocessor interface, and floating-point arithmetic is coded exactly like integer arithmetic.

Address bus (A0 through A4)

These active-high address line inputs are used by the main processor to select the coprocessor interface register locations located in the CPU address space. These lines control the register selection as listed in Table 10.

When the TS 68882 is configured to operate over an 8-bit data bus, the A0 pin is used as an address signal for byte acceses of the coprocessor interface registers. When the TS 68882 is configured to operate over a 16- or 32-bit system data bus, both the A0 and SIZE pins are stapped high and/or low as listed in Table 11.

Table 10 - Coprocessor interface register selection

A4-A0	Offset	Width	Type	Register
0000x	S00	16	Read	Response
0001x	S02	16	Write	Control
0010x	S04	16	Read	Save
0011x	S06	16	R/W	Restore
0100x	S08	16	—	(Reserved)
0101x	S0A	16	Write	Command
0110x	S0C	16	—	(Reserved)
0111x	S0E	16	Write	Condition
100xx	S10	32	R/W	Operand
1010x	S14	16	Read	Register select
1011x	S16	16	—	(Reserved)
110xx	S18	32	Read	Instruction Address
111xx	S1C	32	R/W	Operand Address

Table 11 - System data bus size configuration

A0	Size	Data bus
	Low	8-Bit
Low	High	16-Bit
High	High	32-Bit

Data bus (D0 through D31)

This 32-bit, bidirectional, three-state bus serves as the general purpose data path between the TS 68020 / TS 68030 and the TS 68882. Regardless of whether the TS 68882 is operated as a coprocessor or a peripheral processor, all inter-processor transfers of instruction information, operand data, status information, and requests for service occur as standard TS 68000 bus cycles.

The TS 68882 will operate over an 8-, 16-, or 32-bit system data bus. Depending upon the system data bus configuration, both the A0 and $\overline{SIZE}$ pins are configured specifically for the applicable bus configuration. (Refer to ADDRESS BUS (A0 through A4) and SIZE ($\overline{SIZE}$) for futher details).

Size ($\overline{SIZE}$)

This active-low input signal is used in conjunction with the A0 pin to configure the TS 68882 for operation over an 8-, 16-, or 32-bit system data bus. When the TS 68882 is configured to operate over a 16- or 32-bit system data bus, both the $\overline{SIZE}$ and A0 pins are strapped high and/or low as listed in Table 11.

Address Strobe ($\overline{AS}$)

This active-low input signal indicates that there is a valid address on the address bus, and both the chip select ($\overline{CS}$) and read/write (R/$\overline{W}$) signal lines are valid.

Chip Select ($\overline{CS}$)

This active-low input signal enables the main processor access to the TS 68882 coprocessor interface registers. When operating the TS 68882 as a peripheral processor, the chip select decode is system dependent (i.e., like the chip select on any peripheral). The $\overline{CS}$ signal must be valid (either asserted or negated) when $\overline{AS}$ is asserted. Refer to CHIP SELECT TIMING for further discussion of timing restrictions for this signal.

Read/Write (R/$\overline{W}$)

This input signal indicates the direction of a bus transaction (read/write) by the main processor. A logic high (1) indicates a read from the TS 68882, and a logic low (0) indicates a write to the TS 68882. The R/$\overline{W}$ signal must be valid when $\overline{AS}$ is asserted.

Data Strobe ($\overline{DS}$)

This active-low input signal indicates that there is valid data on the data bus during a write bus cycle.

Data transfer and size acknowledge ($\overline{DSACK0}$, $\overline{DSACK1}$)

These active-low, three-state output signals indicate the completion of a bus cycle to the main processor. The TS 68882 asserts both the $\overline{DSACK0}$ and $\overline{DSACK1}$ signals upon assertion of $\overline{CS}$.

If the bus cycle is a main processor read, the TS 68882 asserts $\overline{DSACK0}$ and $\overline{DSACK1}$ signals to indicate that the information on the data bus is valid. (Both DSACK signals may be asserted in advance of the valid data being placed on the bus). If the bus cycle is a main processor write to the TS 68882, $\overline{DSACK0}$ and $\overline{DSACK1}$ are used to acknowledge acceptance of the data by the TS 68882.

The TS 68882 also uses $\overline{DSACK0}$ and $\overline{DSACK1}$ signals to dynamically indicate to the TS 68020 / TS 68030 the «port» size (system data bus width) on a cycle-by-cycle basis. Depending upon which of the two DSACK pins are asserted in a given bus cycle, the TS 68020 / TS 68030 assumes data has been transferred to/from an 8-, 16-, or 32-bit wide data port. Table 12 lists the DSACK assertions that are used by the TS 68882 for the various bus cycles over the various bus cycles over the various system data bus configurations.

Table 12 indicates that all accesses over a 32-bit bus where A4 equals zero are to 16-bit registers. The TS 68882 implements all 16-bit coprocessor interface registers on data lines D16-D13 (to eliminate the need for on-chip multiplexers) ; howerver, the TS 68020 / TS 68030 expects 16-bit registers that are located in a 32-bit port at odd word addresses (A1 = 1) to be implemented on data lines D0-D15. For accesses to these registers when configured for 32-bit bus operation, the TS 68882 generates DSACK signals as listed in Table 12 to inform the TS 68020 / TS 68030 of valid data on D16-D31 instead of D0-D15.

An external holding resistor is required to maintain both $\overline{DSACK0}$ and $\overline{DSACK1}$ high between bus cycles. In order to reduce the signal rise time, the $\overline{DSACK0}$ and $\overline{DSACK1}$ lines are actively pulled up (negated) by the TS 68882 following the rising edge of $\overline{AS}$ or $\overline{DS}$, and both DSACK lines are then three-stated (placed in the high-impedance state) to avoid interference with the next bus cycle.

Table 12 - DSACK assertions

Data Bus	A4	$\overline{DSACK1}$	$\overline{DSACK2}$	Comments
32-Bit	1	L	L	Valid data on D31-D0
32-Bit	0	L	H	Valid data on D31-D16
16-Bit	x	L	H	Valid data on D31-D16 or D15-D0
8-Bit	x	H	L	Valid data on D31-D24, D23-D16, D15-D8 or D7-D0
All	x	H	H	Insert wait states in current bus cycle

Reset ($\overline{RESET}$)

This active-low input signal causes the TS 68882 to initialize the floating-point data registers to non-signaling not-a-numbers (NANs) and clears the floating-point control, status, and instruction address registers.

When performing a power-up reset, external circuity should keep the $\overline{RESET}$ line asserted for a minimum of four clock cycles after V_{CC} is within tolerance. This assures correct initialization of the TS 68882 when power is applied. For compatibility with all TS 68000 Family devices, 100 milliseconds should be used as the minimum.

When performing a reset of the TS 68882 after V_{CC} has been within tolerance for more than the initial power-up time, the $\overline{RESET}$ line must have an asserted pulse width which is greater than two clock cycles. For compatibility with all TS 68000 Family devices, 10 clock cycles should be used as the minimum.

Clock (CLK)

The TS 68882 clock input is a TTL-compatible signal that is internally buffered for development of the internal clock signals. The clock input should be a constant frequency square wave with no stretching or shaping techniques required. The clock should not be gated off at any time and must conform to minimum and maximum period and pulse width times.

Sense device ($\overline{SENSE}$)

This pin may be used optionally as an additional GND pin, or as an indicator to external hardware that the TS 68882 is present in the system. This signal is internally connected to the GND of the die, but it is not necessary to connect it to the external ground for correct device operation. If a pullup resistor (which should be larger than 10 kΩ) is connected to this pin location, external hardware may sense the presence of the TS 68882 in a system.

Power (V_{CC} and GND)

These pins provide the supply voltage and system reference level for the internal circuitry of the TS 68882. Care should be taken to reduce the noise level on these pins with appropriate capacitive decoupling.

No Connect (NC)

One pin of the TS 68882 package is designated as a no connect (NC). This pin position is reserved for future use by THOMSON, and should not be used for signal routing or connected to V_{CC} or GND.

Interfacing methods

TS 68882 / TS 68020 or TS 68030 Interfacing

The following paragraphs describe how to connect the TS 68882 to an TS 68020 or TS 68030 for coprocessor operation via an 8-, 16-, or 32-bit data bus.

32-Bit Data Bus Coprocessor Connection

Figure 18 illustrates the coprocessor interface connection of an TS 68882 to an TS 68020 / TS 68030 via a 32-bit data bus. The TS 68882 is configured to operate over a 32-bit data bus when both the A0 and $\overline{SIZE}$ pins are connected to V_{CC}.

16-Bit Data Bus Coprocessor Connection

Figure 19 illustrates the coprocessor interface connection of an TS 68882 to an TS 68020 / TS 68030 via a 16-bit data bus. The TS 68882 is configured to operate over a 16-bit data bus when the $\overline{SIZE}$ pin is connected to V_{CC}, and the A0 pin is connected to GND. The sixteen least significant data pins (D0-D15) must be connected to the sixteen most siginificant data pins (D16-D31) when the TS 68882 is configured to operate over a 16-bit data bus (i.e., connect D0 to D16, D1 to D17, ... and D15 to D31). The DSACK pins of the two devices are directly connected, although it is not necessary to connect the $\overline{DSACK0}$ pin since the TS 68882 never aserts it in this configuration.

8-Bit Data Bus Coprocessor Connection

Figure 20 illustrates the connection of an TS 68882 to an TS 68020 / TS 68230 as a coprocessor over an 8-bit data bus. The TS 68882 is configured to operate over a 8-bit data bus when the $\overline{SIZE}$ pin is connected to GND. The twenty four least significant data pins (D0-D23) must be connected to the eight most siginificant data pins (D24-D31) when the TS 68882 is configured to operate over a 8-bit data bus (i.e., connect D0 to D8, D16 to D24 ; D1 to D9, D17, and D15 ; ... and D7 to D15, D23 and D31). The DSACK pins of the two devices are directly connected, although it is not necessary to connect the $\overline{DSACK1}$ pin since the TS 68882 never asserts it in this configuration.

TS 68882 / TS 68000 / TS 68008 / TS 68010 Interfacing

The following paragraphs describe how to connect the TS 68882 to an TS 6800, TS 68008, or TS 68010 processor for operation as a peripheral via an 8- or 16-bit data bus.

16-Bit Data Peripheral Processor Connection

Figure 21 illustrates the connection of an TS 68882 to an TS 68000 or TS 68010 as a peripheral processor over an 16-bit data bus. The TS 68882 is configured to operate over an 16-bit data bus when the $\overline{SIZE}$ pin is connected to V_{CC}, and the A0 pin is connected to GND. The sixteen least significant data pins (D0-D15) must be connected to the sixteen most significant data pins (D16-D31) when the TS 68882 is configured to operate over an 16-bit data bus (i.e., connect D0 to D16, D1 to D17,... and D15 to D31). The $\overline{DSACK1}$ pin of the TS 68882, is connected to the $\overline{DTACK}$ pin of the main processor, and the $\overline{DSACK0}$ pin is not used.

When connected as a peripheral processor, the TS 68882 chip select ($\overline{CS}$) decode is system dependent. If the TS 68000 is used as the main processor, the TS 68882 $\overline{CS}$ must be decoded in the supervisor or user data spaces. Howerver, if the TS 68010 is used for the main processor, the MOVES instruction may be used to emulate any CPU space access that the TS 68020 / TS 68030 generates for coprocessor communications. Thus, the $\overline{CS}$ decode logic for such systems may be the same as in an TS 68020 / TS 68030 systems, such that the TS 68882 will not use anly part of the data address spaces.

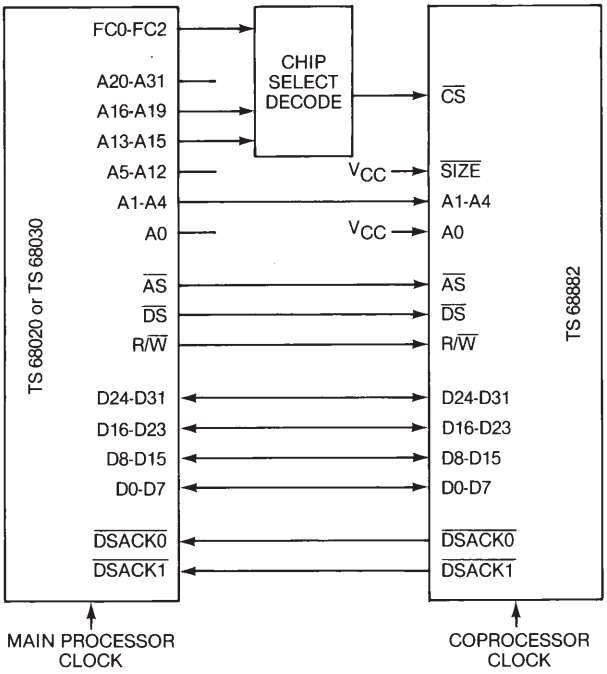


Figure 18 : 32-bit data bus coprocessor connection.

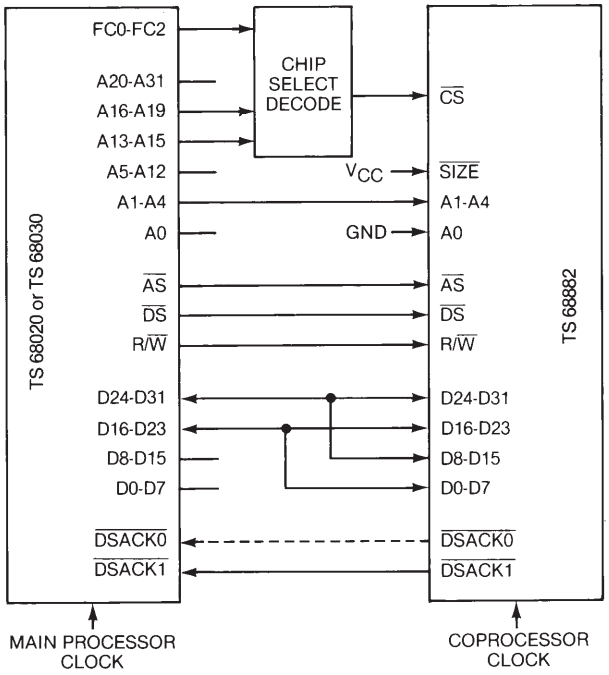


Figure 19 : 16-bit data bus coprocessor connection.

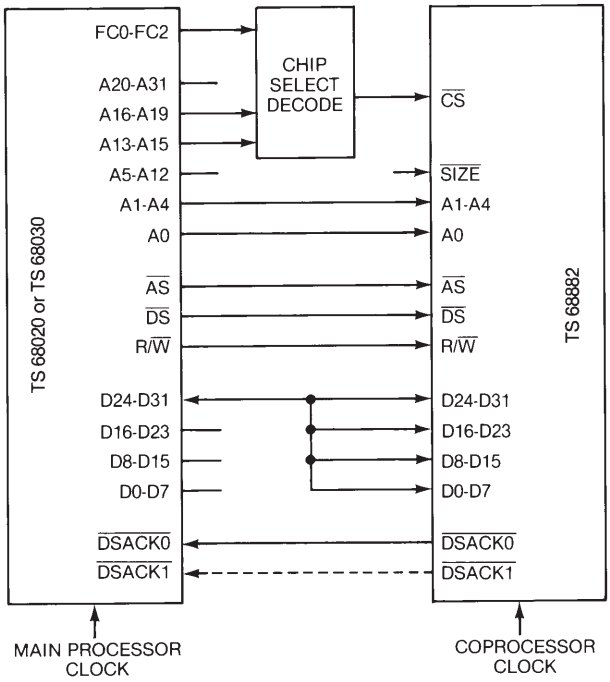


Figure 20 : 8-bit data bus coprocessor connection.

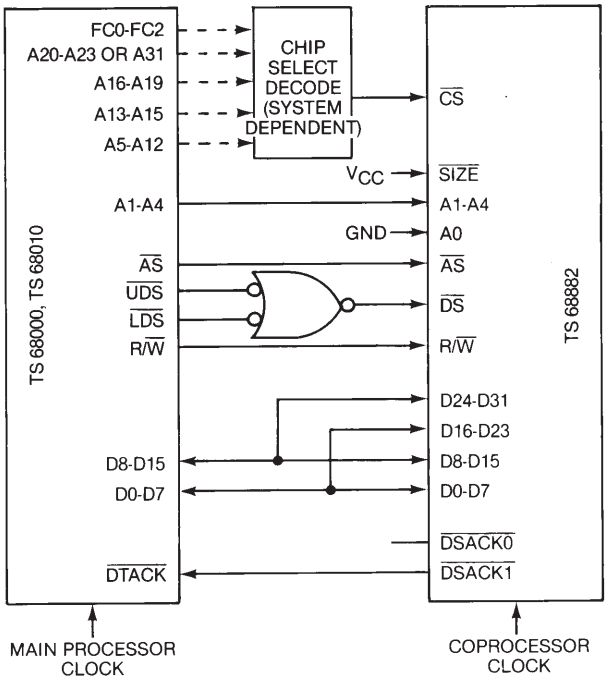


Figure 21 : 16-bit data bus peripheral processor connection.

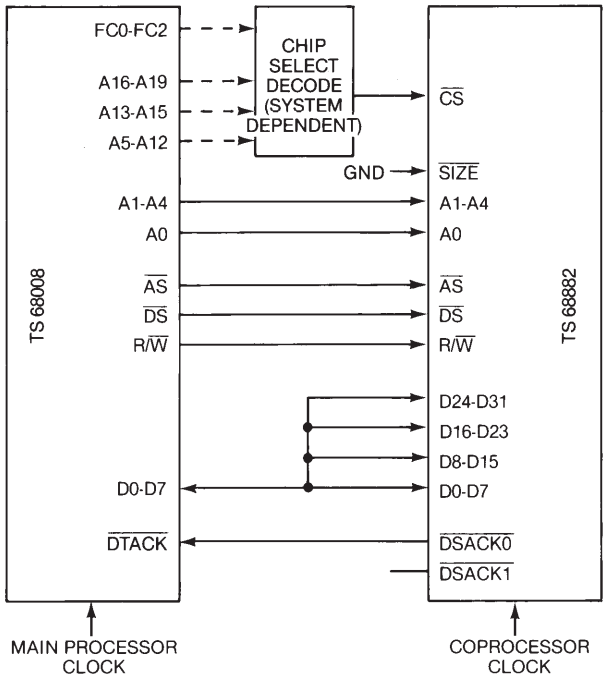


Figure 22 : 8-bit data bus peripheral processor connection.

8-Bit Data Bus Peripheral Processor Connection

Figure 22 illustrates the connection of an TS 68882 to an TS 68008 as a peripheral processor over an 8-bit data bus. The TS 68882 is configured to operate over an 8-bit data bus when the SIZE pin is connected to GND. The eight least significant data pins (D0-D7) must be connected to the twenty four most significant data pins (D8-D31) when the TS 68882 is configured to operate over an 8-bit data bus (i.e., connect D0 to D8, D16, and D24 ; D1 to D9, D17, and D25 ; ... and D7 to D15, D23, and D31). The DSACK0 pin of the TS 68882 is connected to the DTACK pin of the TS 68008, and the DSACK1 pin is not used.

When connected as a peripheral processor, the TS 68882 chip select (CS) decode is system dependent, and the CS must be decoded in the supervisor or user data spaces.

7 - PREPARATION FOR DELIVERY

7.1 - Packaging

Microcircuit are prepared for delivery in accordance with MIL-M-38510 or CECC 90000.

7.2 - Certificate of compliance

TMS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or CECC 90000 and guarantying the parameters are tested at extreme temperatures for the entire temperature range.

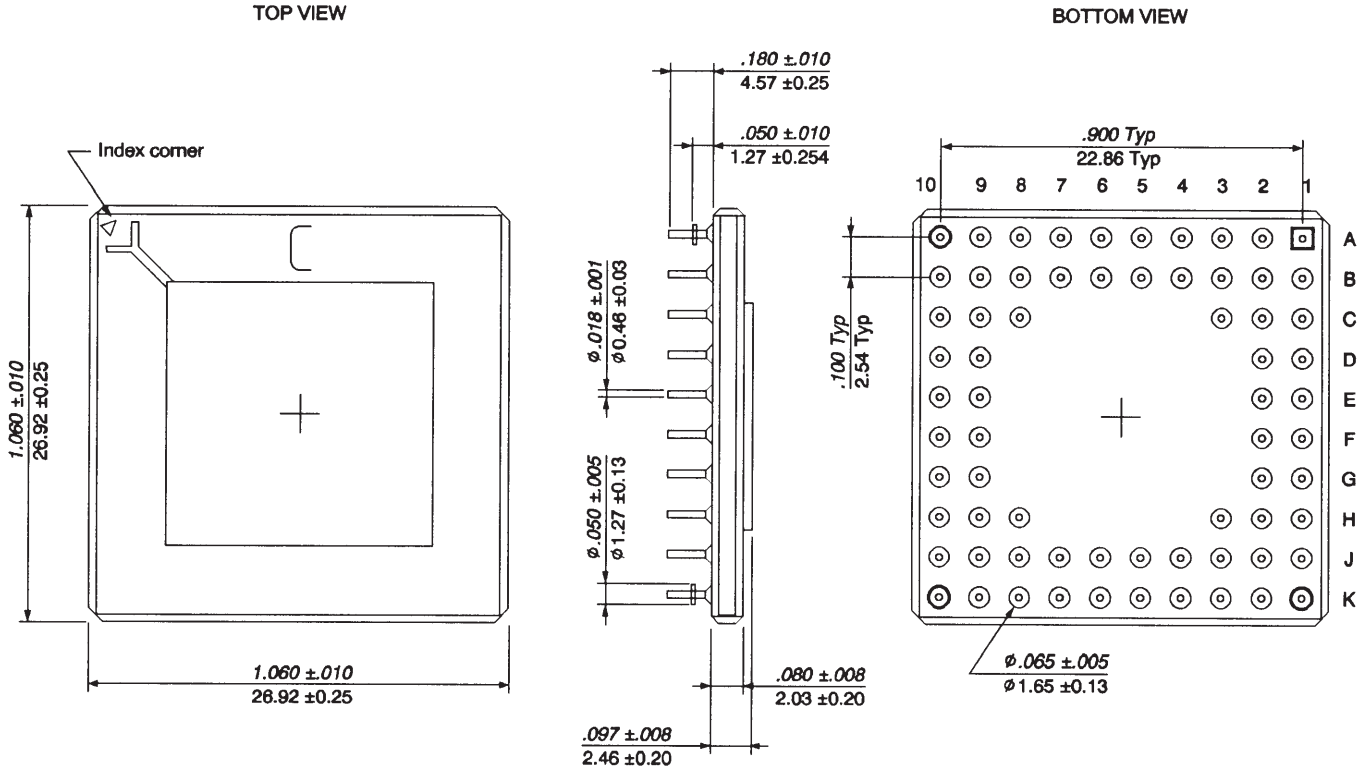
8 - HANDLING

Devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. Howerver, the following handling practices are recommended :

a) Device should be handled on benches with conductive and grounded surface.
b) Ground test equipment, tools and operator.
c) Do not handle devices by the leads.
d) Store devices in conductive foam or carriers.
e) Avoid us of plastic, rubber, or silk.
f) Maintain relative humidity above 50 %, if practical.

9 - PACKAGE MECHANICAL DATA

9.1 - 68 pins - Ceramic Pin Grid Array



Note 1 : Dimensions A and B are datums and T S datum surface.

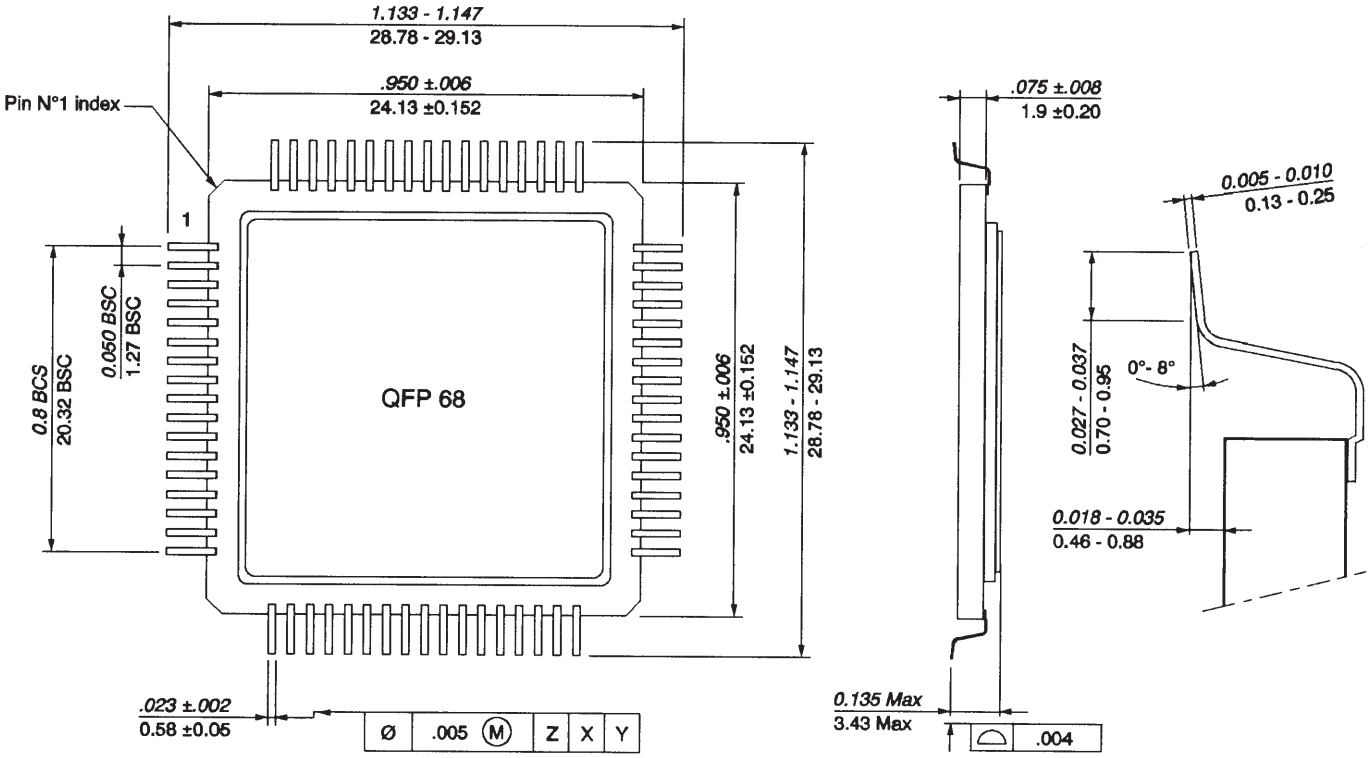
Note 2 : Positional tolerance for leads 168 places :

⌖ ø0.13 (.005) | T, A ⑤ | B ⑤

Note 3 : Dimensioning and tolerancing per AN5I Y14 5M 1982.

Note 4 : Controlling dimension : INCH.

9.2 - 68 pins - Ceramic Quad Flat Pack



10 - TERMINAL CONNECTIONS

10.1 - 68 pins - Ceramic Ping Grid Array

See Figure 2.1.

10.2 - 68 pins - Ceramic Quad Flat Pack

See Figure 2.2.

11 · ORDERING INFORMATION

11.1 · Hi-REL product

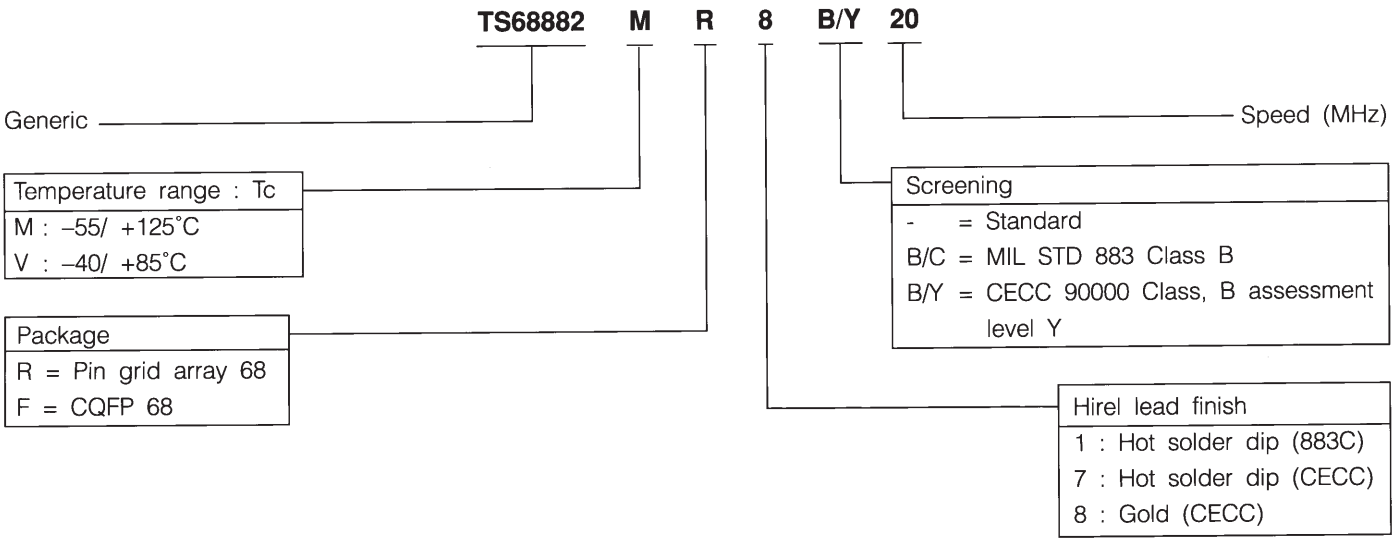
Commercial TCS Part-Number (see Note)	Norms	Package	Temperature range T_C (°C)	Frequency (MHz)	Drawing number
TS 68882MR8B/Y16	CECC	PGA 68	– 55 / + 125	16.67	90110-024
TS 68882MR8B/Y20	CECC	PGA 68	– 55 / + 125	20	90110-024
TS 68882MR8B/Y25	CECC	PGA 68	– 55 / + 125	25	90110-024
TS 68882MF8B/Y16	CECC	CQFP 68	– 55 / + 125	16.67	90110-024
TS 68882MF8B/Y20	CECC	CQFP 68	– 55 / + 125	20	90110-024
TS 68882MF8B/Y25	CECC	CQFP 68	– 55 / + 125	25	90110-024
TS 68882MRB/C16	MIL-STD-883	PGA 68	– 55 / + 125	16.67	—
TS 68882MRB/C20	MIL-STD-883	PGA 68	– 55 / + 125	20	—
TS 68882MRB/C25	MIL-STD-883	PGA 68	– 55 / + 125	25	—
TS 68882MRB/C33	MIL-STD-883	PGA 68	– 55 / + 125	33	—
TS 68882MFB/C16	MIL-STD-883	CQFP 68	– 55 / + 125	16.67	—
TS 68882MFB/C20	MIL-STD-883	CQFP 68	– 55 / + 125	20	—
TS 68882MFB/C25	MIL-STD-883	CQFP 68	– 55 / + 125	25	—
TS 68882DESC02XA	DESC	PGA 68	– 55 / + 125	16.67	5962 8946302XA
TS 68882DESC03XA	DESC	PGA 68	– 55 / + 125	20	5962 8946303XA
TS 68882DESC04XA	DESC	PGA 68	– 55 / + 125	25	5962 8946304XA
TS 68882DESC05XA	DESC	PGA 68	– 55 / + 125	33	5962 8946305XA
TS 68882DESC02YA	DESC	CQFP 68	– 55 / + 125	16.67	5962 8946302YA
TS 68882DESC03YA	DESC	CQFP 68	– 55 / + 125	20	5962 8946303YA
TS 68882DESC04YA	DESC	CQFP 68	– 55 / + 125	25	5962 8946304YA
TS 68882DESC05YA	DESC	CQFP 68	– 55 / + 125	33	5962 8946305YA

Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.

11.2 · Standard product

Commercial TCS Part-Number (see Note)	Norms	Package	Temperature range T_C (°C)	Frequency (MHz)	Drawing number
TS 68882VR16	TCS Standard	PGA 68	– 40 / + 85	16.67	Internal
TS 68882VR20	TCS Standard	PGA 68	– 40 / + 85	20	Internal
TS 68882VR25	TCS Standard	PGA 68	– 40 / + 85	25	Internal
TS 68882VR33	TCS Standard	PGA 68	– 40 / + 85	33	Internal
TS 68882MR16	TCS Standard	PGA 68	– 55 / + 125	16.67	Internal
TS 68882MR20	TCS Standard	PGA 68	– 55 / + 125	20	Internal
TS 68882MR25	TCS Standard	PGA 68	– 55 / + 125	25	Internal
TS 68882MR33	TCS Standard	PGA 68	– 55 / + 125	33	Internal
TS 68882VF16	TCS Standard	CQFP 68	– 40 / + 85	16.67	Internal
TS 68882VF20	TCS Standard	CQFP 68	– 40 / + 85	20	Internal
TS 68882VF25	TCS Standard	CQFP 68	– 40 / + 85	25	Internal
TS 68882VF33	TCS Standard	CQFP 68	– 40 / + 85	33	Internal
TS 68882MF16	TCS Standard	CQFP 68	– 55 / + 125	16.67	Internal
TS 68882MF20	TCS Standard	CQFP 68	– 55 / + 125	20	Internal
TS 68882MF25	TCS Standard	CQFP 68	– 55 / + 125	25	Internal
TS 68882MF33	TCS Standard	CQFP 68	– 55 / + 125	33	Internal

Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.



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