Electrical Specifications

ABSOLUTE MAXIMUM CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
P_D	Power Dissipation	–	–	1	W
V_{CC}	Supply Voltage	–0.5	–	7	V
V_I	Input Voltage	–0.5	–	V_{CC}+0.5	V
V_O	Output Voltage	–0.5	–	V_{CC}+0.5	V
T_{OP}	Operating Temperature (Ambient)	–25	–	85	°C
T_{STG}	Storage Temperature	–40	–	125	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

NORMAL OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
T_A	Ambient Temperature	0	–	70	°C

DC CHARACTERISTICS

(Under Normal Operation Conditions Unless Noted Otherwise)

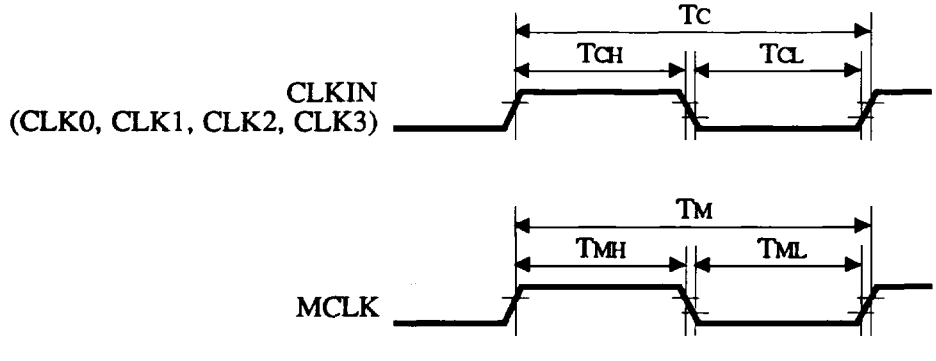
Symbol	Parameter	Notes	Min	Typ	Max	Units
I_{CC1}	Power Supply Current	@28.322 MHZ CLK, 0°C, V_{CC}=5.5V	–	65	150	mA
I_{IL}	Input Leakage Current		–100	–	+100	uA
I_{OZ}	Output Leakage Current	High Impedance	–100	–	+100	uA
V_{IL}	Input Low Voltage		–0.5	–	0.8	V
V_{IH}	Input High Voltage	All pins except clocks	2.0	–	V_{CC}+0.5	V
		CLK0, CLK1, CLK2, CLK3	2.8	–	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 8 mA (RDY, IRQ)	–	–	0.45	V
		I_{OL} = 2 mA (AA8-2,BA8-2,MAD7-0,MBD7-0)	–	–	0.45	V
		I_{OL} = 4 mA (all others)	–	–	0.45	V
V_{OH}	Output High Voltage	I_{OH} = –8 mA (RDY, IRQ)	V_{CC}–0.5	–	–	V
		I_{OL} = –2 mA (AA8-2,BA8-2,MAD7-0,MBD7-0)	V_{CC}–0.5	–	–	V
		I_{OH} = –4 mA (all others)	V_{CC}–0.5	–	–	V

Note: AC timing specifications are measured using V_{OH}=2.4V (TTL High) but outputs are CMOS and drive rail-to-rail

Electrical specifications contained herein are preliminary and subject to change without notice.

AC TIMING CHARACTERISTICS - CLOCK TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Unit
T_C	CLK Period	45 MHz	22	–	–	nS
T_{CH}	CLK High Time		$0.45T_C$	–	$0.55T_C$	nS
T_{CL}	CLK Low Time		$0.45T_C$	–	$0.55T_C$	nS
T_M	MCLK Period	50 / 56 MHz	18	–	20	nS
T_{MH}	MCLK High Time		$0.45T_M$	–	$0.55T_M$	nS
T_{ML}	MCLK Low Time		$0.45T_M$	–	$0.55T_M$	nS
T_{RF}	Clock Rise / Fall		–	–	5	nS
–	MCLK Frequency for 80 ns DRAMs		–	56.644	–	MH
–	MCLK Frequency for 100 ns DRAMs		–	50.350	–	MH



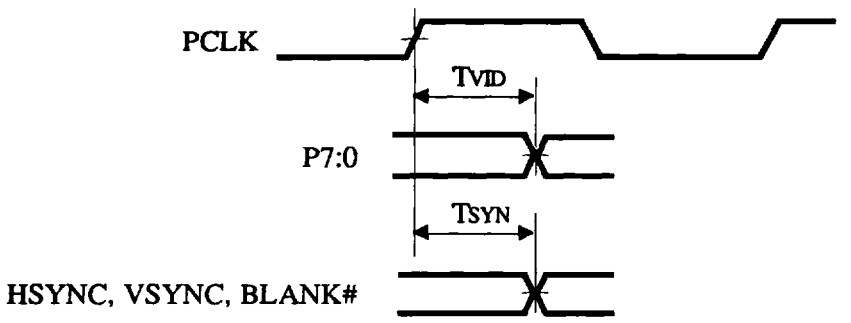
82C450 Clock Timing

AC TIMING CHARACTERISTICS - RESET TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Uni
–	RESET Pulse Width		64 T_C	–	–	nS

AC TIMING CHARACTERISTICS - VIDEO TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{SYN}	PCLK Delay to Sync/Blank	PCLK=50MHz & RAMDAC Ts/Th=3ns	3	–	17	nS
T_{VID}	PCLK Delay to Video Data	PCLK=50MHz & RAMDAC Ts/Th=3ns	3	–	17	nS
T_{SK}	Skew Between Sync/Blank & Video	PCLK=50MHz & RAMDAC Ts/Th=3ns	–	–	6	nS



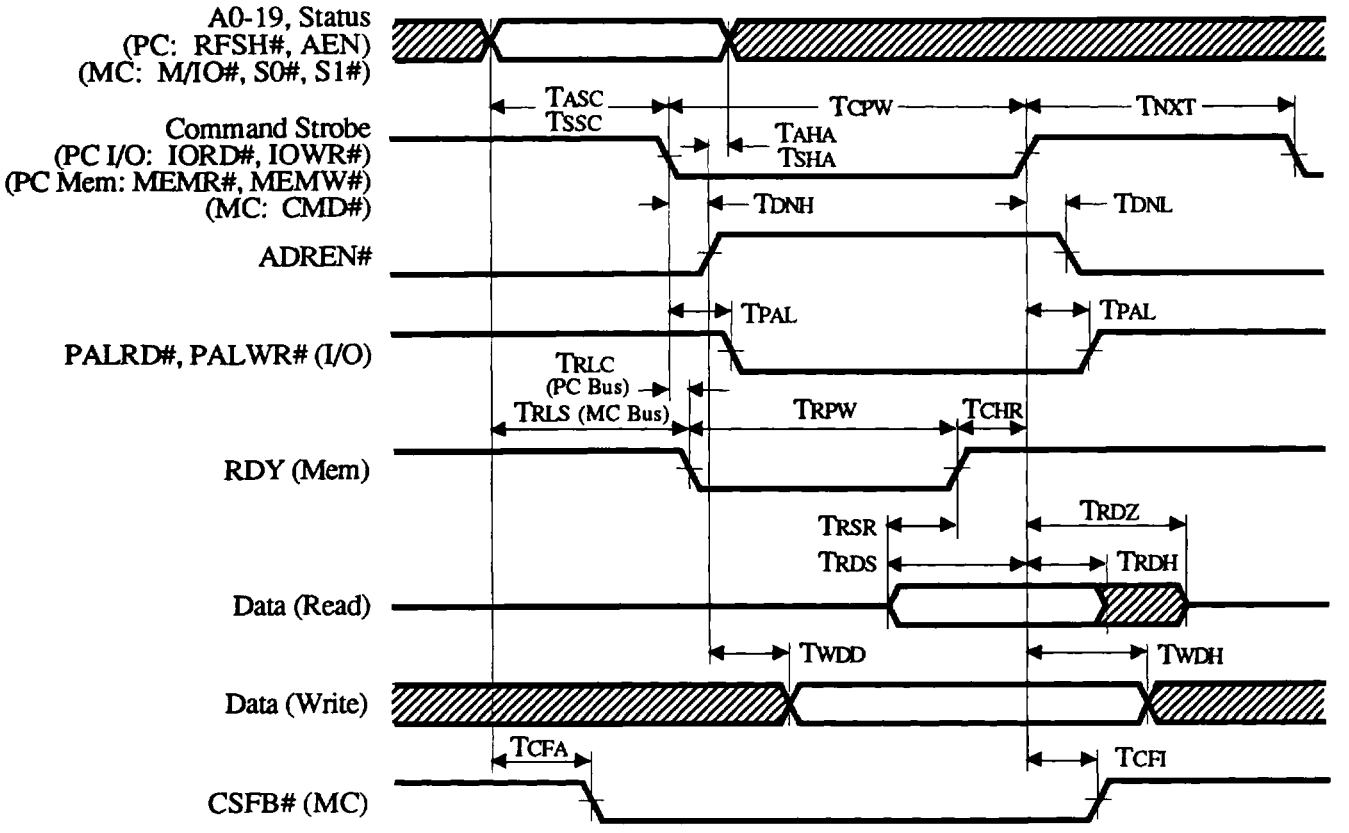
82C450 Video Timing

AC TIMING CHARACTERISTICS - BUS TIMING

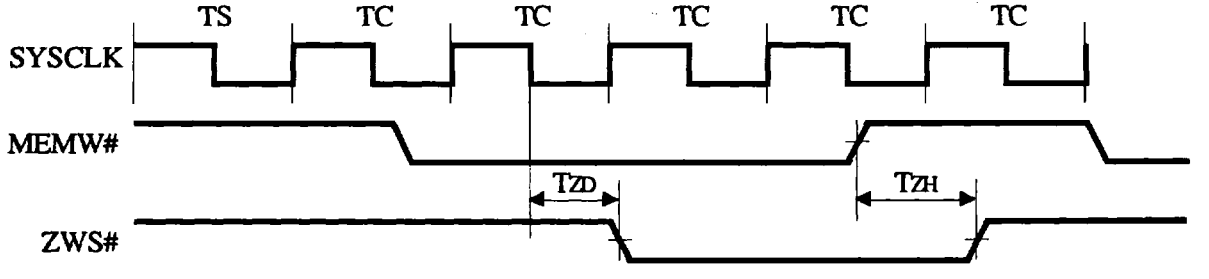
Symbol	Parameter	Notes	Min	Typ	Max	Unit
T_{CPW}	Command Strobe Pulse Width	PC Bus	175	–	–	nS
T_{CPW}	Command Strobe Pulse Width	MC Bus	90	–	–	nS
T_{CHR}	Command Strobe Hold from Ready	Mem Accesses Only	0	–	–	nS
T_{DNH}	Command Strobe Falling to ADREN# Rising		–	–	15	nS
T_{DNL}	Command Strobe Rising to ADREN# Falling		–	–	15	nS
T_{PAL}	Command Strobe Delay to Palette R/W Strobe	I/O Accesses Only	–	–	25	nS
T_{NXT}	Command Strobe Inactive to Next Strobe		80	–	–	nS
T_{ASC}	Address Setup to Command Strobe		30	–	–	nS
T_{SSC}	Status Setup to Command Strobe		30	–	–	nS
T_{AHA}	Address Hold from Address Enable		0	–	–	nS
T_{SHA}	Status Hold from Address Enable		20	–	–	nS
T_{RDS}	Read Data Setup to Read Strobe		30	–	–	nS
T_{RSR}	Read Data Setup to Ready	Mem Accesses Only	25	–	–	nS
T_{RDH}	Read Data Hold from Read Strobe		10	–	–	nS
T_{RDZ}	Read Data Tristated from Read Strobe		–	–	40	nS
T_{WDD}	Write Data Delay from Address Enable		–	–	20	nS
T_{WDH}	Write Data Hold from Write Strobe		10	–	–	nS
T_{RLC}	Ready Low Delay from Command Strobe	PC Bus Mem Only	–	–	25	nS
T_{RLS}	Ready Low Delay from Status	MC Bus Mem Only	–	–	25	nS
T_{RPW}	Ready Pulse Width	Mem Accesses Only	0	–	128Tm	nS
T_{CFA}	CSFB# Active from Address/Status Valid	MC Bus Only	–	–	25	nS
T_{CFI}	CSFB# Inactive from End of Strobe	MC Bus Only	5	–	25	nS

AC TIMING CHARACTERISTICS - ISA ZERO WAIT STATE TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Uni
T_{ZD}	ZWS# Delay	Relative to SYSCLK Falling edge for 4-SYSCLK Timing	–	–	50	nS
		Relative to SYSCLK Rising edge for 3-SYSCLK Timing				
T_{ZH}	ZWS# Hold		–	–	50	nS

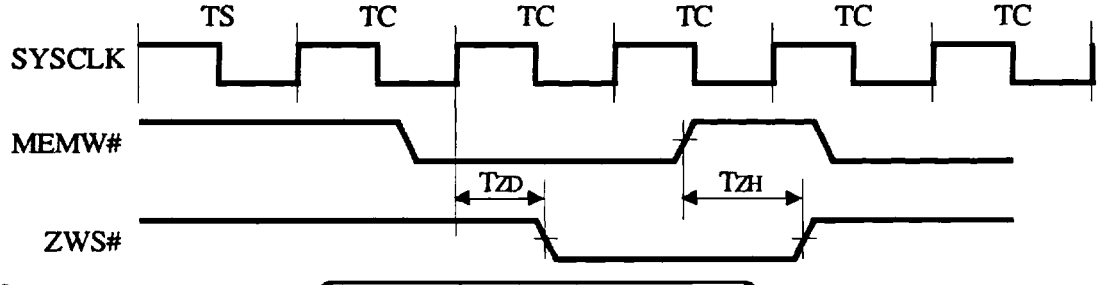


82C450 Bus Cycle Timing



Compaq 25 MHz
(Bus Speed = 8 MHz)
Note: TZD is a very critical parameter

82C450 4-SYSCLK ZWS Timing

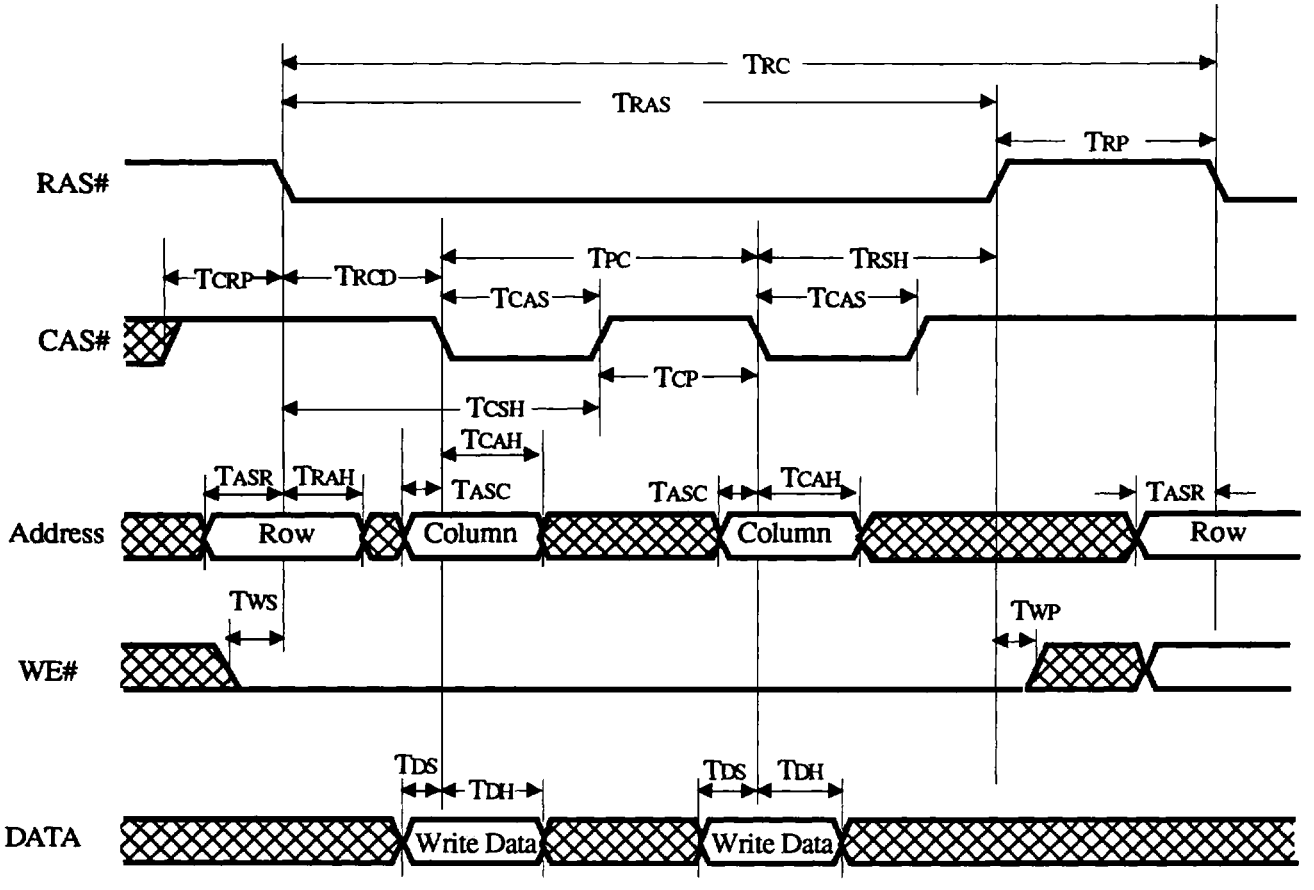


Compaq 25 MHz
(Bus Speed = 8 MHz)

82C450 3-SYSCLK ZWS Timing

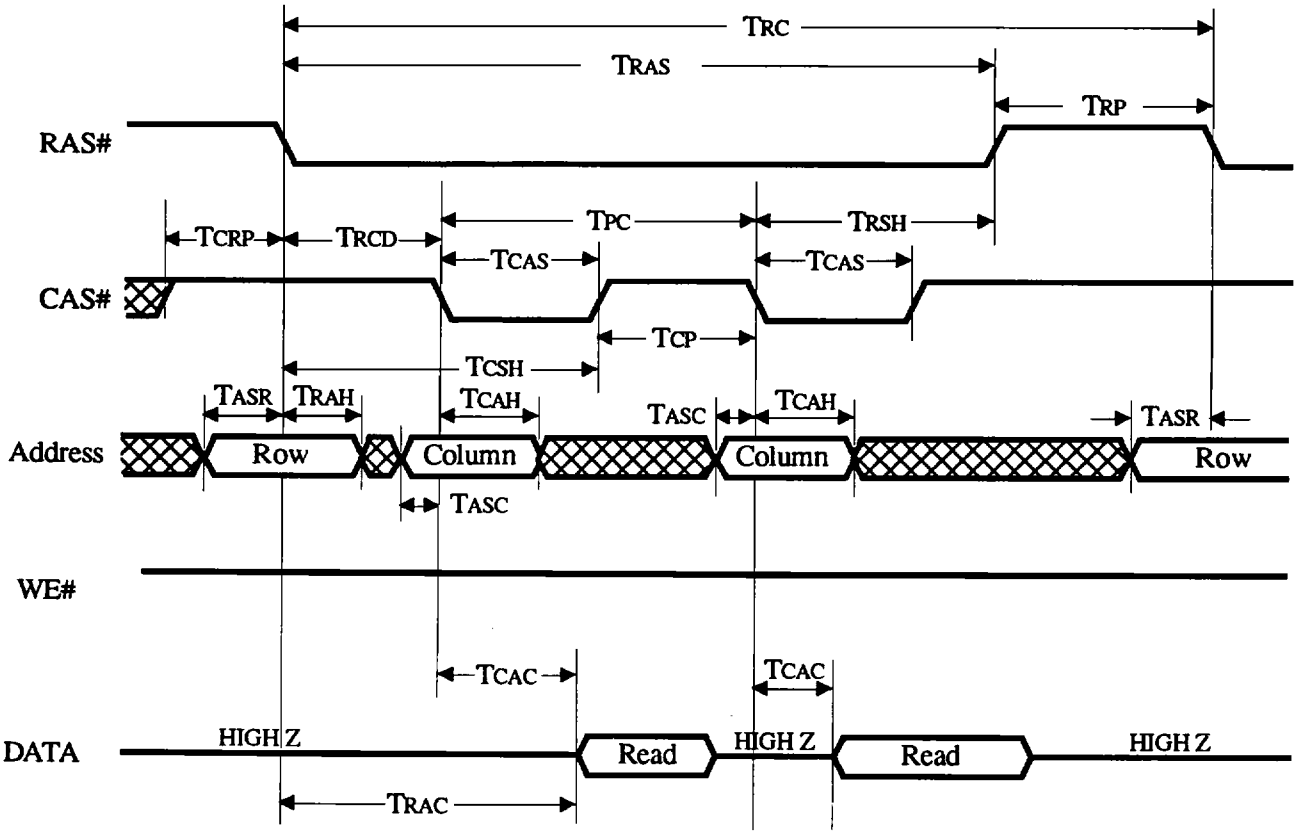
AC TIMING CHARACTERISTICS - DRAM TIMING

Symbol	Parameter	2 DRAM Min	2 DRAM Max	4 DRAM Min	4 DRAM Max	Unit
T_{RC}	Read/Write Cycle Time	18Tm – 5	–	12Tm – 5	–	nS
T_{RAS}	RAS# Pulse Width	14Tm – 5	–	8Tm – 5	–	nS
T_{RP}	RAS# Precharge	4Tm – 5	–	4Tm – 5	–	nS
T_{CRP}	CAS# to RAS# Precharge	4Tm – 5	–	4Tm – 5	–	nS
T_{CSH}	CAS# Hold from RAS#	5Tm – 5	–	5Tm – 5	–	nS
T_{RCD}	RAS# to CAS# Delay	3Tm – 5	–	3Tm – 5	–	nS
T_{RSH}	RAS# Hold from CAS#	2Tm – 5	–	2Tm – 5	–	nS
T_{CP}	CAS# Precharge	Tm – 5	–	Tm – 5	–	nS
T_{CAS}	CAS# Pulse Width	2Tm – 5	–	2Tm – 5	–	nS
T_{ASR}	Row Address Setup to RAS#	Tm – 5	–	Tm – 5	–	nS
T_{ASC}	Column Address Setup to CAS#	Tm – 5	–	Tm – 5	–	nS
T_{RAH}	Row Address Hold from RAS#	Tm – 5	–	Tm – 5	–	nS
T_{CAH}	Column Address Hold from CAS#	Tm – 5	–	Tm – 5	–	nS
T_{CAC}	Data Access Time from CAS#	–	2Tm – 5	–	2Tm – 5	nS
T_{RAC}	Data Access Time from RAS#	–	5Tm – 5	–	–	nS
T_{DS}	Write Data Setup to CAS#	Tm – 5	–	Tm – 5	–	nS
T_{DH}	Write Data Hold from CAS#	2Tm – 5	–	2Tm – 5	–	nS
T_{WS}	WE# Setup to RAS#	5	–	2Tm	–	nS
T_{WP}	WE# Hold from RAS#	0	–	–	–	nS
T_{PC}	CAS# Cycle Time	3Tm-5	–	3Tm – 5	–	nS



DRAM Page Mode Write Cycle Timing

Note: The above diagram represents a typical page mode write cycle.
The number of actual CAS cycles may vary between 0 and 4.

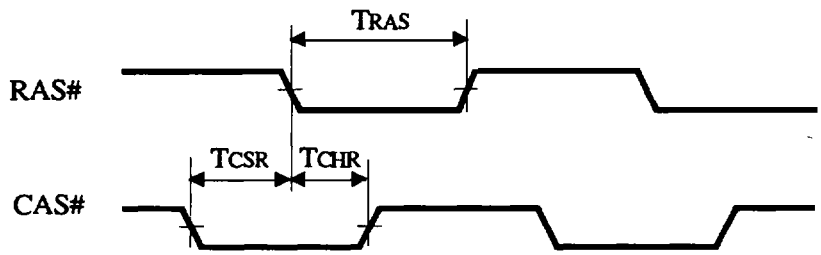


DRAM Page Mode Read Cycle Timing

Note: The above diagram represents a typical page mode read cycle. The number of actual CAS cycles may vary. The maximum number of CAS cycles allowed is 32 (when the FIFO is being filled).

AC TIMING CHARACTERISTICS - REFRESH TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{CHR}	RAS to CAS delay	Tm = 17.7 @ 56 MHz	5Tm – 5	–	5Tm + 5	nS
T_{CSR}	CAS to RAS delay	5Tm = 88.3 ns (56 MHz) or 100 ns (50MHz)	Tm – 5	–	Tm + 5	nS
T_{RAS}	RAS pulse width		5Tm – 5	–	5Tm + 5	nS



82C450 CAS-Before-RAS (CBR) Refresh Cycle Timing