

T6L97

Gate Driver for TFT LCD Panels

The T6L97 is a 263 / 256 / 240-channel output gate driver for TFT LCD panels.

Features

- LCD drive output pins : Switchable 263 / 256 / 240 pins
- LCD drive voltage : max 43.5 V
- Data transfer method : Bidirectional shift register
- Operating temperature : -20 to 75°C
- Package : TCP / COF

Application

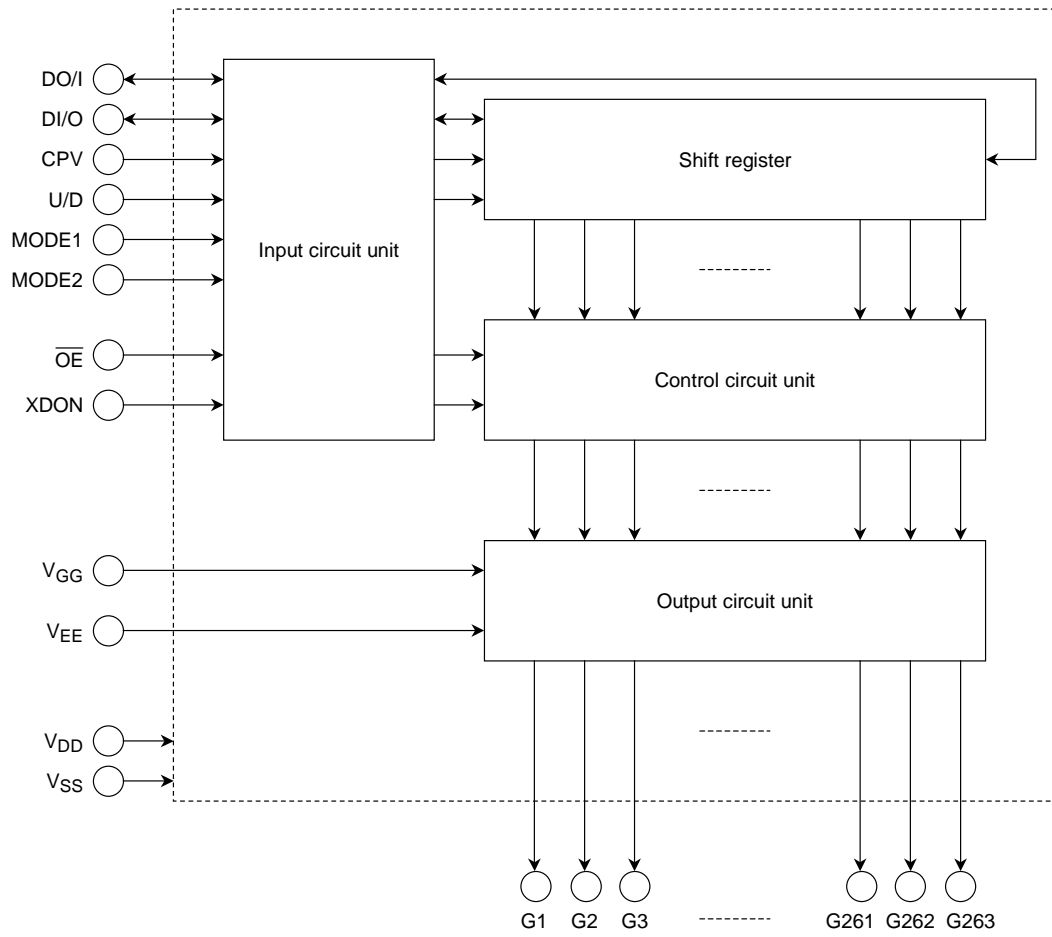
- Module for PC monitor

Unit: mm		
T6L97	User Area Pitch	
	IN	OUT

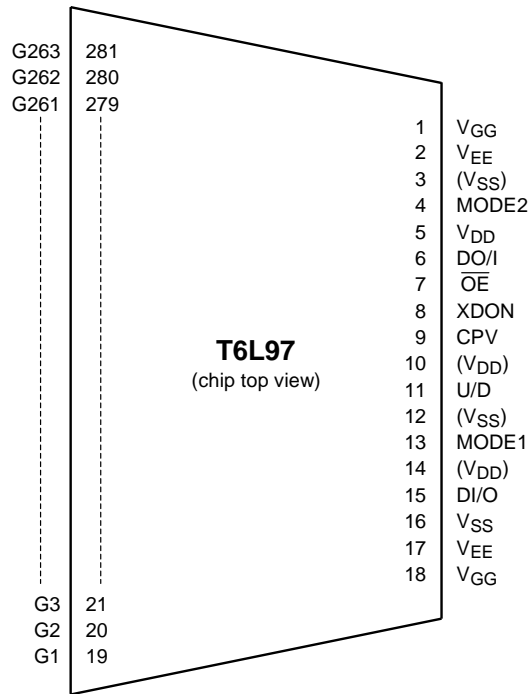
Please contact Toshiba or a distributor for the latest TCP specification and product line-up.

TCP (Tape Carrier Package)

Block Diagram



Pin Assignment



The above diagram shows the device's pin configuration only and does not necessarily correspond to the pad layout on the chip. Please contact Toshiba or our distributors for the latest TCP / COF specification.

Pin Function

Pin Name	I/O	Function														
DI/O DO/I	I/O	<p>Vertical shift data I/O pins These pins are used to input and output shift data. These pins are switched between input and output by setting the U/D pin as shown below.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>U/D</th> <th>DI/O</th> <th>DO/I</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>Input</td> <td>Output</td> </tr> <tr> <td>L</td> <td>Output</td> <td>Input</td> </tr> </tbody> </table> <p>When set for input This pin is used to feed data into the shift registers at the first stage of the LCD driver. The data is latched into the shift registers at the rising edge of CPV.</p> <p>When set for output When two or more T6L97s are cascaded, this pin outputs the data to be fed into the next stage. This data changes state synchronously with the falling edge of CPV.</p>	U/D	DI/O	DO/I	H	Input	Output	L	Output	Input					
U/D	DI/O	DO/I														
H	Input	Output														
L	Output	Input														
U/D	I	<p>Transfer direction select pin This pin specifies the direction in which data is transferred through the shift registers. The shift register data is shifted synchronously with each rising edge of CPV as follows: When U/D is high, data is shifted in the direction U/D = "H": G1 → G2 → G3 → G4 → ... → G263 When U / D is low, the direction is reversed to give U/D = "L": G263 → G262 → G261 → G260 → ... → G1 The voltage applied to this pin must be a DC-level voltage that is either high (V_{DD}) or low (V_{SS}).</p>														
CPV	I	<p>Vertical shift clock This is the shift clock for the shift registers. Data is shifted through the shift registers synchronously with the rising edge of CPV.</p>														
\overline{OE}	I	<p>Output enable pins These signals control the data appearing at the LCD panel drive pins (G1 through G263). \overline{OE} doesn't synchronize with the CPU. The V_{EE} voltage is output when \overline{OE} is high; normal shift data is output when \overline{OE} is low.</p>														
MODE1 MODE2	I	<p>Output channels select pin This signal selects 263 / 256 / 240-pin mode for the LCD panel driver.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>MODE1</th> <th>MODE2</th> <th>LCD drive output pins</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>263</td> </tr> <tr> <td>H</td> <td>L</td> <td rowspan="2">256</td> </tr> <tr> <td>L</td> <td>H</td> </tr> <tr> <td>L</td> <td>L</td> <td>240</td> </tr> </tbody> </table>	MODE1	MODE2	LCD drive output pins	H	H	263	H	L	256	L	H	L	L	240
MODE1	MODE2	LCD drive output pins														
H	H	263														
H	L	256														
L	H															
L	L	240														
XDON	I	<p>Display-ON input pin When XDON = low, the V_{GG} voltage is output all output pins irrespective of the shift data and the content of input data. However, this does not cause the contents of the shift registers to be cleared. XDON operates asynchronously with CPV. If XDON and \overline{OE} are asserted simultaneously, XDON is given priority over \overline{OE}. This pin is pulled up on the T6L97. Since all LCD drive outputs output the V_{GG} level, much current may generate them momentarily. When 256 / 240-pin mode, unapplied LCD panel drive pins fixed V_{EE}.</p>														
G1 to G263	O	<p>LCD panel drive pins These pins output the shift register data or the voltage applied to V_{GG} or V_{EE} depending on the control signals \overline{OE} and XDON.</p>														
V _{GG}	—	Power supply for LCD drive														
V _{EE}	—	Power supply for LCD drive														
V _{DD}	—	Power supply for the internal logic The (V _{DD}) is the pin for connection.														
V _{SS}	—	Power supply for the internal logic The (V _{SS}) is the pin for connection.														

Device Operation

- Shift data transfer method

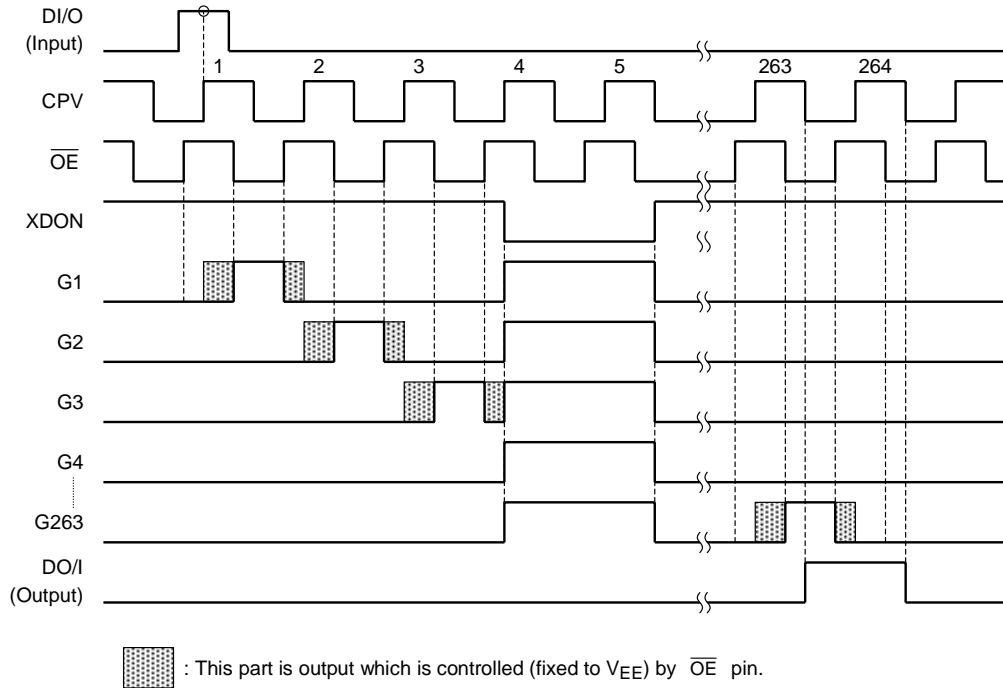
MODE1	MODE2	Output Mode	U/D Pin	Shift Data		Data Transfer Method
				Input	Output	
H	H	263-out	H	DI/O	DO/I	G1 → G2 → G3 → G4 → ... → G263
			L	DO/I	DI/O	G263 → G262 → G261 → ... → G1
H	L	256-out	H	DI/O	DO/I	G1 → G2 → G3 → G4 → ... → G128 → G136 → ... → G263
L	H		L	DO/I	DI/O	G263 → G262 → G261 → ... → G136 → G128 → ... → G1
L	L	240-out	H	DI/O	DO/I	G1 → G2 → G3 → G4 → ... → G120 → G144 → ... → G263
			L	DO/I	DI/O	G263 → G262 → G261 → ... → G144 → G120 → ... → G1

The input data (DI/O or DO/I) is latched into the internal register synchronously with the rising edge of the shift clock CPV. At the same time that the data is shifted to the next register at the next rise of CPV, new vertical shift data is latched into.

In the output operation, the data in the last shift register (G263 or G1) is output synchronously with the falling edge of CPV. (The output high voltage is the VDD level; the output low voltage is the VSS level.)

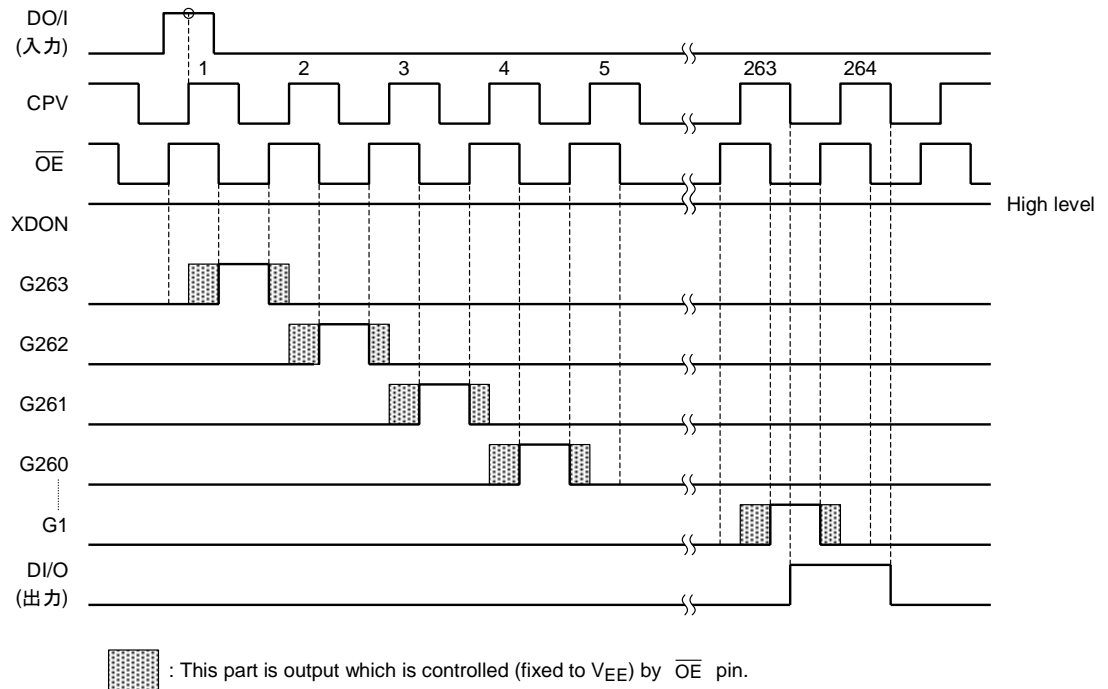
Timing Diagram 1

- 263-out mode (U/D = high, MODE1 = high, MODE2 = high)



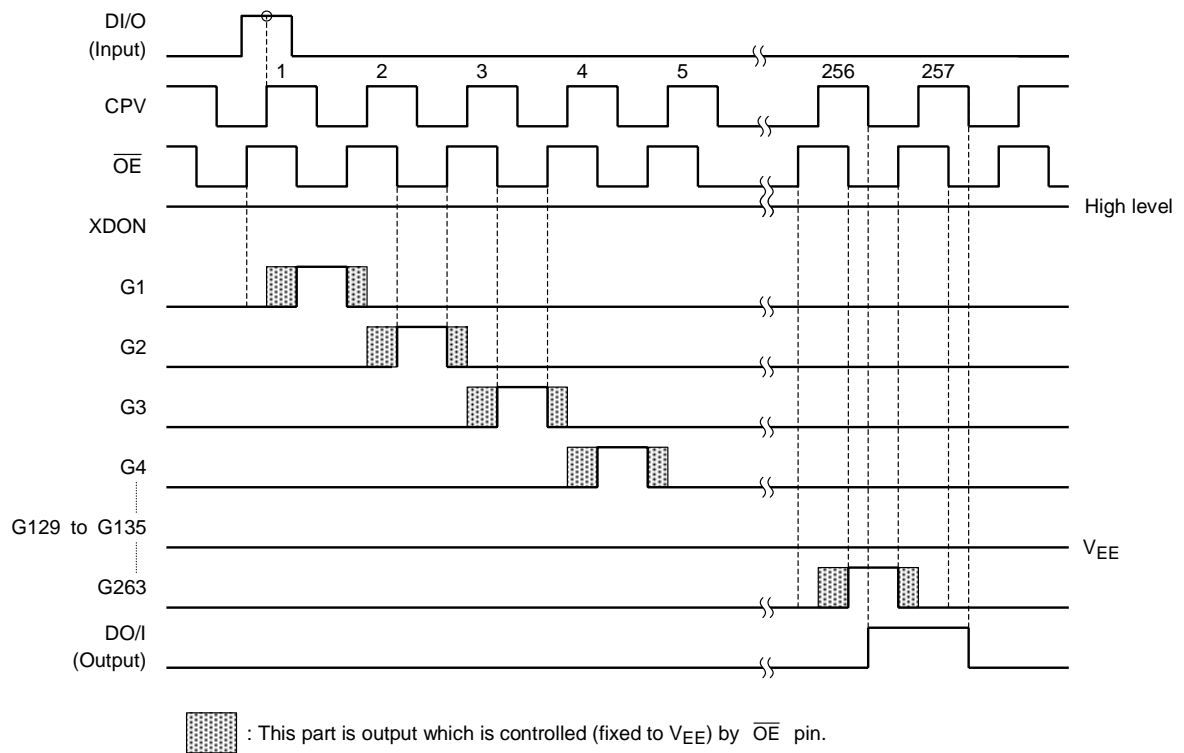
Timing Diagram 2

- 263-out mode (U/D = low, MODE1 = high, MODE2 = high)



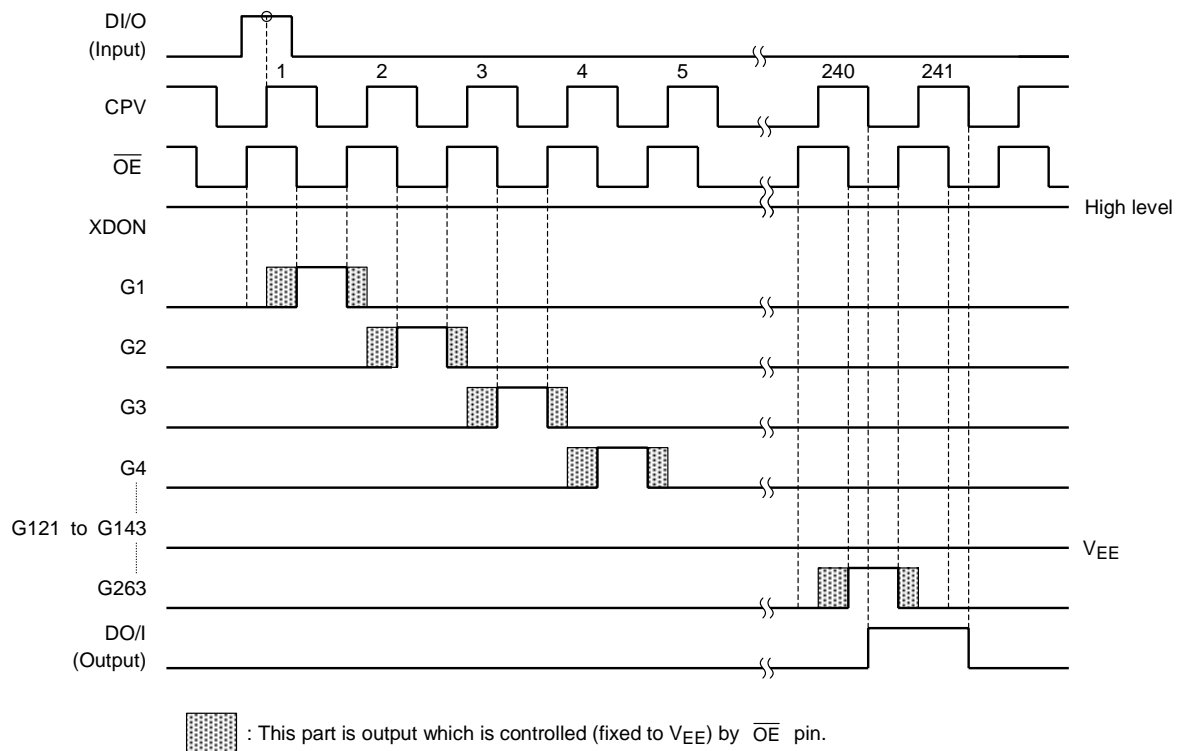
Timing Diagram 3

- 256-out mode (U/D = high, MODE1 = high, MODE2 = low)



Timing Diagram 4

- 240-out mode (U/D = low, MODE1 = low, MODE2 = low)



Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V _{DD}	-0.3 to 3.6	V
Supply voltage (2)	V _{GG}	-0.3 to 45.0	
Supply voltage (3)	V _{EE}	-20.0 to 0.3	
Supply voltage (4)	V _{GG} - V _{EE}	-0.3 to 45.0	
Input voltage	V _{IN}	-0.3 to V _{DD} + 0.3	V
Storage temperature	T _{stg}	-55 to 125	°C

Recommended Operating Conditions (V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V _{DD}	2.7 to 3.6	V
Supply voltage (2)	V _{GG}	10 to 35	
Supply voltage (3)	V _{EE}	-15 to -5	
Supply voltage (4)	V _{GG} - V _{EE}	15.0 to 43.5	
Operating temperature	T _{opr}	-20 to 75	°C
Operating frequency	f _{CPV}	DC to 100	kHz
Output Load capacitance	C _L	300 (max)	pF/PIN

Electrical Characteristics

DC Characteristics

(V_{GG} - V_{EE} = 30.0 to 43.5 V, V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, T_a = -20 to 75°C)

Parameter		Symbol	Test circuit	Test Condition	Min	Max	Unit	Relevant
Input voltage	Low Level	V _{IL}	—	—	V _{SS}	0.3 × V _{DD}	V	(Note1)
	High Level	V _{IH}		—	0.7 × V _{DD}	V _{DD}		
Output voltage	Low Level	V _{OL}	—	I _{OL} = 40 μA	V _{SS}	V _{SS} + 0.4	V	DI/O, DO/I
	High Level	V _{OH}		I _{OH} = -40 μA	V _{DD} - 0.4	V _{DD}		
Output resistance	Low Level	R _{OL}	—	V _{OUT} = V _{EE} + 0.5 V	—	1000	Ω	G1 to G263
	High Level	R _{OH}		V _{OUT} = V _{GG} - 0.5 V				
Pull-up resistance		R _{ION}	—	—	—	150	kΩ	XDON
Input leakage current		I _{IN}	—	—	-1	1	μA	(Note1)
Current consumption (1)		I _{GG}	—	non-load (Note2)	—	50	μA	V _{GG}
Current consumption (2)		I _{DD}		(Note2)	—	50		V _{DD}
Current consumption (3)		I _{EE}		non-load (Note2)	—	50		V _{EE}

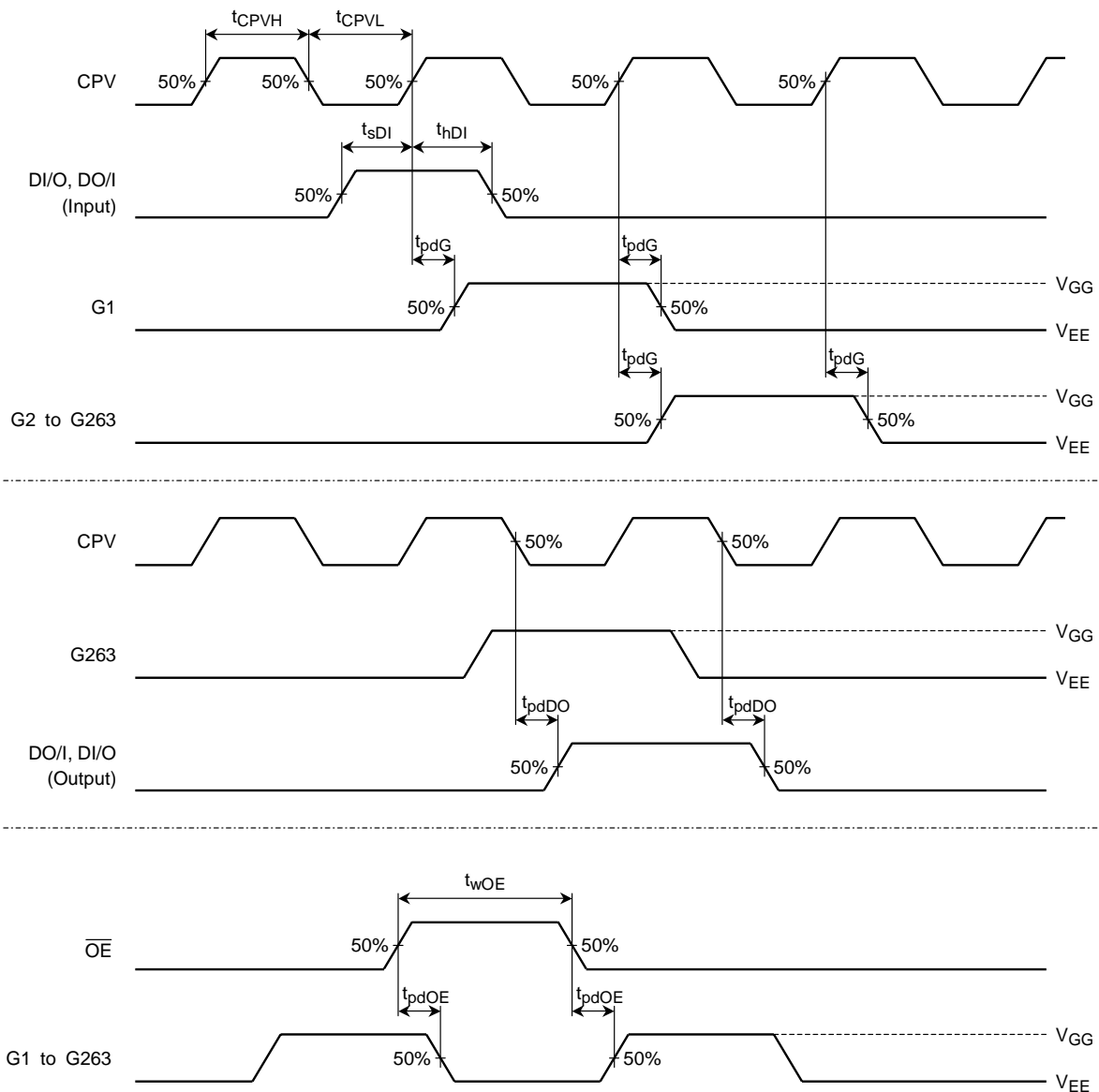
Note1 : These input pins include DI/O, DO/I, CPV, \overline{OE}

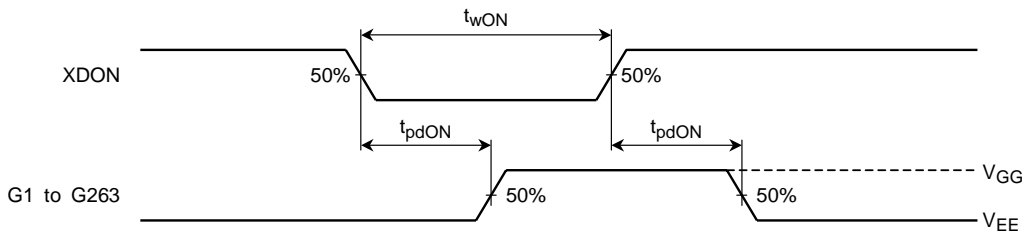
Note2 : f_{CPV} = 50kHz, Shift data input : 60Hz, \overline{OE} = "L", XDON = "H", MODE1 / MODE2 = "H"

AC Characteristics

($V_{GG} - V_{EE} = 30.0$ to 43.5 V, $V_{DD} = 2.7$ to 3.6 V, $V_{SS} = 0$ V, $T_a = -20$ to 75°C)

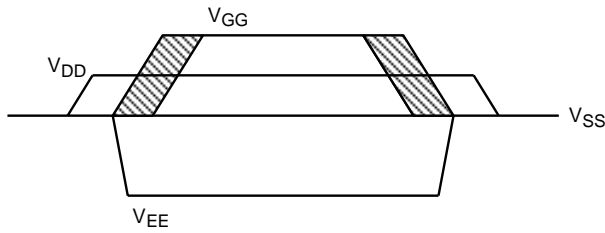
Parameter	Symbol	Test circuit	Test Condition	Min	Max	Unit
Clock frequency	t_{CPV}	—	—	—	100	kHz
CPV pulse width (H)	t_{CPVH}	—	—	500	—	ns
CPV pulse width (L)	t_{CPVL}	—	—	500	—	ns
Data set-up time	t_{sDI}	—	—	200	—	ns
Data hold time	t_{hDI}	—	—	200	—	ns
\overline{OE} enable time	t_{wOE}	—	—	1	—	μs
Display-ON pulse width	t_{wON}	—	$C_L = 300$ pF	100	—	μs
Output delay time (1)	t_{pdDO}	—	$C_L = 50$ pF	—	100	ns
Output delay time (2)	t_{pdG}	—	$C_L = 300$ pF	—	800	
Output delay time (3)	t_{pdOE}	—	$C_L = 300$ pF	—	800	
Output delay time (4)	t_{pdON}	—	$C_L = 300$ pF	—	10	μs





Power Supply Sequence

Turn power on in the order $V_{DD} \rightarrow V_{EE} \rightarrow$ Input signal $\rightarrow V_{GG}$. Turn power off in th reverse order. It may input V_{EE} , input signal and V_{GG} simultaneously.



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