LOW POWER, HIGH CMRR, 3-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 120 dB CMRR (± 0.01 Count / Volt CMV error)
- Fast Overrange Recovery, Guaranteed First Reading Accuracy
- Low Temperature Drift Internal Reference
  TC7131 .... 70 ppm/°C Typ
- Guaranteed Zero Reading With Zero Input
- Low Noise .... 15 μV_{P-P}
- High Resolution 0.05%
- Wide Dynamic Range .... 72 dB
- Low Input Leakage Current .... 1 pA Typ
  10 pA Max
- Direct LCD Drive — No External Components
- Precision Null Detectors With True Polarity at Zero
- High-Impedance Differential Input
- Convenient 9V Battery Operation With Low Power Dissipation .... 500 µW Typ
  900 µW Max
- Internal Clock Circuit

TYPICAL APPLICATIONS

- Thermometry
- Bridge Readouts
  - — Strain Gauges
  - — Load Cells
  - — Null Detectors
- Digital Meters
  - — Voltage/Current/Ohms/Power
  - — pH
  - — Capacitance/Inductance
  - — Fluid Flow Rate/Viscosity/Level
  - — Humidity
  - — Position
- Digital Scales
- Panel Meters
- LVDT Indicators
- Portable Instrumentation
- Power Supply Readouts
- Process Monitors
- Gaussometers

ORDERING INFORMATION

Part No.	Package	Temperature Range	Reference TempCo (Max)
TC7131CPL	40-Pin Plastic DIP	0°C to +70°C	150 ppm/°C
TC7131CLW	44-Pin PQFP	0°C to + 70° C	150 ppm/°C

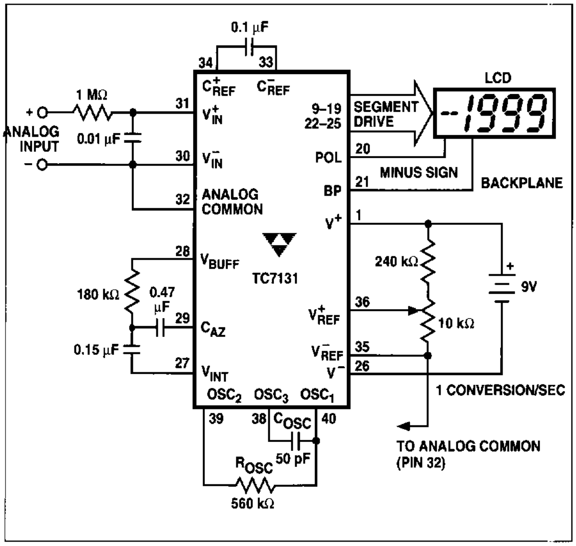
GENERAL DESCRIPTION

The TC7131 is a low-power, 3-1/2 digit, LCD-drive analog-to-digital converter (ADC). It has superior DC Common-Mode Rejection (CMR) when used with either a single or split power supply. It incorporates an "integrator output zero" phase which guarantees overrange recovery. The performance of existing TC7126, TC7126A and ICL7136-based systems may be upgraded with minor changes to external passive components. (see "System Timing")

The TC7131 limits linearity error to less than 1 count on 200 mV or 2V full-scale ranges. Roll-over error — the difference in readings for equal magnitude but opposite polarity input signals — is below ±1 count. High-impedance differential inputs offer 1 pA leakage currents and a $10^{12}\Omega$ input impedance. The differential reference input allows ratiometric measurements for ohms or bridge transducer measurements. The 15 μV_{P-P} noise performance guarantees a "rock solid" reading. The auto-zero cycle guarantees a zero display readout for a 0V input.

The single-chip CMOS TC7131 incorporates all the active devices for a 3-1/2 digit ADC to directly drive an LCD. The internal oscillator, precision voltage reference, and display segment/backplane drivers simplify system integration, reduce board space requirements and lower total cost. A low-cost, high-resolution (0.05%) indicating meter requires only a display, four resistors, four capacitors and a 9V battery.

TYPICAL OPERATING CIRCUIT



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (Either Input) (Note 1) .... V^+ to V^-
Reference Input Voltage (Either Input) .... V^+ to V^-
Clock Input ....TEST to V^+
Power Dissipation (Note 2)
Plastic DIP (P)... 800 mW
Flat Package (L)... 500 mW
Operating Temperature Range
C Devices ....0°C to +70°C
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) .... +300°C

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

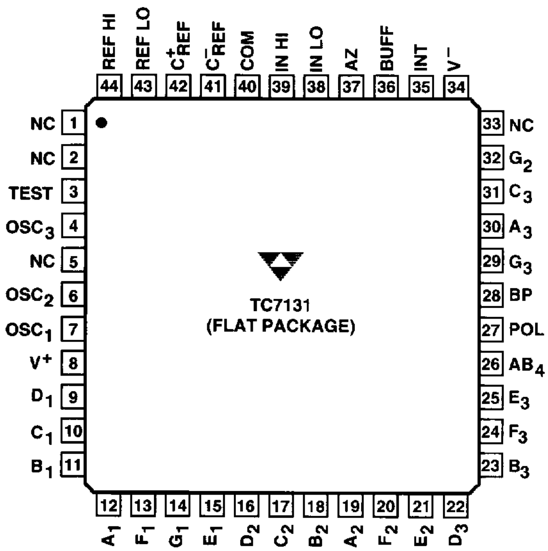
ELECTRICAL CHARACTERISTICS: V_S = 9V, f_{CLK} = 16 kHz, and T_A = +25°C, unless otherwise noted.

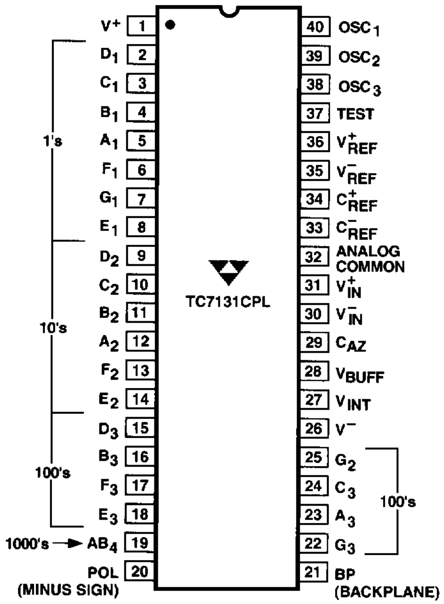
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
	Zero Input Reading	V_{IN} = 0V Full Scale = 200 mV	–000.0	±000.0	+000.0	Digital Reading
	Zero Reading Drift	V_{IN} = 0V, 0°C ≤ T_A ≤ +70°C	—	0.2	1	µV/°C
	Ratiometric Reading	$V_{IN} = V_{REF}$, V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
NL	Nonlinearity Error	Full Scale = 200 mV or 2V Max Deviation From Best Straight Line	–1	±0.2	1	Count
	Roll-Over Error	$-V_{IN} = +V_{IN} \approx$ 200 mV	–1	±0.2	1	Count
e_N	Noise	V_{IN} = 0V, Full Scale = 200 mV	—	15	—	$µV_{P-P}$
I_L	Input Leakage Current	V_{IN} = 0V	—	1	10	pA
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V, Full Scale = 200 mV	—	1	—	µV/V
	Scale Factor Temperature Coefficient	V_{IN} = 199 mV, 0°C ≤ T_A ≤ +70°C Ext Ref Temp Coeff = 0 ppm/°C	—	1	5	ppm/°C
Analog Common						
V_{CTC}	Analog Common Temperature Coefficient	250 kΩ Between Common and V^+ 0°C ≤ T_A ≤ +70°C	—	70	150	ppm/°C
V_C	Analog Common Voltage	250 kW Between Common and V^+	2.7	3.05	3.35	V
LCD Drive						
V_{SD}	LCD Segment Drive Voltage	V^+ to V^- = 9V	4	5	6	V_{P-P}
V_{BD}	LCD Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V_{P-P}
Power Supply						
I_S	Power Supply Current	V_{IN} = 0V, V^+ to V^- = 9V (Note 6)	—	70	100	µA

NOTES:
1. Input voltages may exceed supply voltages when input current is limited to 100 µA.
2. Dissipation rating assumes device is mounted with all leads soldered to PC board.
3. Refer to "Differential Input" discussion.
4. Backplane drive is in-phase with segment drive for "off" segment and 180° out-of-phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50 mV.
5. See "Typical Operating Circuit".
6. A 48 kHz oscillator increases current by 20 µA (typical). Common current not included.

2

PIN CONFIGURATIONS





NC = NO INTERNAL CONNECTION

PIN DESCRIPTION

40-Pin DIP Pin Number	44-Pin Plastic Quad Flat Package Pin Number	Name	Description
1	2	V^+	Positive supply voltage.
2	3	D_1	Activates the D section of the units display.
3	4	C_1	Activates the C section of the units display.
4	5	B_1	Activates the B section of the units display.
5	6	A_1	Activates the A section of the units display.
6	7	F_1	Activates the F section of the units display.
7	8	G_1	Activates the G section of the units display.
8	9	E_1	Activates the E section of the units display.
9	10	D_2	Activates the D section of the tens display.
10	11	C_2	Activates the C section of the tens display.
11	13	B_2	Activates the B section of the tens display.
12	14	A_2	Activates the A section of the tens display.
13	15	F_2	Activates the F section of the tens display.
14	16	E_2	Activates the E section of the tens display.
15	17	D_3	Activates the D section of the hundreds display.
16	18	B_3	Activates the B section of the hundreds display.
17	19	F_3	Activates the F section of the hundreds display.
18	20	E_3	Activates the E section of the hundreds display.
19	21	AB_4	Activates both halves of the 1 in the thousands display.
20	22	POL	Activates the negative polarity display.
21	24	BP	Backplane drive output.
22	25	G_3	Activates the G section of the hundreds display.
23	26	A_3	Activates the A section of the hundreds display.
24	27	C_3	Activates the C section of the hundreds display.
25	28	G_2	Activates the G section of the tens display.
26	29	V^-	Negative power supply voltage.
27	30	V_{INT}	The integrating capacitor should be selected to give the maximum voltage swing that ensures component tolerance build-up will not allow the integrator output to saturate. When ANALOG COMMON is used as a reference and the conversion rate is 3 readings per second, a 0.047 µF capacitor may be used. The capacitor must have a low dielectric constant to prevent roll-over errors. See Integrating Capacitor section for additional details.
28	31	V_{BUFF}	Integration resistor connection. Use a 180 kΩ for a 200 mV full-scale range and a 1.8 MΩ for 2V full-scale range.
29	32	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.47 µF capacitor for a 200 mV full scale, and a 0.1 µF capacitor for a 2V full scale. See paragraph on Auto-Zero Capacitor for more details.
30	33	V_{IN}^-	The low input signal is connected to this pin.
31	35	V_{IN}^+	The high input signal is connected to this pin.
32	36	ANALOG COMMON	Internal V COMMON GENERATOR.

TC7131 PIN DESCRIPTION (Cont.)

40-Pin DIP Pin Number	44-Pin Plastic Quad Flat Package Pin Number	Name	Description
33	37	C_{REF}^-	See pin 34.
34	38	C_{REF}^+	A 0.1 µF capacitor is used in most applications. If a large common-mode voltage exists (for example, the V_{IN}^- pin is not at analog common), and a 200 mV scale is used, a 1 µF capacitor is recommended and will hold the roll-over error to 0.5 count.
35	39	V_{REF}^-	See pin 36.
36	40	V_{REF}^+	The analog input required to generate a full-scale output (1999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full scale. Place 1V between pins 35 and 36 for 2V full scale. See paragraph on Reference Voltage.
37	41	TEST	Lamp test. When pulled high (to V+) all segments will be turned on and the display should read –1888. It may also be used as a negative supply for externally-generated decimal points. See paragraph under TEST for additional information.
38	42	OSC_3	See pin 40.
39	43	OSC_2	See pin 40.
40	44	OSC_1	Pins 40, 39 and 38 make up the oscillator section. For a 48 kHz clock (3 readings per second) connect pin 40 to the junction of a 180 kΩ resistor and a 50 pF capacitor. The 180 kΩ resistor is tied to pin 39 and the 50 pF capacitor is tied to pin 38.

GENERAL THEORY OF OPERATION

(All Pin designations refer to 40-Pin DIP)

Dual-Slope Conversion Principles

The TC7131 is a dual-slope, integrating analog-to-digital converter. An understanding of the dual-slope conversion technique will aid in following detailed TC7131 operational theory.

The conventional dual-slope converter measurement cycle has two distinct phases:

(1) Input signal integration

(2) Reference voltage integration (deintegration)

The input signal being converted is integrated for a fixed time period (t_{SI}), measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (t_{RI}).

In a simple dual-slope converter, a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

A simple mathematical equation relates the input signal, reference voltage, and integration time:

$$\frac{1}{RC}\int_0^{t_{SI}} V_{IN}(t)\,dt = \frac{V_R\,t_{RI}}{RC},$$

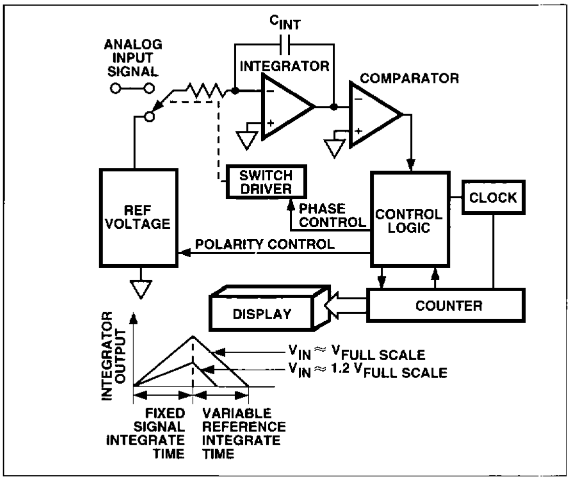


Figure 1 Basic Dual-Slope Converter

where:

V_R = Reference voltage

t_{SI} = Signal integration time (fixed)

t_{RI} = Reference voltage integration time (variable).

For a constant V_{IN}:

$$V_{IN} = V_R\left[\frac{t_{RI}}{t_{SI}}\right]$$

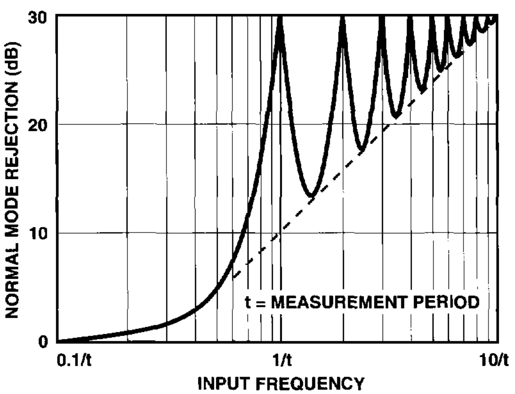


Figure 2 Normal-Mode Rejection of Dual-Slope Converter

The dual-slope converter accuracy is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. Noise immunity is an inherent benefit. Noise spikes are integrated, or averaged, to zero during integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated. Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50 Hz/60 Hz power line period.

The TC7131 is similar to the 7136 family in terms of features. A side-by -side comparison would show a difference in reference point during the conversion cycle. Specifically, the TC7131 uses IN LO only during the integrate phase, and ANALOG COMMON during the other three phases. The result is superior DC CMR for the TC7131 (120dB) at the expense of a reduced AC CMR.

ANALOG SECTION

In addition to the basic integrate and deintegrate dual-slope cycles discussed above, the TC7131 design incorporates an "integrator output-zero cycle" and an "auto-zero cycle." These additional cycles ensure that the integrator starts at 0V (even after a severe overrange conversion) and that all offset voltage errors (buffer amplifier, integrator and comparator) are removed from the conversion. A true digital zero reading is assured without any external adjustments.

A complete conversion consists of four distinct phases:

(1) Integrator output-zero phase
(2) Auto-zero phase
(3) Signal integrate phase
(4) Reference deintegrate phase

Integrator Output-Zero Phase

This phase guarantees the integrator output is at 0V before the system-zero phase is entered. This ensures that true system offset voltages will be compensated for even after an overrange conversion. The count for this phase is a function of the number of counts required by the deintegrate phase.

The count lasts from 11 to 140 counts for non-overrange conversions and from 31 to 640 counts for overrange conversions.

Auto-Zero Phase

During the auto-zero phase, the differential input signal is disconnected from the circuit by opening internal analog switches. The internal nodes are shorted to IN LO (ground) to establish a zero input condition. Additional analog switches close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on C_{AZ} compensates for device offset voltages. The auto-zero phase residual is typically 10 µV to 15 µV.

The auto-zero duration is from 910 to 2900 counts for non-overrange conversions and from 300 to 910 counts for overrange conversions.

Signal Integration Phase

The auto-zero loop is entered and the internal differential inputs connect to V_{IN}^+ and V_{IN}^-. The differential input signal is integrated for a fixed time period. The TC7131 signal integration period is 1000 clock periods or counts. The externally-set clock frequency is divided by four before clocking the internal counters. The integration time period is:

$$t_{SI} = \frac{4}{f_{OSC}} \times 1000,$$

where f_{OSC} = external clock frequency.

The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, V_{IN}^- should be tied to analog common.

Polarity is determined at the end of signal integrate phase. The sign bit is a true polarity indication, in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and auto-zero residual offsets.

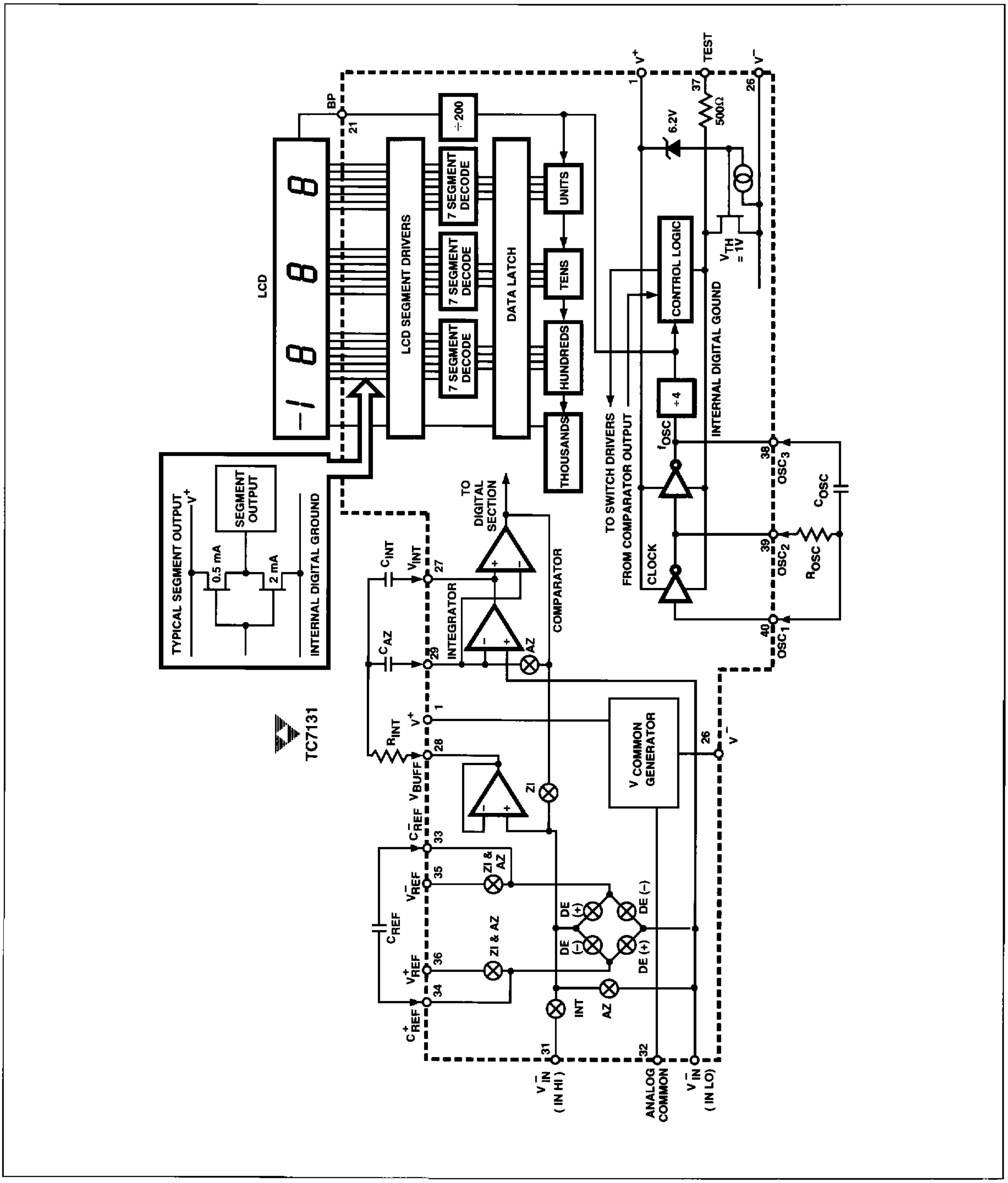


Figure 3   TC7131 Block Diagram

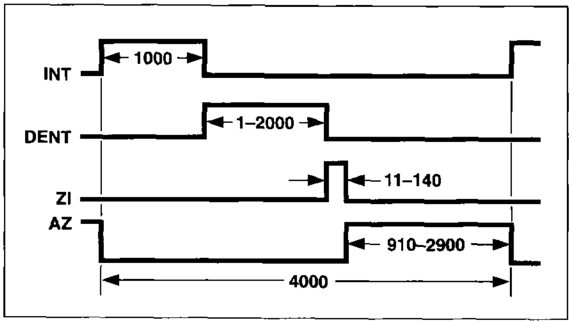


Figure 4 Conversion Timing During Normal Operation

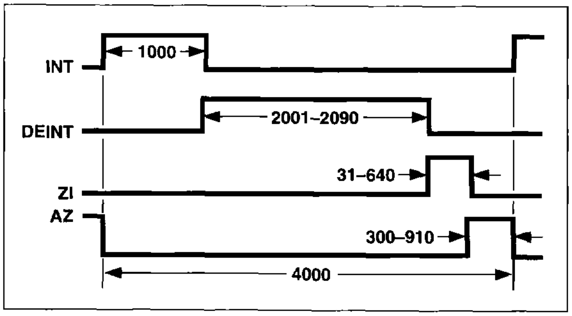


Figure 5 Conversion Timing During Overrange Operation

Reference Integrate Phase

The third phase is reference integrate or deintegrate. V_{IN}^- is internally connected to analog common and V_{IN}^+ is connected across the previously-charged reference capacitor. Circuitry within the chip ensures the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 2000 internal clock periods. The digital reading displayed is

$$1000 \frac{V_{IN}}{V_{REF}}$$

DIGITAL SECTION

The TC7131 contains all the segment drivers necessary to directly drive a 3-1/2 digit LCD. An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 800. For three conversions per second the backplane frequency is 60 Hz with a 5V nominal amplitude. When a segment driver is in-phase with the backplane signal, the segment is OFF. An out-of-phase segment drive signal causes the segment to be ON, or visible. This AC drive configuration results in negligible DC voltage across each LCD segment, ensuring long LCD life. The polarity segment driver is ON for negative analog inputs. If V_{IN}^+ and V_{IN}^- are reversed, this indicator would reverse.

On the TC7131, when the TEST pin is pulled to V^+, all segments are turned ON. The display reads –1888. During this mode the LCD segments have a constant DC voltage impressed. DO NOT LEAVE THE DISPLAY IN THIS MODE FOR MORE THAN SEVERAL MINUTES. LCDs may be destroyed if operated with DC levels for extended periods.

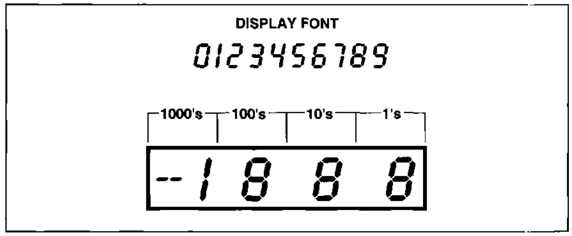


Figure 6 Display FONT and Segment Assignment

The display font and segment drive assignment are shown in Figure 6.

System Timing

The oscillator frequency is divided by 4 prior to clocking the internal decade counters. The four-phase measurement cycle takes a total of 4000 counts, or 16,000 clock pulses. The 4000-count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

(1) Auto-zero phase: 3000 to 2900 counts (1200 to 11,600 clock pulses)

(2) Signal integrate: 1000 counts (4000 clock pulses)

This time period is fixed. The integration period is:

$$t_{SI} = 4000 \left[\frac{1}{f_{OSC}}\right]$$

where f_{OSC} is the externally-set clock frequency.

(3) Reference integrate: 0 to 2000 counts

(4) Zero integrator: 11 to 640 counts

The TC7131 is a drop-in replacement for the TC7126 and ICL7126 when V_{IN}^- is tied to ANALOG COMMON.

COMPONENT VALUE SELECTION

Auto-Zero Capacitor (C_{AZ})

The C_{AZ} capacitor size has some influence on system noise. A 0.47 μF capacitor is recommended for 200 mV full-scale applications where 1 LSB is 100 μV. A 0.1 μF capacitor is adequate for 2V full-scale applications. A Mylar dielectric capacitor is adequate.

Reference Voltage Capacitor (C_{REF})

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate phase is stored on C_{REF}. A 0.1 μF capacitor is acceptable when V_{REF}^- is tied to analog common. If a large common-mode voltage exists ($V_{REF}^- \neq$ analog common) and the application requires a 200 mV full scale, increase C_{REF} to 1 μF. Roll-over error will be held to less than 0.5 count. A Mylar dielectric capacitor is adequate.

Integrating Capacitor (C_{INT})

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Analog common will normally supply the differential voltage reference in this case: a ±2V full-scale integrator output swing is satisfactory. For 3 readings per second (f_{OSC} = 48 kHz) a 0.047 μF value is suggested. For one reading per second, 0.15 μF is recommended. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ±2V integrator swing.

An exact expression for C_{INT} is:

$$C_{INT} = \frac{(4000)\left(\frac{1}{f_{OSC}}\right)\left(\frac{V_{FS}}{R_{INT}}\right)}{V_{INT}},$$

where: f_{OSC} = Clock frequency at pin 38
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing.

C_{INT} must have low dielectric absorption to minimize roll-over error. A polypropylene capacitor is recommended.

Integrating Resistor (R_{INT})

The input buffer amplifier and integrator are designed with Class A output stages. The output stage idling current is 6 μA. The integrator and buffer can supply 1 μA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region, but not so large that PC board leakage currents induce errors. For a 200 mV full scale, R_{INT} is 180 kΩ. A 2V full scale requires 1.8 MΩ.

Component	Nominal Full-Scale Voltage	
Value	**200 mV**	**2V**
C_{AZ}	0.47 μF	0.1 μF
R_{INT}	180 kΩ	1.8 MΩ
C_{INT}	0.047 μF	0.047 μF

NOTE: f_{OSC} = 48 kHz (3 readings per sec). R_{OSC} = kΩ, C_{OSC} = 50 pF.

Oscillator Components

C_{OSC} should be 50 pF. R_{OSC} is selected from the equation:

$$f_{OSC} = \frac{0.45}{RC}$$

Note that f_{OSC} is ÷ 4 to generate the TC7131's internal clock. The backplane drive signal is derived by dividing f_{OSC} by 800.

To achieve maximum rejection of 60 Hz noise pickup, the signal integrate period should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 40 kHz,etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66-2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings per second) will reject both 50 Hz and 60 Hz.

Reference Voltage Selection

A full-scale reading (2000 counts) requires the input signal be twice the reference voltage.

Required Full-Scale Voltage*	V_{REF}
200 mV	100 mV
2V	1V

*$V_{FS} = 2\ V_{REF}$.

In some applications, a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output for 2000 lb/in.^{2} is 400 mV. Rather than dividing the input voltage by two, the reference voltage should be set to 200 mV. This permits the transducer input to be used directly.

The differential reference can also be used when a digital zero reading is required when V_{IN} is not equal to zero. This is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and V_{IN}^-. The transducer output is connected between V_{IN}^+ and analog common.

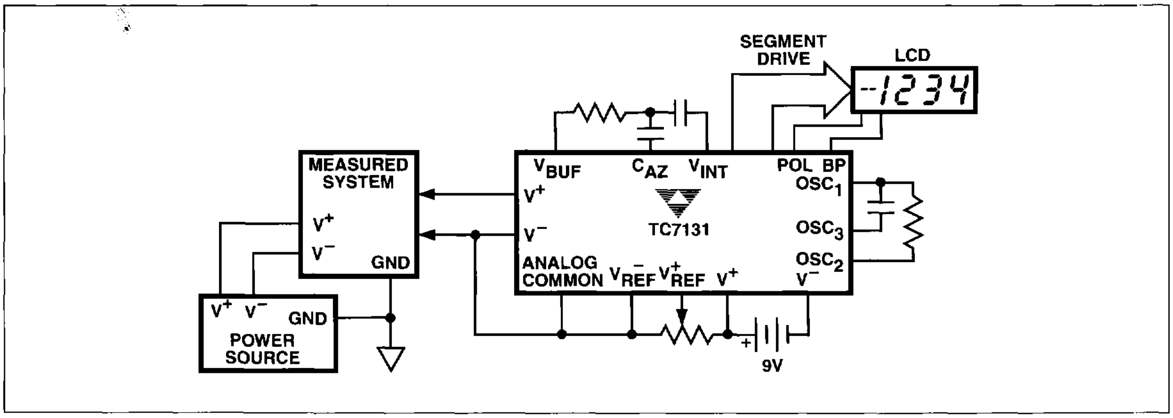


Figure 7 Common-Mode Voltage Removed in Battery Operation With V_{IN} = Analog Common

DEVICE PIN FUNCTIONAL DESCRIPTION

Differential Signal Inputs

V_{IN}^+ (Pin 31), V_{IN}^- (Pin 30)

The TC7131 is designed with true differential inputs and accepts input signals within the input stage common-mode voltage range (V_{CM}). The typical range is V^+ –1V to V^- +1V. Common-mode voltages are removed from the system when the TC7131 operates from a battery or floating power source (isolated from measured system), and V_{IN}^- is connected to ANALOG COMMON (V_{COM}). (See Figure 7.)

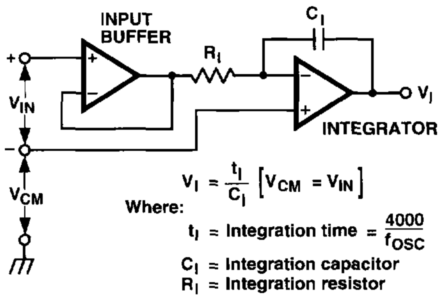
In systems where common-mode voltages exist, the 120 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. A worst-case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (see Figure 8.) For such applications, the integrator output swing can be reduced below the recommended 2V full-scale swing. The integrator output will swing within 0.3V of V^+ or V^- without increased linearity error.

Differential Reference

V_{REF}^+ (Pin 36), V_{REF}^- (Pin 35)

The reference voltage can be generated anywhere within the V^+ to V^- power supply range.

To prevent roll-over type errors being induced by large common-mode voltages, C_{REF} should be large compared to stray node capacitance.



$$V_I = \frac{t_I}{C_I}\left[V_{CM} = V_{IN}\right]$$

Where:

t_I = Integration time = $\frac{4000}{f_{OSC}}$

C_I = Integration capacitor

R_I = Integration resistor

Figure 8 Common-Mode Voltage Reduces Available Integrator Swing ($V_{COM} \neq V_{IN}$)

The TC7131 offers a significantly improved ANALOG COMMON temperature coefficient. This potential provides a very stable voltage, suitable for use as a voltage reference. The temperature coefficient of ANALOG COMMON is typically 70 ppm/°C.

ANALOG COMMON (Pin 32)

The ANALOG COMMON pin is set at a voltage potential approximately 3V below V^+. The potential is guaranteed to be between 2.7V and 3.35V below V^+. ANALOG COMMON is tied internally to an N-channel FET capable of sinking 100µA. This FET will hold the COMMON line at 3V below V^+ if an external load attempts to pull the COMMON line toward V^+. ANALOG COMMON source current is limited to 1 µA. ANALOG COMMON is therefore easily pulled to a more negative voltage (i.e., below V^+ –3V).

The ANALOG COMMON pin serves to set the analog section reference, or COMMON point. The TC7131 is specifically designed to operate from a battery or in any measurement system where input signals are not referenced (float) with respect to the TC7131 power source. The ANALOG COMMON potential of $V^+ - 3V$ gives a 7V end of battery life voltage. The COMMON potential has a 0.001%/% voltage coefficient.

TEST (Pin 37)

The TEST pin potential is 5V less than V^+. TEST may be used as the negative power supply connection for external CMOS logic. The TEST pin is tied to the internally-generated negative logic supply through a 500Ω resistor. The TEST pin load should not be more than 1 mA. See the Applications Section for additional information on using TEST as a negative digital logic supply.

If TEST is pulled high (to V^+), all segments plus the minus sign will be activated. DO NOT OPERATE IN THIS MODE FOR MORE THAN SEVERAL MINUTES. With TEST = V^+, the LCD segments are impressed with a DC voltage which will destroy the LCD.

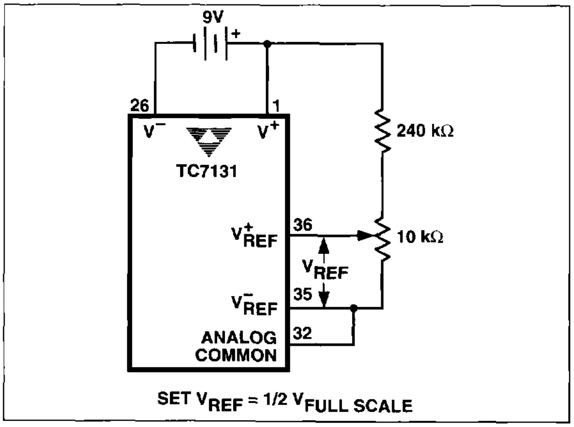


Figure 9 TC7136A Internal Voltage Reference Connection

APPLICATIONS INFORMATION

Liquid Crystal Display Sources

Several manufacturers supply standard LCDs to interface with the TC7131 3-1/2 digit analog-to-digital converter applications information

Manufacturer	Address/Phone	Representative Part Numbers*
Crystaloid Electronics	5282 Hudson Dr., Hudson, OH 44236 216-655-2429	C5335, H5535, T5135, SX440
AND	770 Airport Blvd., Burlingame, CA 94010 415-347-9916	FE 0801, FE 0203
VGI, Inc.	1800 Vernon St., Ste. 2 Roseville, CA 95678 916-783-7878	I1048, I1126
Hamlin, Inc.	612 E. Lake St., Lake Mills, WI 53551 414-648-2361	3902, 3933, 3903

*NOTE: Contact LCD manufacturer for full product listing/specifications.

Decimal Point and Annunciator Drive

The TEST pin is connected to the internally-generated digital logic supply ground through a 500Ω resistor. The TEST pin may be used as the negative supply for external CMOS gate segment drivers. LCD annunciators for decimal points, low battery indication, or function indication may be added without adding an additional supply. No more than 1 mA should be supplied by the TEST pin; its potential is approximately 5V below V^+.

Ratiometric Resistance Measurements

The TC7131's true differential input and differential reference make ratiometric readings possible. In ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately-defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input and the voltage across the known resistor applied to the reference input. If the unknown equals the standard, the display will read 1000. The displayed reading can be determined from the following expression:

$$\text{Displayed reading} = \frac{R_{UNKNOWN}}{R_{STANDARD}} \times 1000.$$

The display will overrange for $R_{UNKNOWN} \geq 2 \times R_{STANDARD}$.

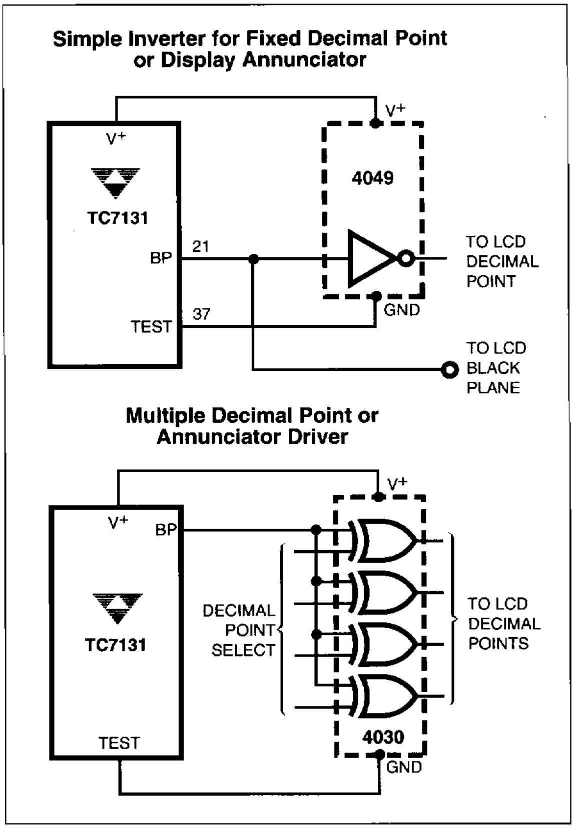


Figure 10 Decimal Point and Annunciator Drives

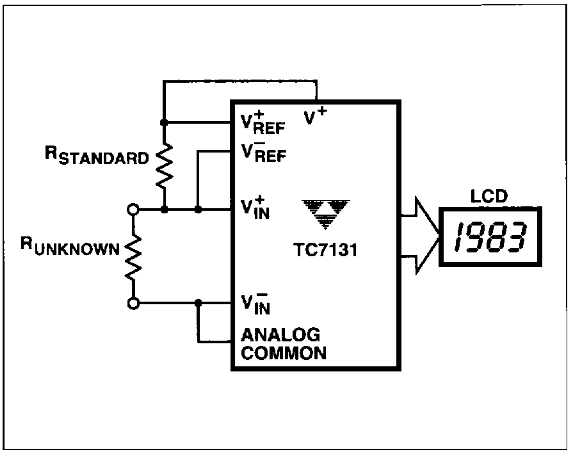


Figure 11 Low Parts Count Ratiometric Resistance Measurement

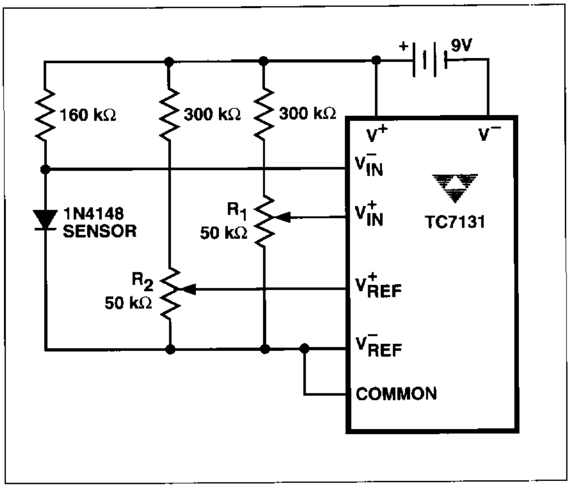


Figure 12 Temperature Sensor