

54F/74F673A

16-Bit Serial-In, Serial/Parallel-Out Shift Register

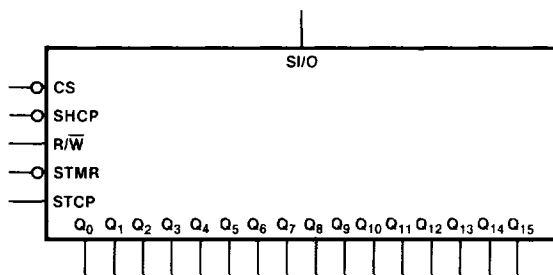
Description

The 'F673A contains a 16-bit serial-in, serial-out shift register and a 16-bit parallel-out storage register. A single pin serves either as an input for serial entry or as a 3-state serial output. In the Serial-out mode, the data recirculates in the shift register. By means of a separate clock, The contents of the shift register are transferred to the storage register for parallel outputting. The contents of the storage register can also be parallel loaded back into the shift register. A HIGH signal on the Chip Select input prevents both shifting and parallel transfer. The storage register may be cleared via $\overline{\text{STMR}}$.

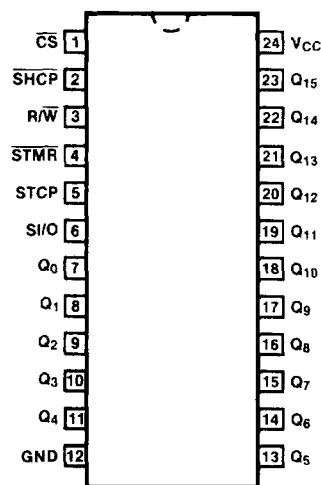
- Serial-to-Parallel Converter
- 16-Bit Serial I/O Shift Register
- 16-Bit Parallel-Out Storage Register
- Recirculating Serial Shifting
- Recirculating Parallel Transfer
- Common Serial Data I/O Pin
- SIlm 24 Lead Package

Ordering Code: See Section 5

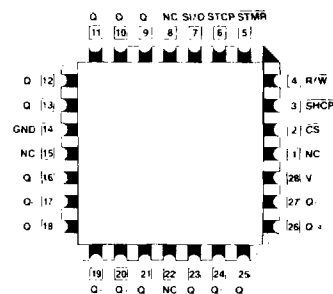
Logic Symbol



Connection Diagrams



Pin Assignment
for DIP and SOIC



Pin Assignment
for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{\text{CS}}$	Chip Select Input (Active LOW)	0.5/0.375
$\overline{\text{SHCP}}$	Shift Clock Pulse Input (Active Falling Edge)	0.5/0.375
$\overline{\text{STMR}}$	Store Master Reset Input (Active LOW)	0.5/0.375
$\overline{\text{STCP}}$	Store Clock Pulse Input	0.5/0.375
$\overline{\text{R/W}}$	Read/Write Input	0.5/0.375
S/I/O	Serial Data Input or 3-State Serial Output	1.75/0.375 75/15 (12.5)
Q_0 - Q_{15}	Parallel Data Outputs	25/12.5

Functional Description

The 16-bit shift register operates in one of four modes, as indicated in the Shift Register Operations Table. A HIGH signal on the Chip Select (\overline{CS}) input prevents clocking and forces the Serial Input/Output (SI/O) 3-state buffer into the high impedance state. During serial shift-out operations, the SI/O buffer is active (i.e., enabled) and the output data is also recirculated back into the shift register. When parallel loading the shift register from the storage register, serial shifting is inhibited.

The storage register has an asynchronous master reset (\overline{STMR}) input that overrides all other inputs and forces the Q_0 - Q_{15} outputs LOW. The storage register is in the Hold mode when either \overline{CS} or the Read/Write (R/\overline{W}) input is HIGH. With \overline{CS} and R/\overline{W} both LOW, the storage register is parallel loaded from the shift register.

Shift Register Operations Table

Control Inputs				S/I/O Status	Operating Mode
\overline{CS}	R/\overline{W}	\overline{SHCP}	STCP		
H L	X L	X	X X	High Z Data In	Hold Serial Load
L	H	↓	L	Data Out	Serial Output with Recirculation
L	H	↓	H	Active	Parallel Load; No Shifting

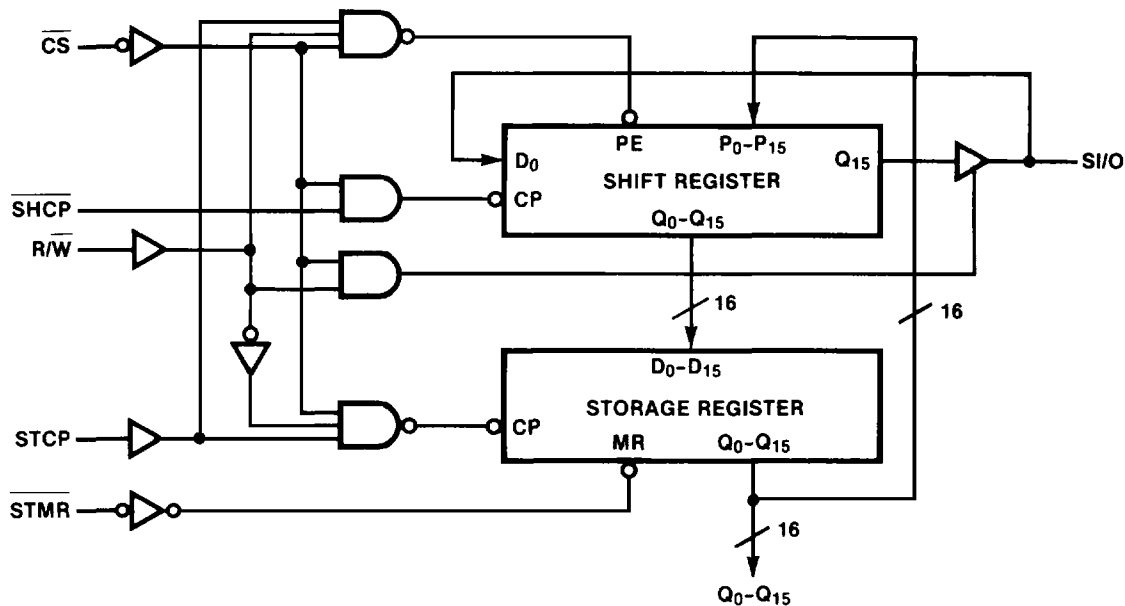
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↓ = HIGH-to-LOW Transition

Storage Register Operations Table

Control Inputs				Operating Mode
\overline{STMR}	\overline{CS}	R/\overline{W}	STCP	
L	X	X	X	Reset; Outputs LOW
H	H	X	X	Hold
H	X	H	X	Hold
H	L	L	↓	Parallel Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↓ = LOW-to-HIGH Transition

Block Diagram



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DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I _{CC}	Power Supply Current		106	160	mA	V _{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A , V _{CC} = Mil C _L = 50 pF		T _A , V _{CC} = Com C _L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f _{max}	Maximum Clock Frequency	100	130			85		MHz	3-1	
t _{PLH} t _{PHL}	Propagation Delay STCP to Q _n	3.0	8.0	10.5		2.5	12.0	ns	3-1 3-7	
t _{PHL}	Propagation Delay STMR to Q _n	6.5	16.5	20.5		5.5	22.5	ns	3-1 3-11	
t _{PLH} t _{PHL}	Propagation Delay SHCP to SI/O	4.0	6.5	8.5		3.5	9.5	ns	3-1 3-8	
t _{PZH} t _{PZL}	Output Enable Time \overline{CS} or R/W to SI/O	5.0	8.5	11.0		4.0	12.5	ns	3-1 3-12 3-13	
t _{PHZ} t _{PLZ}	Output Disable Time \overline{CS} or R/W to SI/O	3.5	5.5	7.5		3.0	8.5			
t _{PZH} t _{PZL}	Output Enable Time R/W to SI/O	4.5	7.5	9.5		4.0	10.5	ns	3-1 3-12 3-13	
t _{PHZ} t _{PHL}	Output Disable Time R/W to SI/O	3.0	5.5	7.0		2.5	8.0			
		2.5	4.0	5.5		2.0	6.5			

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$			$T_A, V_{CC} =$ Mil		$T_A, V_{CC} =$ Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW \overline{CS} or R/\overline{W} to STCP	3.5					4.0	7.0	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW \overline{CS} or R/\overline{W} to STCP	0					0	0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW S/I/O to \overline{SHCP}	3.0					3.5	3.5	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW S/I/O to \overline{SHCP}	3.0					3.5	3.5		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW \overline{CS} to \overline{SHCP}	3.0					3.5	3.5	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW \overline{CS} to \overline{SHCP}	3.0					3.5	3.5		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW R/\overline{W} to \overline{SHCP}	6.5					7.5	10.0	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW R/\overline{W} to \overline{SHCP}	0					0	0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW STCP to SHCP	7.0					8.0	8.0	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW STCP to SHCP	0					0	0		
$t_s(L)$	Setup Time, LOW \overline{SHCP} to STCP	7.5					8.5		ns	3-6
$t_h(H)$	Hold Time, HIGH \overline{SHCP} to STCP	0					0			
$t_w(H)$ $t_w(L)$	\overline{SHCP} Pulse Width HIGH or LOW	4.0					4.5	6.5	ns	3-8
$t_w(H)$ $t_w(L)$	STCP Pulse Width HIGH or LOW	3.5					4.0	4.0	ns	3-7
$t_w(L)$	\overline{STMR} Pulse Width, LOW	7.5					8.5		ns	3-11
t_{rec}	Recovery Time \overline{STMR} to STCP	2.5					3.0		ns	3-11