Signetics

FAST Products

FAST 74F655A, 74F656A
Buffers/Drivers

Octal Buffers/Line Drivers with Parity
('F655A – Inverting 3-State)
('F656A – Non-Inverting 3-State)
Product Specification

FEATURES

- **Significantly improved AC performance over 'F655 and 'F656**
- **High-impedance NPN base input for reduced loading (20μA in High and Low states)**
- **Ideal in applications where high output drive and light bus loading are required (I_{IL} is 20μA vs FAST std of 600μA)**
- **'F655A combines 'F240 and 'F280 functions in one package**
- **'F656A combines 'F244 and 'F280A functions in one package**
- **'F655A Inverting**
  'F656A Non-Inverting
- **3-State outputs sink 64mA**
- **Inputs source 15mA**
- **24-pin plastic Slim DIP (300mil) package**
- **Inputs on one side and outputs on the other side simplify PC board layout**
- **Combined functions reduce part count and enhance system performance**

DESCRIPTION

The 'F655A and 'F656A are octal buffers and line drivers with parity generation/checking designed to be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F655A	6.5ns	64mA
74F656A	6.5ns	64mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP	N74F655AN, N74F656AN
24-Pin Plastic SOL	N74F655AD, N74F656AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

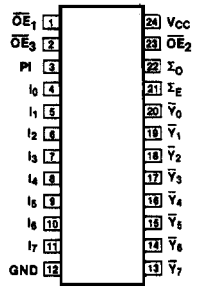
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_n	Data inputs	2.0/0.066	40μA/40μA
PI	Parity input	1.0/0.033	20μA/20μA
$\overline{OE}_1$, $\overline{OE}_2$ $\overline{OE}_3$	3-State output enable inputs (active-Low)	1.0/0.033	20μA/20μA
$\overline{Y}_n$	Data outputs ('F655A)	750/106.7	15mA/64mA
Y_n	Data outputs ('F656A)	750/106.7	15mA/64mA
Σ_E, Σ_O	Parity outputs	750/106.7	15mA/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

6

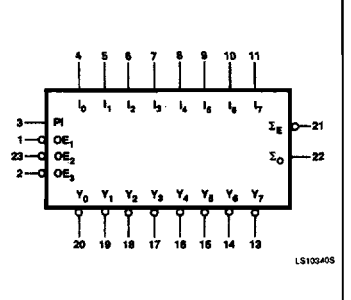
PIN CONFIGURATION

'F655A



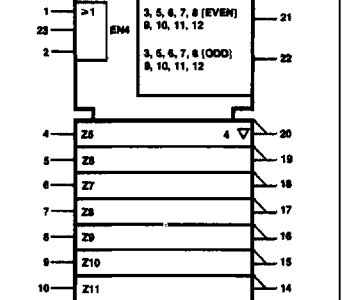
LOGIC SYMBOL

'F655A



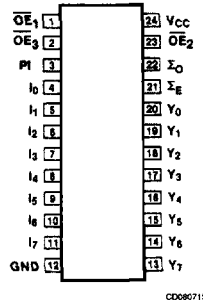
LOGIC SYMBOL (IEEE/IEC)

'F655A



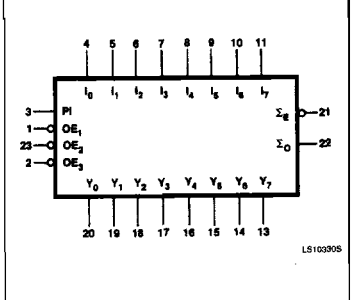
PIN CONFIGURATION

'F656A



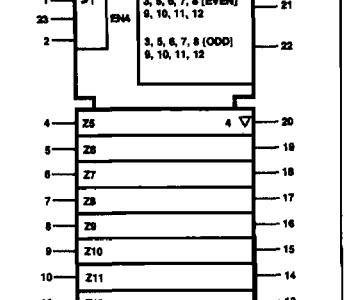
LOGIC SYMBOL

'F656A

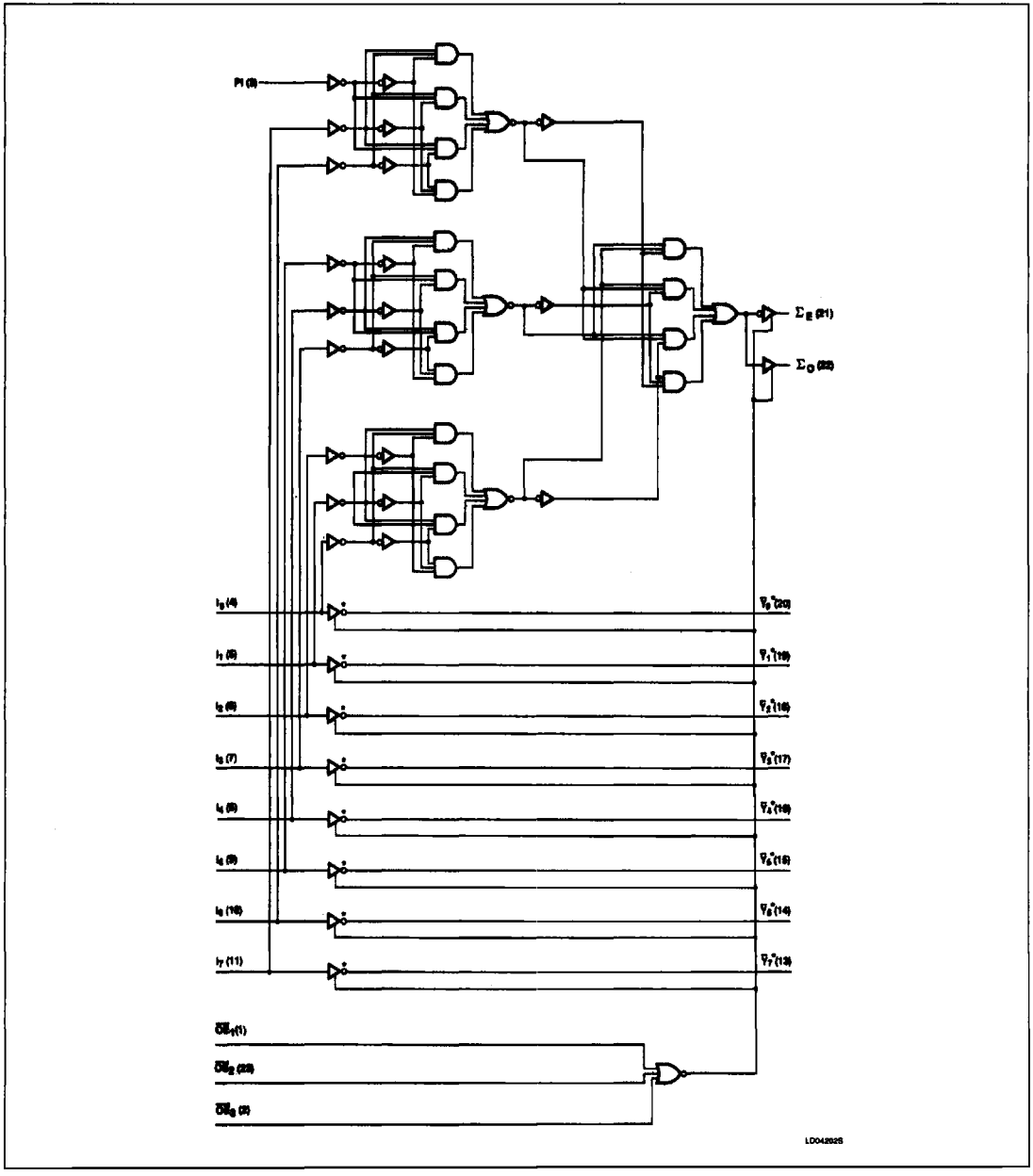


LOGIC SYMBOL (IEEE/IEC)

'F656A



LOGIC DIAGRAM FOR 'F655A
(Non-inverting for 'F656A Indicated by Symbol *)



FUNCTION TABLE

INPUTS				DATA OUTPUTS	
$\overline{OE}_1$	$\overline{OE}_2$	$\overline{OE}_3$	I_n	'655A	'656A
L	L	L	L	H	L
L	L	L	H	L	H
H	X	X	X	Z	Z
X	H	X	X	Z	Z
X	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance state

INPUTS	PARITY OUTPUTS	
Number of inputs High (PI, $I_0 - I_7$)	Σ_E	Σ_O
EVEN – 0, 2, 4, 6, 8	H	L
ODD – 1, 3, 5, 7, 9	L	H
Any $\overline{OE}$ = High	Z	Z

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F655A, 'F655A			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = −15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.35	0.50	V
				I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input clamp current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	I_n	V_{CC} = MAX, V_I = 2.7V					40	µA
		PI, $\overline{OE}_n$						20	µA
I_{IL}	Low-level input current	I_n	V_{CC} = MAX, V_I = 0.5V					−40	µA
		PI, $\overline{OE}_n$						−20	µA
I_{OZH}	OFF-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	OFF-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					−50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX, V_O = 0.0V			−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				50	80	mA
		I_{CCL}					78	110	mA
		I_{CCZ}					63	90	mA

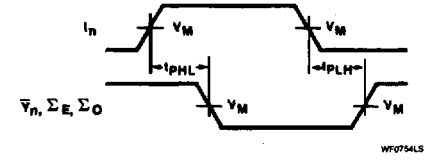
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

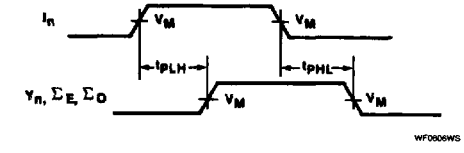
SYMBOL	PARAMETER		TEST CONDITIONS	74F655A, 656A					UNIT
				T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay I_n to $\overline{Y}_n$	'F655A	Waveform 1	2.0	4.5	6.5	2.0	7.5	ns
t_{PHL}				1.0	2.5	4.0	1.0	4.5	
t_{PLH}	Propagation delay I_n to Y_n	'F656A	Waveform 2	2.0	4.0	6.5	2.0	7.0	ns
t_{PHL}				2.5	5.5	7.0	2.5	7.5	
t_{PLH}	Propagation delay I_n to Σ_E, Σ_O		Waveform 1, 2	5.5	10.0	13.0	5.5	14.0	ns
t_{PHL}				5.5	11.0	14.5	5.5	16.5	
t_{PZH}	Output enable time to High or Low level		Waveform 3	4.0	7.0	10.5	4.0	11.5	ns
t_{PZL}			Waveform 4	4.0	8.0	11.0	4.0	12.0	
t_{PHZ}	Output disable time from High or Low level		Waveform 3	1.5	4.5	8.0	1.5	9.0	ns
t_{PLZ}			Waveform 4	2.0	5.0	8.0	2.0	9.0	

6

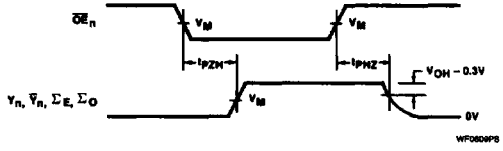
AC WAVEFORMS



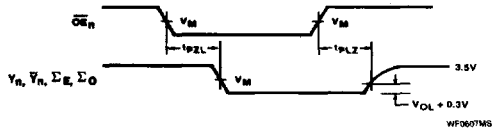
Waveform 1. Clock to Output Delays and Clock Pulse Width



Waveform 2. Propagation Delay for I_n to Y_n, Σ_E, Σ_O



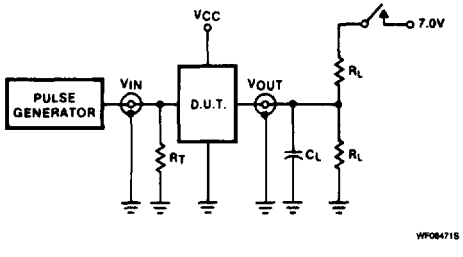
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level



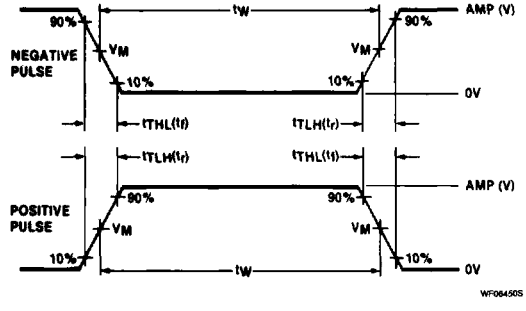
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V.

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.