FUJITSU

262144×9 BIT DYNAMIC RANDOM ACCESS MEMORY MODULE

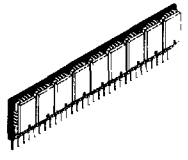
MB85227-10
MB85227-12
MB85227-15

December 1987
Edition 2.0

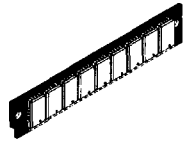
262,144 x 9-BIT DYNAMIC RANDOM ACCESS MEMORY SIP MODULE

This Fujitsu MB85227 is a fully decoded, 262,144 words x 9 bits NMOS dynamic random access memory composed of nine 256K DRAM chips (MB81256 x 9). Assembling nine PLCC chips on a 30 pin PCB, this RAM module is optimized for the applications where high-density and large capacity of storage memory with parity bit is needed.
The electrical characteristics of the MB85227 are the same as the original MB81256; each timing requirements are noncritical, and power supply tolerance is very wide. All inputs and outputs are TTL compatible.

- 262,144 x 9 DRAM, 30-pin SIP (MB81256 x 9)
- Row access time (t_{RAC}),
  100 ns max. (MB85227-10)
  120 ns max. (MB85227-12)
  150 ns max. (MB85227-15)
- Cycle time (t_{RC}),
  200 ns min. (MB85227-10)
  220 ns min. (MB85227-12)
  260 ns min. (MB85227-15)
- Page Cycle Time (t_{PC}),
  100 ns min (MB85227-10)
  120 ns min (MB85227-12)
  150 ns min. (MB85227-15)
- Single +5V supply, ±10% tolerance
- Low power (active)
  3465 mW max. (MB85227-10)
  3213 mW max. (MB85227-12)
  2822 mW max. (MB85227-15)
  226 mW max. (Standby)
- 4 ms/256 refresh cycles capability
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$ and Hidden refresh capability
- Page Mode Capability
- On-chip latches for Addresses and Data-in
- Leaded and Leadless types are available
- Compatible with TM4256EL9/TM4256EU9 and MH25609J
- Standard Leaded Epoxy SIP (Suffix: PDPS)
- Standard Leadless Epoxy SIM (Suffix: PDPB)

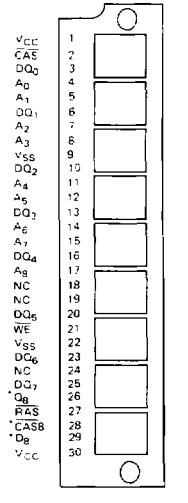


PLASTIC PACKAGE
MSP-30P-P02



PLASTIC PACKAGE
MSS-30P-P01

PIN ASSIGNMENT



* : For parity bit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Storage temperature	T_{STG}	−55 to 125	°C
Power dissipation	P_D	4.5	W
Short circuit output current	—	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

Fig. 1 – FUNCTIONAL BLOCK DIAGRAM

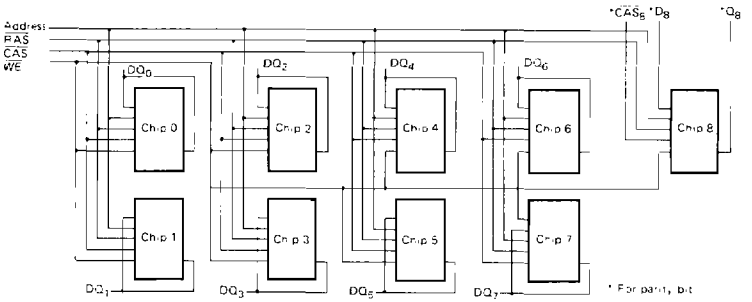
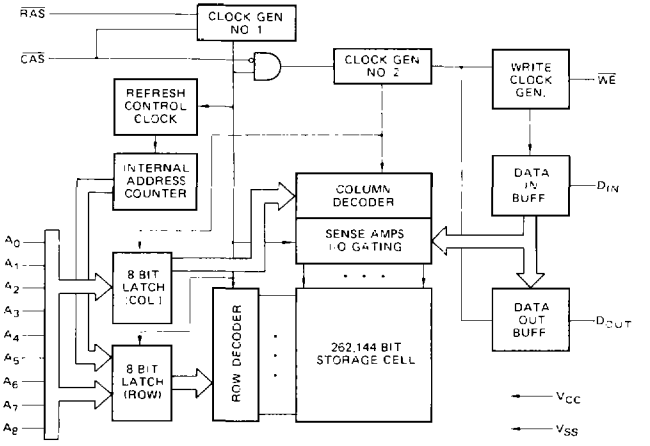


Fig. 2 – BLOCK DIAGRAM FOR EACH CHIP



CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A_0 to A_8	C_{IN1}		75	pF
Input Capacitance, $\overline{RAS}$	C_{IN2}		80	pF
Input Capacitance, $\overline{CAS}$	C_{IN3}		70	pF
Input Capacitance, $\overline{WE}$	C_{IN4}		55	pF
Input Capacitance, $\overline{CAS8}$	C_{IN5}		10	pF
Input Capacitance, D_8	C_{IN6}		7	pF
I/O Capacitance, DQ_0 to DQ_7	C_D		17	pF
Output Capacitance, Q_8	C_O		12	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V	0°C to +70°C*
Input High Voltage	V_{IH}	2.4	–	6.5	V	
Input Low Voltage	V_{IL}	-2.0	–	0.8	V	

Note * : Maximum ambient temperature is permissible under certain conditions.
See the derating curve Fig. 3 for normal cycle, and Fig. 4 for page mode cycle.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$, $\overline{CAS8}$ cycling; t_{RC} = Min.)	MB85227-10	I_{CC1}		630	mA
	MB85227-12			585	
	MB85227-15			513	
STANDBY CURRENT Standby Power Supply Current ($\overline{RAS}$ = $\overline{CAS}$ = $\overline{CAS8}$ = V_{IH})		I_{CC2}		41	mA
REFRESH CURRENT 1* Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS}$, $\overline{CAS8}$ = V_{IH}; t_{RC} = Min.)	MB85227-10	I_{CC3}		540	mA
	MB85227-12			495	
	MB85227-15			450	
PAGE MODE CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, $\overline{CAS8}$ cycling; t_{PC} = Min.)	MB85227-10	I_{CC4}		315	mA
	MB85227-12			270	
	MB85227-15			225	
REFRESH CURRENT 2* Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = Min.)	MB85227-10	I_{CC5}		585	mA
	MB85227-12			540	
	MB85227-15			495	
INPUT LEAKAGE CURRENT (Except for DQ_0 to DQ_7) Input Leakage Current, Any Input ($0 \leqq V_{IN} \leqq 5.5V$, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)		$I_{I(L)1}$ ($\overline{CAS8}$, D8)	-10	10	μA
		$I_{I(L)2}$ (Others)	-90	90	
DQ and Q8 LEAKAGE CURRENT (Data out is disabled, $0V \leqq V_{OUT} \leqq 5.5V$) Each DQ is high impedance		$I_{O(L)}$	-10	10	μA
OUTPUT LEVELS Output High Voltage (I_{OH} = -5 mA) Output Low Voltage (I_{OL} = -4.2 mA)		V_{OH} V_{OL}	2.4	0.4	V

Note 1): I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

4

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1, 2, 3

Parameter	NOTES	Symbol	MB85227-10		MB85227-12		MB85227-15		Unit
			Min	Max	Min	Max	Min	Max	
Time between Refresh		t_{REF}		4		4		4	ms
Random Read/Write Cycle Time	4	t_{RC}	200		220		260		ns
Access Time from $\overline{RAS}$	5, 6	t_{RAC}		100		120		150	ns
Access Time from $\overline{CAS}$	6, 7	t_{CAC}		50		60		75	ns
Output Buffer Turn off Delay		t_{OFF}	0	25	0	25	0	30	ns
Transition Time		t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	85		90		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	105	100000	120	100000	150	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	55		60		75		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	55	100000	60	100000	75	100000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	105		120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delat Time	8, 9	t_{RCD}	20	50	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	10		10		10		ns
Row Address Set Up Time		t_{ASR}	0		0		0		ns
Row Address Hold Time		t_{RAH}	10		12		15		ns
Column Address Set Up Time		t_{ASC}	0		0		0		ns
Column Address Hold Time		t_{CAH}	15		20		25		ns
Read Command Set Up Time		t_{RCS}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	10	t_{RCH}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	10	t_{RRH}	20		20		20		ns
Write Command Set Up Time		t_{WCS}	0		0		0		ns
Write Command Pulse Width		t_{WP}	15		20		25		ns
Write Command Hold Time		t_{WCH}	15		20		25		ns
Data In Set Up Time		t_{DS}	0		0		0		ns
Data In Hold Time		t_{DH}	15		20		25		ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCS}	20		20		20		ns
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCH}	20		25		30		ns

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

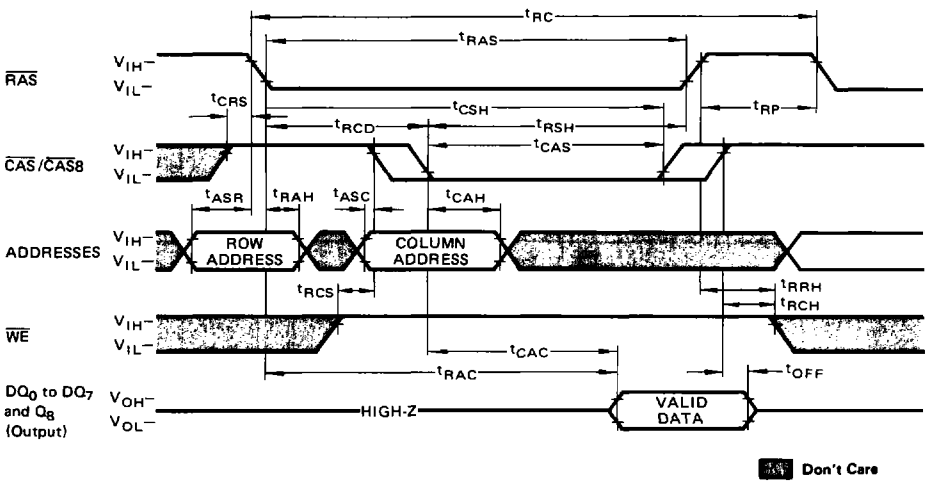
Parameter	NOTES	Symbol	MB85227-10		MB85227-12		MB85227-15		Unit
			Min	Max	Min	Max	Min	Max	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	20		20		20		ns
Page Mode Read/Write Cycle Time	11	t_{PC}	100		120		150		ns
Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	40		50		65		ns
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{CPR}	20		25		30		ns
Write Command to $\overline{RAS}$ Lead Time	12	t_{RWL}	40		50		60		ns
Write Command to $\overline{CAS}$ Lead Time	12	t_{CWL}	40		50		60		ns
$\overline{CAS}$ to $\overline{WE}$ Delay Time	12	t_{CWD}	15		20		25		ns
Read-Write Cycle Time	12	t_{RWC}	200		220		260		ns

4

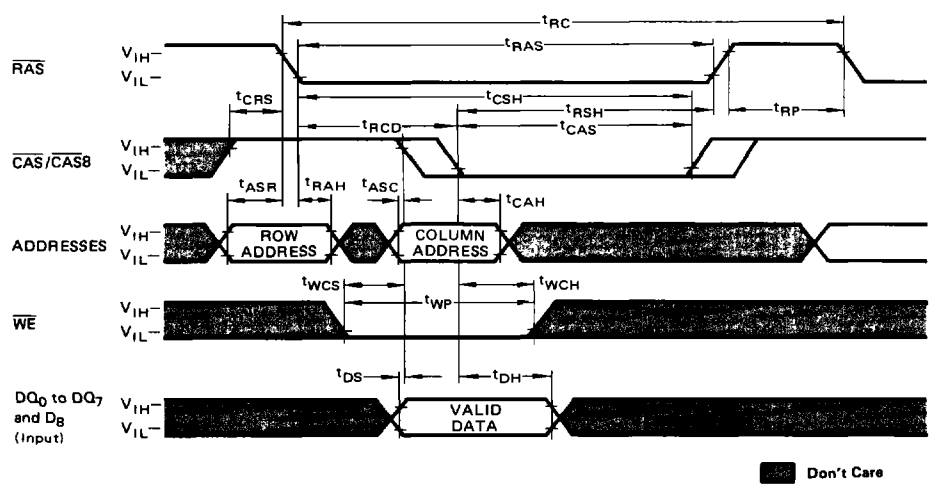
Notes:

1. An initial pause of 200 μs is required after power-up. And then several cycle (to which any 8 cycle to perform refresh are adequate) are required before proper device operation is achieved.
   If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
2. AC characteristics assume t_T = 5 ns.
3. V_{IH} (min) and V_{IL} (max) are refrence levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. The minimum cycle time is dependent on the ambient temperature and cooling conditions.
   See Fig. 3 for durating curve.
5. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
8. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. t_{RCD} (min) = t_{RAH} (min) + 2t_T (t_T = 5 ns) + t_{ASC} (min).
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. The minimum cycle time is dependent on the ambient temperature and cooling conditions.
    See Fig. 4 for derating curve.
12. Only for parity bit.

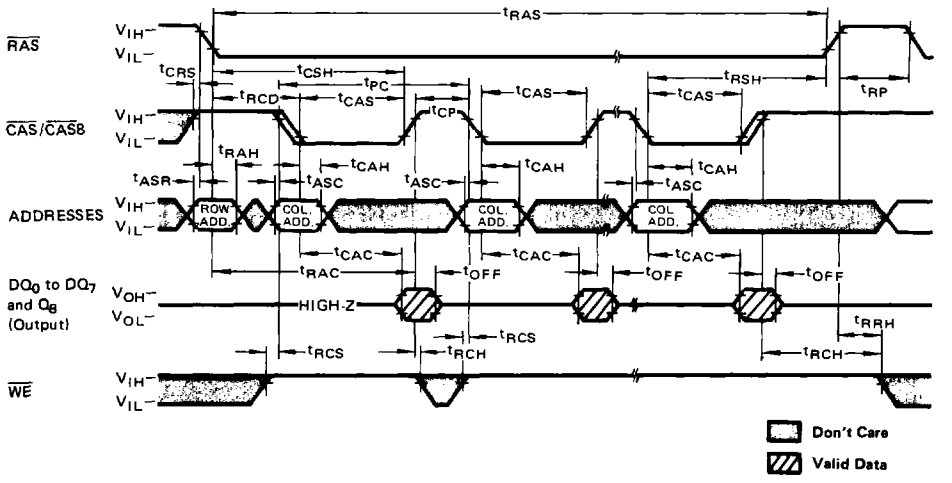
Read Cycle



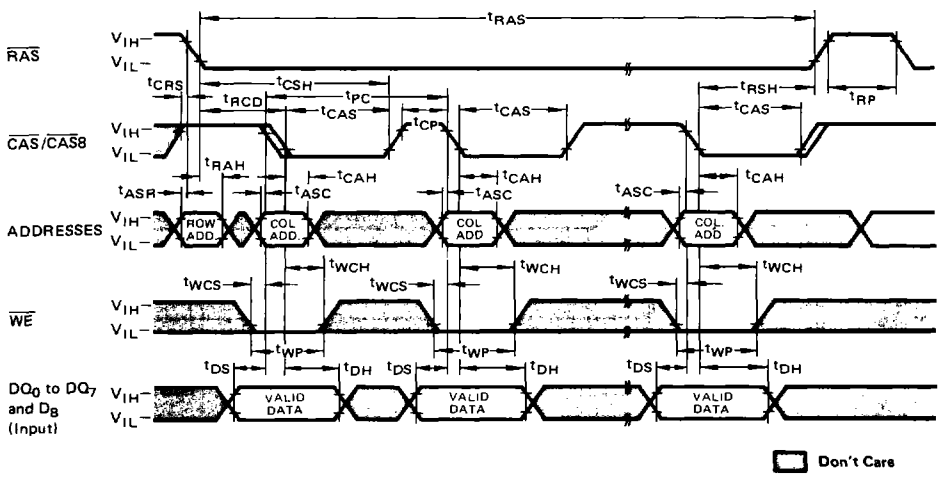
Write Cycle



Page Mode Read Cycle



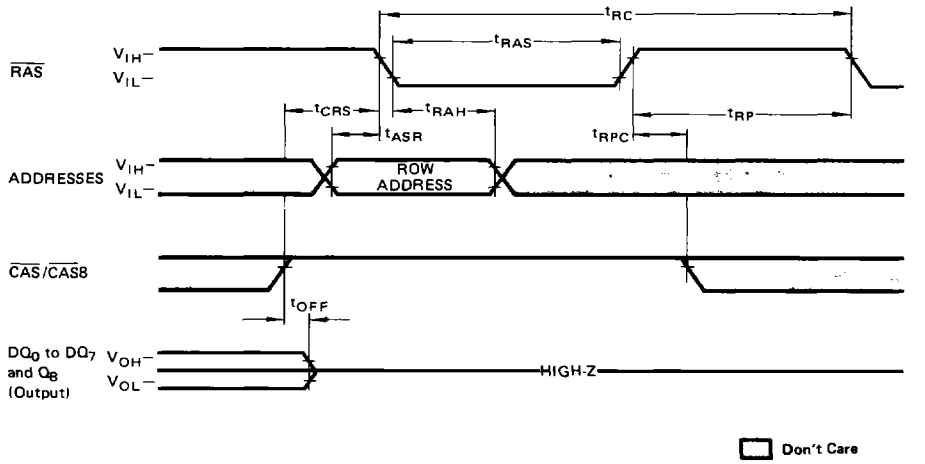
Page Mode Write Cycle



4

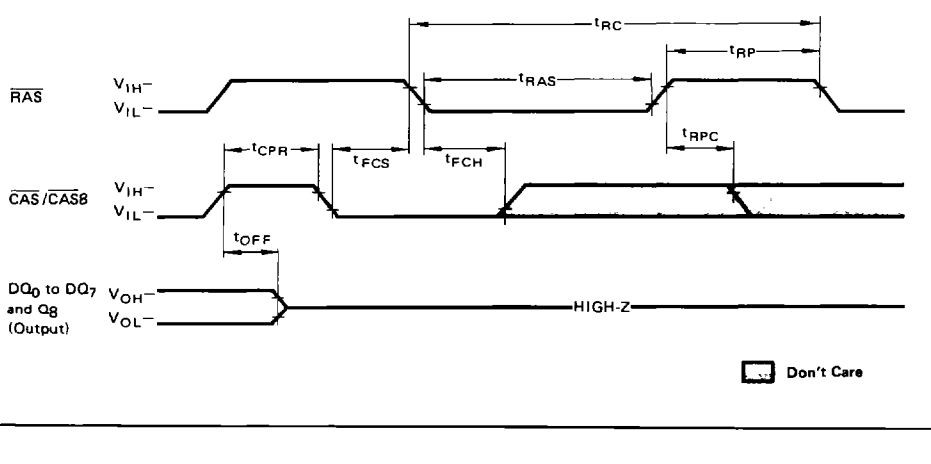
$\overline{RAS}$-only Refresh Cycle

NOTE: $\overline{WE}$, and D_8 = Don't Care

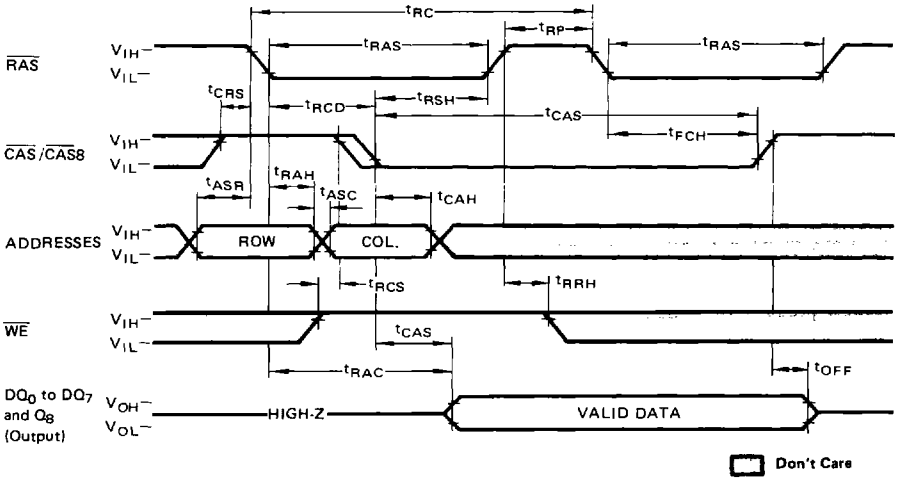


$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

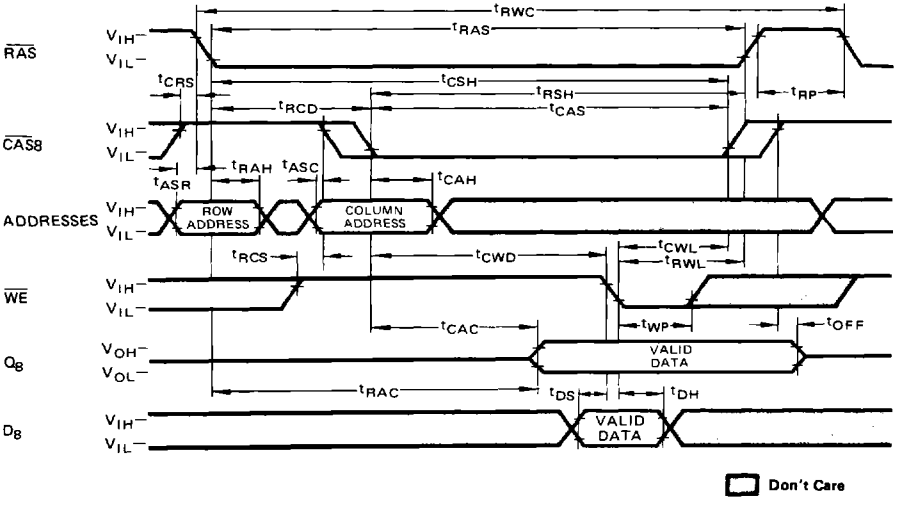
NOTE: Address, $\overline{WE}$, and D_8 = Don't Care



Hidden Refresh Cycle



Read–Write/Read–Modify–Write Cycle*



* ; Only for parity bit.

FUNCTIONAL TRUTH TABLE

$\overline{RAS}$	$\overline{CAS}$ and $\overline{CAS_8}$	$\overline{WE}$	DQ_0 to DQ_7, D_8 and Q_8	Function
H	H	Don't Care	High-Z	Standby
L	L	H	Valid Data Out[1]	Ready cycle
L	L	L	Valid Data In[2]	Write cycle
L	L[3]	Don't Care	High-Z	$\overline{CAS}$-before $\overline{RAS}$ Refresh cycle
L	H	Don't Care	High-Z	$\overline{RAS}$-only Refresh cycle
L	H ($\overline{CAS}$) L ($\overline{CAS_8}$)	H → L[4]	High-Z (DQ_0 to DQ_7) Valid Data In (D_8) Valid Data Out (Q_8)	$\overline{RAS}$-only Refresh cycle (Except for Pairyt bit) Read-Write/Read-Modify-Write (Parity bit)

Notes: 1): DQ Pins are output mode.
2): DQ pins are input mode.
3): $t_{FCS} \geqq t_{FCS}$ (min)
4): $t_{CWD} \geqq t_{CWD}$ (min)

DESCRIPTION

Simple Timing Requirement:
The MB 85227 has improved circuitry that eases timing requirements for high speed access operations. The MB 85227 can operate under the condition of t_{RCD} (max) = t_{CAC} thus providing optimal timing for address multiplexing. In addition, the MB 85227 has the minimal hold times of address (t_{CAH}), $\overline{WE}$ (t_{WCH}) and D_{IN} (t_{DH}). The MB 85227 provides higher throughput in interleaved memory system applications. Fujitsu has made timing requirement that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, and t_{DHR}. As a result, the hold times of the column address, D_{IN} and $\overline{WE}$ are not restricted by t_{RCD}.

Address Inputs:
A total of eighteen binary input address bits are required to decode any 9 bits data of 2359296 storage cells within the MB 85227.
Nine row address bits are established on the input pin (A_0 through A_8) and latched with $\overline{RAS}$.
Nine columns address bits are established on the input pins and latched with $\overline{CAS}$ and $\overline{CAS8}$. All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ and $\overline{CAS8}$ are internally inhibited by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ and $\overline{CAS8}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

Write Enable:
The read mode or write mode is selected with the $\overline{WE}$ input. A high on the $\overline{WE}$ selects read mode, low selects write mode. Data inputs are disabled when read mode is selected.

Data Pins:
The input and output pins of each PLCC except for parity bit are directly connected on the mother board to minimized the number of I/O pins. The write cycle should be early write cycle in order to avoid data conflict between output data and input data. However, it is possible to execute read-modify-write cycle on the parity bit because the input & output of parity bit are separated.

Data Input:
The 9 bits data are written through the DQ pins (DQ_0 to DQ_7 and D_8) during write (early write) cycle.
The falling edge of $\overline{CAS}$ and $\overline{CAS8}$ are triggered for the data input register. The set up and hold times are referenced to $\overline{CAS}$ and $\overline{CAS8}$.

Data Output:
The output buffer of each chips are three state TTL compatible with a fan out of two standard TTL loads.
The outputs are in high impedance state until $\overline{CAS}$ and $\overline{CAS8}$ are brought low. In a read cycle, the output is valid after t_{RAC} from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from the falling edge of $\overline{CAS}$ and $\overline{CAS8}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ and $\overline{CAS8}$ are returned to a high level.

Page-Mode:
Page-mode operation permits strobing the row-address into the MB 85227 while maintaining $\overline{RAS}$ at low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the falling edge of $\overline{RAS}$ is saved. Access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

Refresh:
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each 256 row address (A_0 through A_7 of the at least every 4 ms. During refresh, either V_{IL} or V_{IH} is permitted for A_8.
The MB 85227 offers the following three types of refresh.
1) $\overline{RAS}$-only Refresh;
   $\overline{RAS}$ Only refresh avoids any output during refresh because the output buffer is in high impedance state unless $\overline{CAS}$ and $\overline{CAS8}$ are brought low. Strobing each of 256 row addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed.
2) $\overline{CAS}$-before-$\overline{RAS}$ Refresh;
   $\overline{CAS}$-before-$\overline{RAS}$ refresh available on the MB 85227 offers an alternate refresh method. If $\overline{CAS}$ and $\overline{CAS8}$ are held low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter on each chip are enabled, and an internal refresh operation takes place. After the refresh operation has been executed the refresh address counter is automatically incremented for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. So, by performing 256 cycles for $\overline{CAS}$-before-$\overline{RAS}$ refresh, all bits in a module are refreshed.
3) Hidden Refresh;
   Hidden refresh may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ and $\overline{CAS8}$ active time. In MB 85227, hidden refresh means $\overline{CAS}$-before-$\overline{RAS}$ refresh and the internal refresh address and used, that is no external refresh address is needed.

Notice for using MB 85227
The MB 85227 is a SIP (Single-In-Line-Package) module which is composed of nine MB 81256 DRAMs housed in plastic LCC, and assembled on the epoxy printed circuit board. Generally the multilayer PCB board has large wiring capacitance. This disadvantage causes relatively noise induction between signal lines and power supply lines (V_{SS} or V_{CC}).
Furthermore, as the MB 85227 is a very high-speed memory, the timing windows to strobe address $\overline{WE}$ and D_{IN} signals are very short (Approx. 5 ns). Therefore, it is very sensitive even to very sharp noise.
From the above reasons, special care should be taken for use the MB 85227. The following notices are recommended;

4

DESCRIPTION

1. Provide a externally capacitor of approx. a few μF each module, the MB 85227 has the nine decoupling capacitors (0.22 μF on each module 0.22 μF x 9).
2. Remove noise, riging, overshoot and undershoot from the address, clocks and DQ lines, so that the MB 85227 won't latch wrong signals due to the noise induction between signal lines and between signal and power supply lines.
3. Keep enough timing margin and remove critical timing in the board design, to avoid the problem mentioned in the above item 2.
4. Provide an appropriate dumping if necessary, to avoid excessive overshoot or undershoot on the TTL input waveforms.

Fig. 3 – MB 85227 DERATING CURVE (Normal Cycle)

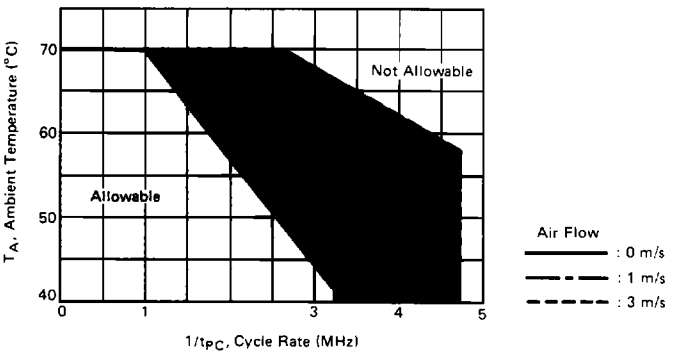
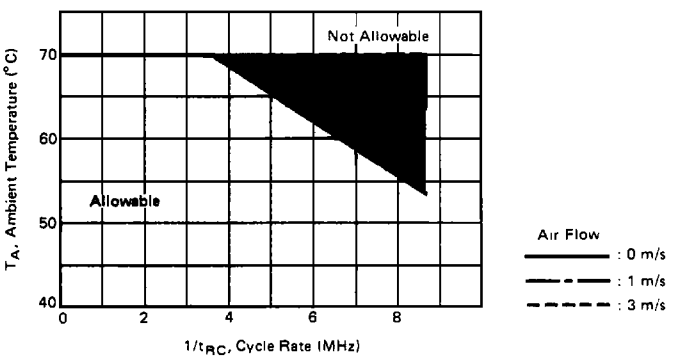
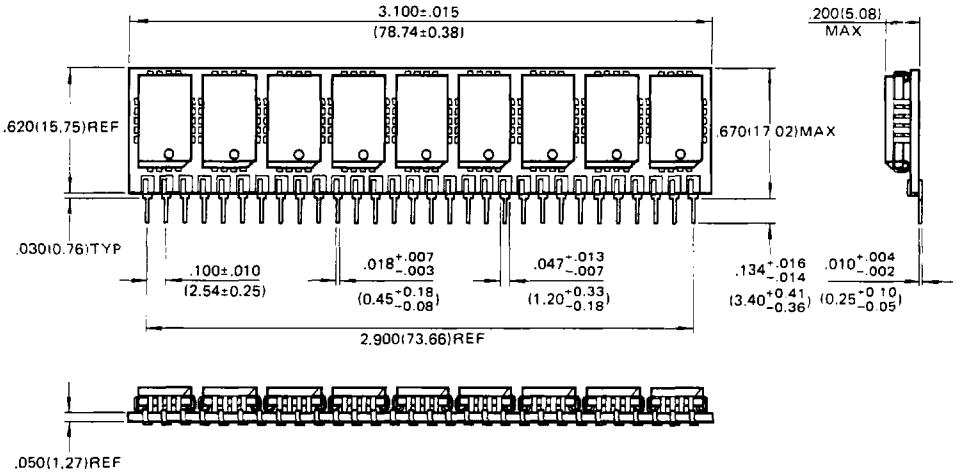


Fig. 4 – MB 85227 DERATING CURVE (Page Mode Cycle)



PACKAGE DIMENSIONS

30-LEAD SINGLE IN-LINE PACKAGE MODULE
(CASE No.: MSP-30P-P02)

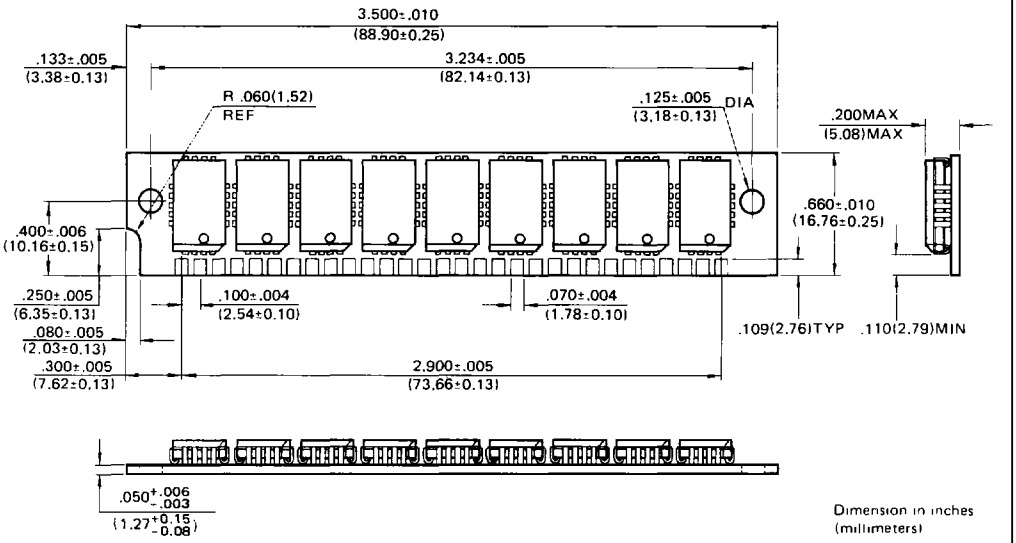


Dimensions in
inches (millimeters)

4

PACKAGE DIMENSIONS

30-PAD PLASTIC SINGLE IN-LINE PACKAGE MODULE
(CASE No.: MSS-30P-P01)



4