2x512Kx32bit DRAM Card

MF14M1-J57ATXX

Connector Type

Two-piece 88-pin

DESCRIPTION

These DRAM CARDs have been developed based on JEIDA DRAM CARD GUIDELINE Ver. 2. 1.
These cards are made using industry standard 512K × 8 Dynamic RAM and interface IC's in TSOP.

FEATURES

- Operating Voltage : V_{CC}=3. 3V ± 5 %
- All inputs except $\overline{RAS}$ inputs are buffered.
- Standard card size : 54mm (W) ×85. 6mm (L) ×3. 3mm (T)
- 88pin 2 piece connector type.
- $\overline{RAS}$ only refresh mode, $\overline{CAS}$ before $\overline{RAS}$ refresh mode and Page mode functions are available.
- Self refresh mode is available. (128ms/1024cycle)

APPLICATIONS

Main/expansion memory unit for Personal Conputer. Laser-Printer, FAX etc.

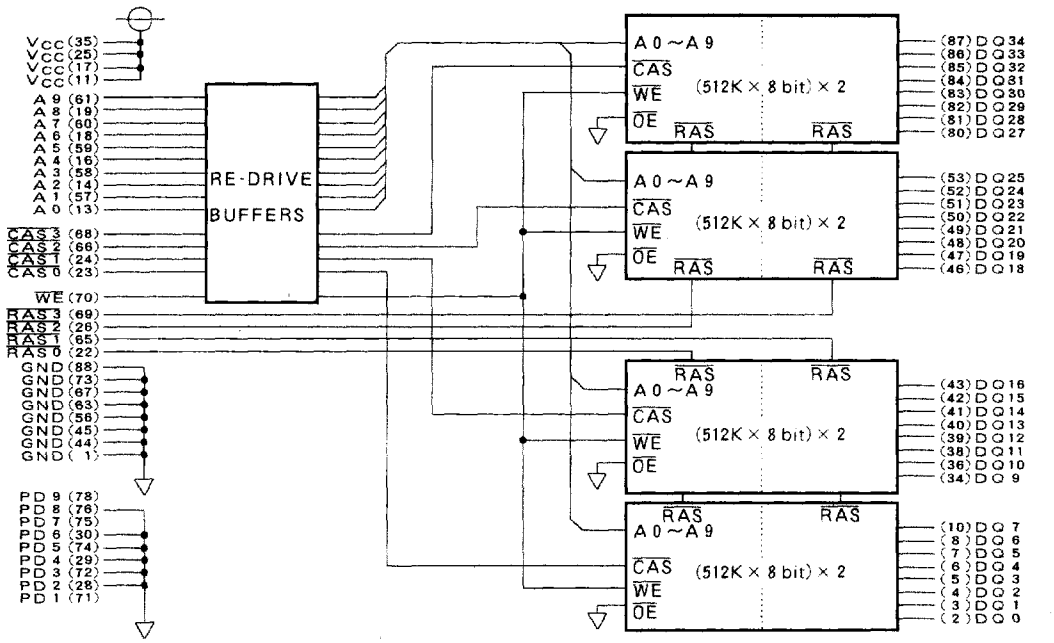
PRODUCT LIST

Item / Type name	Memory capacity	Data bus width (bits)	Access time (t_{RAC}) (ns)	Connector type	Number of pins	Outline drawing
MF14M1-J57ATXX	4 MB	32	70	Two-piece	88	88P-002

PIN ASSIGNMENT

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground	45	GND	Ground
2	DQ0	Data I/O	46	DQ18	Data I/O
3	DQ1		47	DQ19	
4	DQ2		48	DQ20	
5	DQ3		49	DQ21	
6	DQ4		50	DQ22	
7	DQ5		51	DQ23	
8	DQ6		52	DQ24	
9	N.C.	No connection	53	DQ25	
10	DQ7	Data I/O	54	N.C.	No connection
11	Vcc	Power supply voltage	55	N.C.	
12	N.C.	No connection	56	GND	Ground
13	A0	Address input	57	A1	Address input
14	A2		58	A3	
15	N.C.	No connection	59	A5	
16	A4	Address input	60	A7	
17	Vcc	Power supply voltage	61	A9	
18	A6	Address input	62	N.C.	No connection
19	A8		63	GND	Ground
20	N.C.	No connection	64	N.C.	No connection
21	N.C.		65	$\overline{RAS1}$	Row address strobe 1
22	$\overline{RAS0}$	Row address strobe 0	66	$\overline{CAS2}$	Column address strobe 2
23	$\overline{CAS0}$	Column address strobe 0	67	GND	Ground
24	$\overline{CAS1}$	Column address strobe 1	68	$\overline{CAS3}$	Column address strobe 3
25	Vcc	Power supply voltage	69	$\overline{RAS3}$	Row address strobe 3
26	$\overline{RAS2}$	Row address strobe 2	70	$\overline{WE}$	Write enable
27	N.C.	No connection	71	PD1 (N.C.)	Presence detect 1
28	PD2 (GND)	Presence detect 2	72	PD3 (GND)	Presence detect 3
29	PD4 (GND)	Presence detect 4	73	GND	Ground
30	PD6 (GND)	Presence detect 6	74	PD5 (GND)	Presence detect 5
31	N.C.	No connection	75	PD7 (N.C.)	Presence detect 7
32	N.C.		76	PD8 (GND)	Presence detect 8
33	N.C.		77	N.C.	No connection
34	DQ9	Data I/O	78	PD9 (N.C.)	Presence detect 9
35	Vcc	Power supply voltage	79	N.C.	
36	DQ10	Data I/O	80	DQ27	Data I/O
37	N.C.	No conneciton	81	DQ28	
38	DQ11	Data I/O	82	DQ29	
39	DQ12		83	DQ30	
40	DQ13		84	DQ31	
41	DQ14		85	DQ32	
42	DQ15		86	DQ33	
43	DQ16		87	DQ34	
44	GND	Ground	88	GND	Ground

BLOCK DIAGRAM



FUNCTION TABLE

Operation	input					input/output		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row address	Column address	input	output		
Read	ACT	ACT	NAC	APD	APD	OPN	VLD	YES	Page mode identical
Early write	ACT	ACT	ACT	APD	APD	VLD	OPN	YES	
$\overline{RAS}$-only refrash	ACT	NAC	DNC	APD	DNC	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	OPN	YES	
Self refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note 1 : ACT : active, NAC : nonactive, DNC : don't care, VLD : calid, APD : applied, OPN : open
Odd numbered $\overline{RAS}$ signals ($\overline{RAS1}$, $\overline{RAS3}$) and even numbered $\overline{RAS}$ signals ($\overline{RAS0}$, $\overline{RAS2}$) should not be active at the same time during Read and Early write cycles.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.5~4.6	V
V_I	Input voltage		−0.5~4.6	V
V_O	Output voltage		−0.5~4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	T_a=25℃	8	W
T_{opr}	Operating temperature		0~55	℃
T_{stg}	Storage temperature		−40~80	℃

RECOMMENDED OPERATING CONDITIONS (T_a= 0 ~55℃, unless otherwise noted) : (Note 2)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	3.135	3.3	3.465	V
GND	Supply voltage	0	0	0	V
V_{IL}	High input voltage	2.0		V_{CC}	V
V_{IH}	Low input voltage	0		0.8	V

Note 2 : With respect to GND

ELECTRICAL CHARACTERISTICS (T_a = 0～55℃, V_{CC} = 3.3V ± 5 %, GND = 0 V) : (Note 3)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	High-level output voltage	I_{OH} = −2mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage	I_{OL} = 2mA	0		0.4	V
I_{OZ}	Off-state output current	0V ≦ V_{OUT} ≦ V_{CC}	−20		20	μA
I_I	Input current	0V ≦ V_{IN} ≦ V_{CC} other input pins = 0V	−20		20	μA
I_{CC1}(AV)	Average supply current from V_{CC}, operating (Note 4, 5, 6)	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = t_{WC} = min, output open			330	mA
I_{CC2}(AV)	Supply current from V_{CC}, Standby (Note 7)	$\overline{RAS}$ = $\overline{CAS}$ ≧ V_{CC} − 0.2V other input pins ≧ V_{CC} − 0.2V or 0.2V output open			0.7	mA
I_{CC3}(AV)	Average supply current from V_{CC}, refrashing (Note 4, 6)	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} t_{RC} = min, output open			590	mA
I_{CC4}(AV)	Average supply current from V_{CC}, Page-mode (Note 4, 5, 6)	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{RC} = min, output open			370	mA
I_{CC6}(AV)	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refrash mode (Note 4, 6)	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC} = min, output open			540	mA
I_{CC8}(AV)	Average supply current from V_{CC}, Extended refresh mode (Note 7)	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{WE}$ ≧ V_{CC} − 0.2V , other input pins = V_{CC} − 0.2V or 0.2V, output open t_{RC} = 125 μs, t_{RAS} (min) ～1 μs			1	mA
I_{CC9}(AV)	Average supply current from V_{CC}, Self refresh mode (Note 7)	$\overline{RAS}$ = $\overline{CAS}$ ≦ 0.2V output open			1	mA

Note 3 : Current flowing into a CARD is positive, out is negative.

4 : I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV) and I_{CC6} (AV) are dependent on cycle rate. Specified values are obtained at the fastest cycle rate.

5 : I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the outputs open.

6 : Column Address can be changed once or less while $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.

SWITCHING CHARACTERISTICS (T_a = 0 ~ 55℃, V_{CC} = 3.3V ± 5 %, GND = 0 V) : (Note 7)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{CAC}	Access time from $\overline{CAS}$ (Note 8, 9)		27	ns
t_{RAC}	Access time from $\overline{RAS}$ (Note 8, 10)		70	ns
t_{AA}	Column address access time (Note 8, 11)		42	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (Note 12)	0	27	ns

Note 7 : An initial pause of 500 μsec is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged period of $\overline{RAS}$ inactivity before proper device operation is achieved.

8 : Measured with a load circuit equivalent to 100pF and V_{OH} = 2.4V (I_{OH} = −2mA), V_{OL} = 0.4V (I_{OL} = 2 mA).
The reference levels for measuring of output signals are 2.0V (V_{OH}) and 0.8V (V_{OL}).

9 : Assumes that $t_{RCD} \geqq t_{RCD}(max)$ and $t_{ASC} \geqq t_{ASC}(max)$.

10 : Assumes that $t_{RCD} \leqq t_{RCD}(max)$ and $t_{RAD} \leqq t_{RAD}(max)$.

11 : Assumes that $t_{RAD} \geqq t_{RAD}(max)$ and $t_{ASC} \leqq t_{ASC}(max)$.

12 : $t_{OFF}(max)$ define the time at which the output achieves the high impedance state ($|I_{OUT}| \leqq 20\,\mu A$) and are not reference to $V_{OH}(min)$ or $V_{OL}(max)$.

TIMING REQUIREMENTS (T_a = 0 ~ 55℃, V_{CC} = 3.3V ± 5 %, GND = 0 V) : (Note 13, 14)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{REF}	Refresh cycle time		128	ms
t_{RP}	$\overline{RAS}$ high pulse width	50		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (Note 15)	20	43	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low (Note 16)	17		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time.	0		ns
t_{CPN}	$\overline{CAS}$ high pulse width	10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low (Note 17)	17	28	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low	10		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low (Note 18)	5	10	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low	10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low	15		ns
t_T	Transition time (Note 19)	3	50	ns

Note 13 : The timing requirements are assumed t_T = 5 ns.

14 : $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals.

15 : $t_{RCD}(max)$ is specified as a reference point only. If $t_{RCD} \leqq t_{RCD}(max)$, access time is t_{RAC}. If $t_{RCD} \geqq t_{RCD}(max)$, access time is defined as t_{CAC} and t_{AA}.

16 : t_{CRP} requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.

17 : $t_{RAD}(max)$ is specified as a reference point only.
If $t_{RAD} \geqq t_{RAD}(max)$ and $t_{ASC} \leqq t_{ASC}(max)$, access time is controlled exclusively by t_{AA}.

18 : $t_{ASC}(max)$ is specified as a reference point only.

19 : t_T is measured between $V_{IH}(min)$ and $V_{IL}(max)$.

Read and Refresh Cycles

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{RC}	Read cycle time	130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	27		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	5		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	10		ns

Write Cycle (Early Write)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{WC}	Write cycle time	130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	27		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		ns
t_{DS}	Data setup time	10		ns
t_{DH}	Data hold time after $\overline{CAS}$ low	22		ns

Page Mode Cycle (Read, Early Write)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{PC}	Read, Write cycle time	55		ns
t_{CP}	$\overline{CAS}$ high pulse width	10		ns
t_{RAS}	$\overline{RAS}$ low pulse width (Note 20)	125	100000	ns

Note 20 : $t_{RAS}(min)$ is specified the following formula as two cycles of $\overline{CAS}$ input are executed.
$t_{RAS}(min) = t_{CSH}(min) + t_{PC}(min)$.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 21)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{CSR}	$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	20		ns
t_{CHR}	$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	15		ns

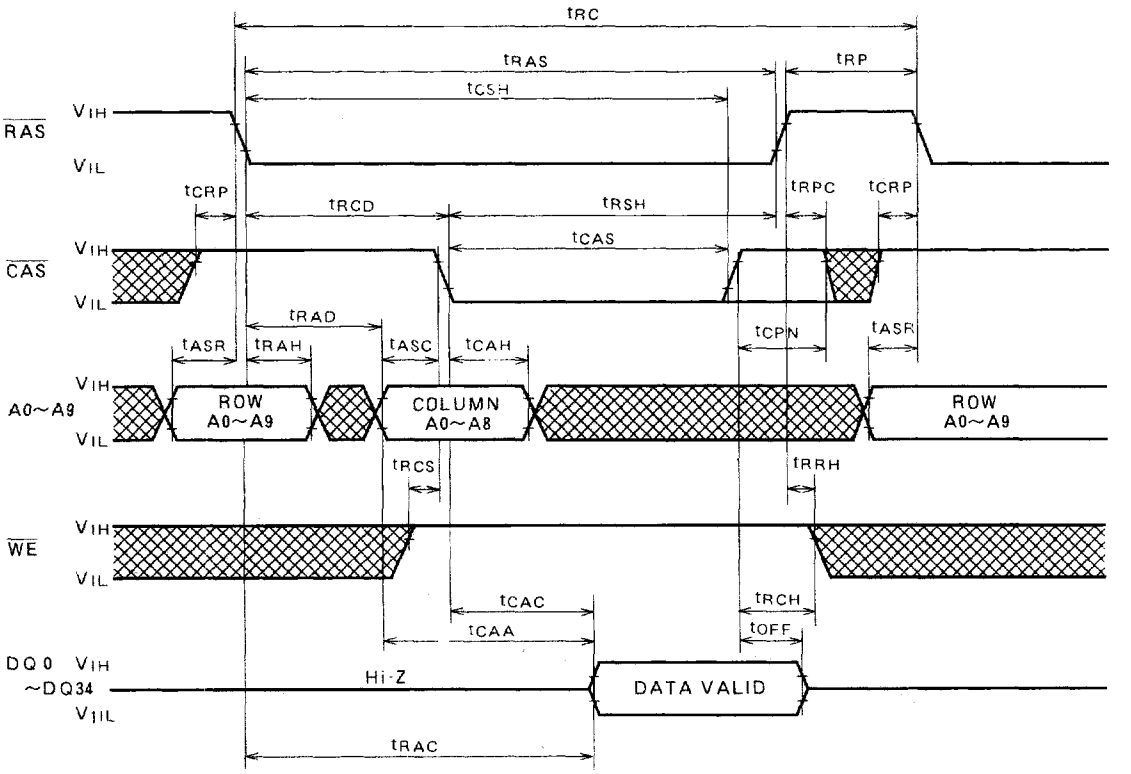
Note 21 : Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

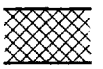
Self Refresh Cycle

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{RASS}	$\overline{RAS}$ low pulse width	100		μs
t_{RPS}	$\overline{RAS}$ high pulse width	130		ns
t_{CHS}	$\overline{CAS}$ hold time after $\overline{RAS}$ high	−50		ns

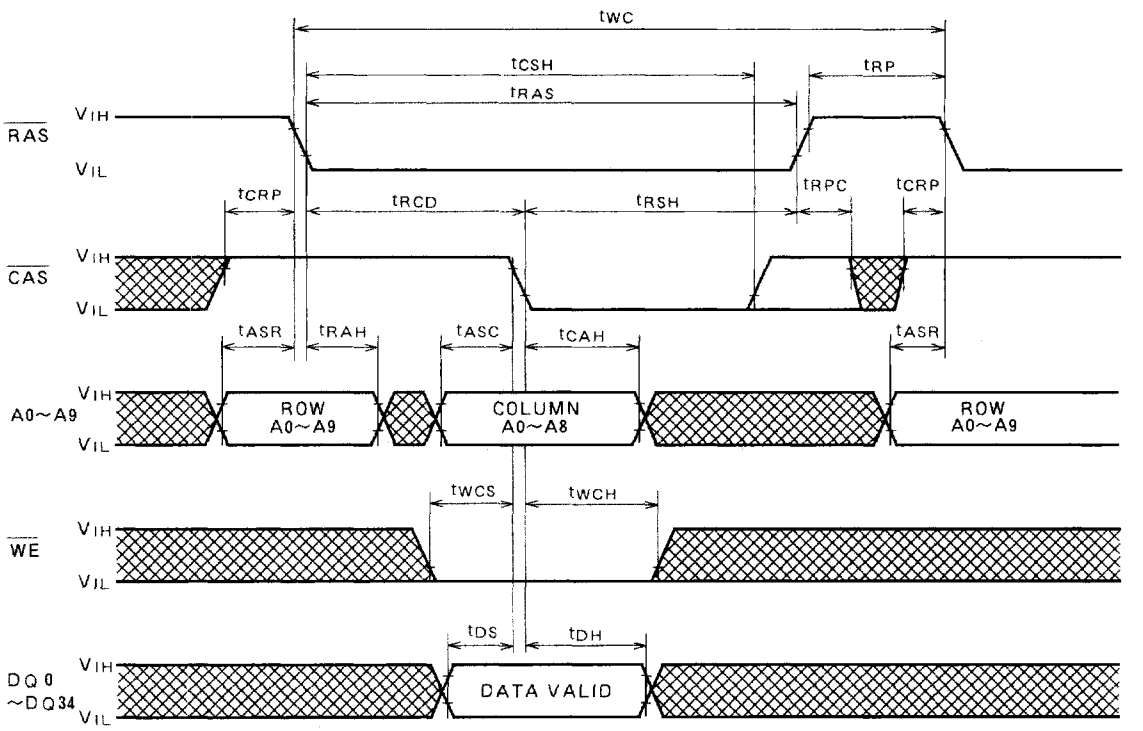
TIMING DIAGRAMS (Note 22)

Read Cycle

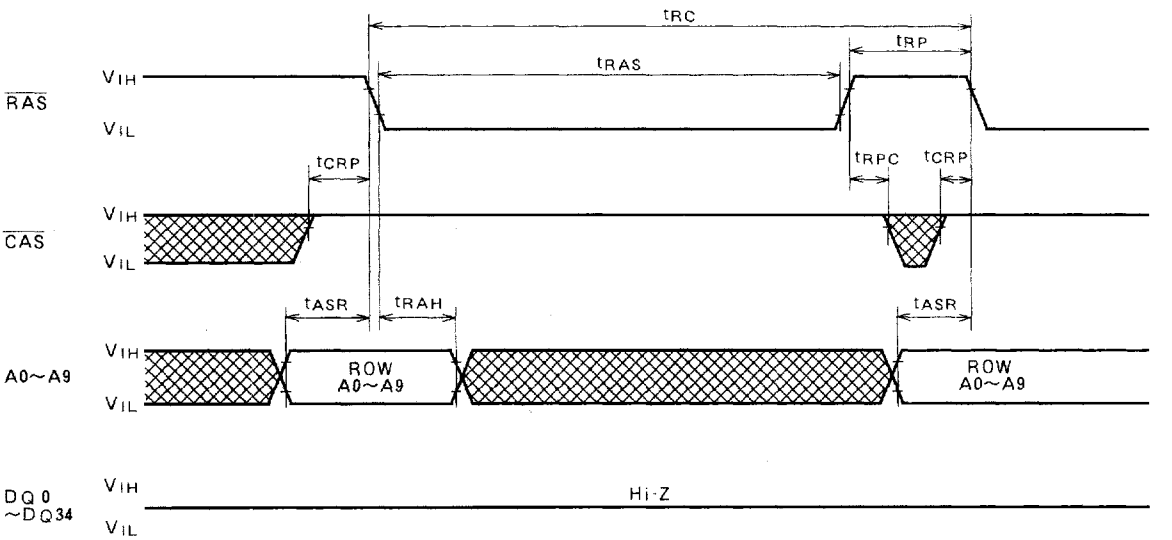


Note 22 :  indicates the don't care input

Early Write Cycle

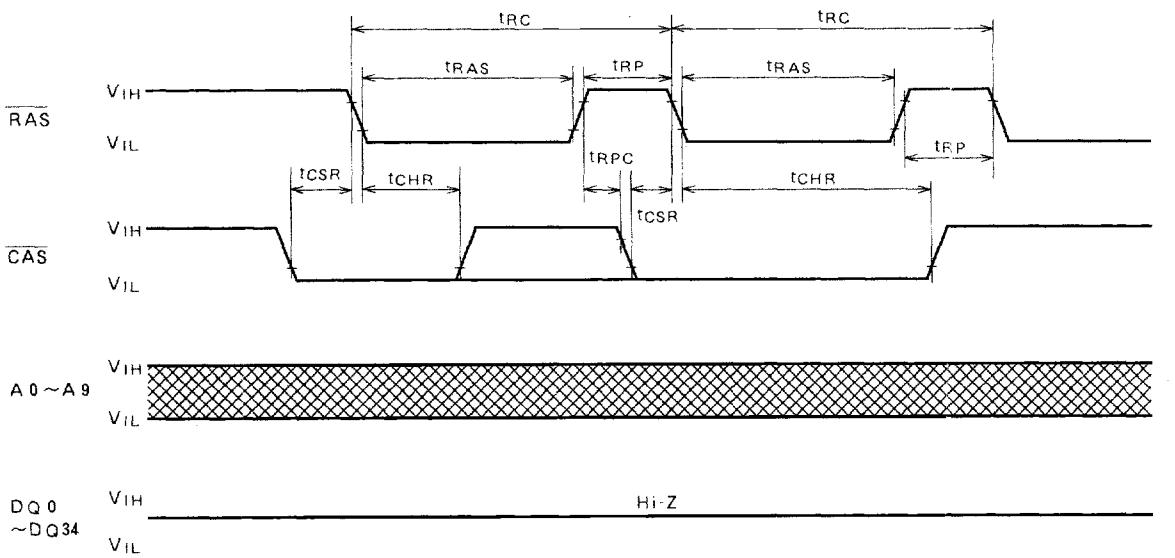


$\overline{RAS}$ only Refresh Cycle (Note 23)



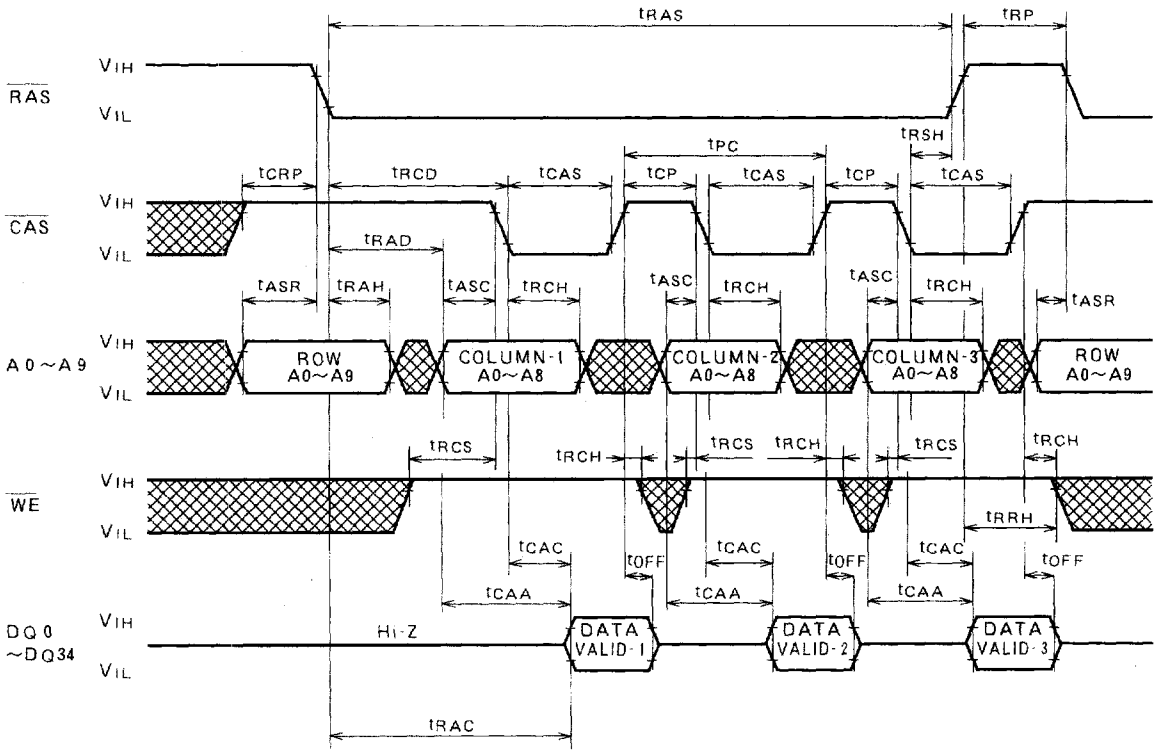
Note 23 : $\overline{WE}$ = don't care

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 24)

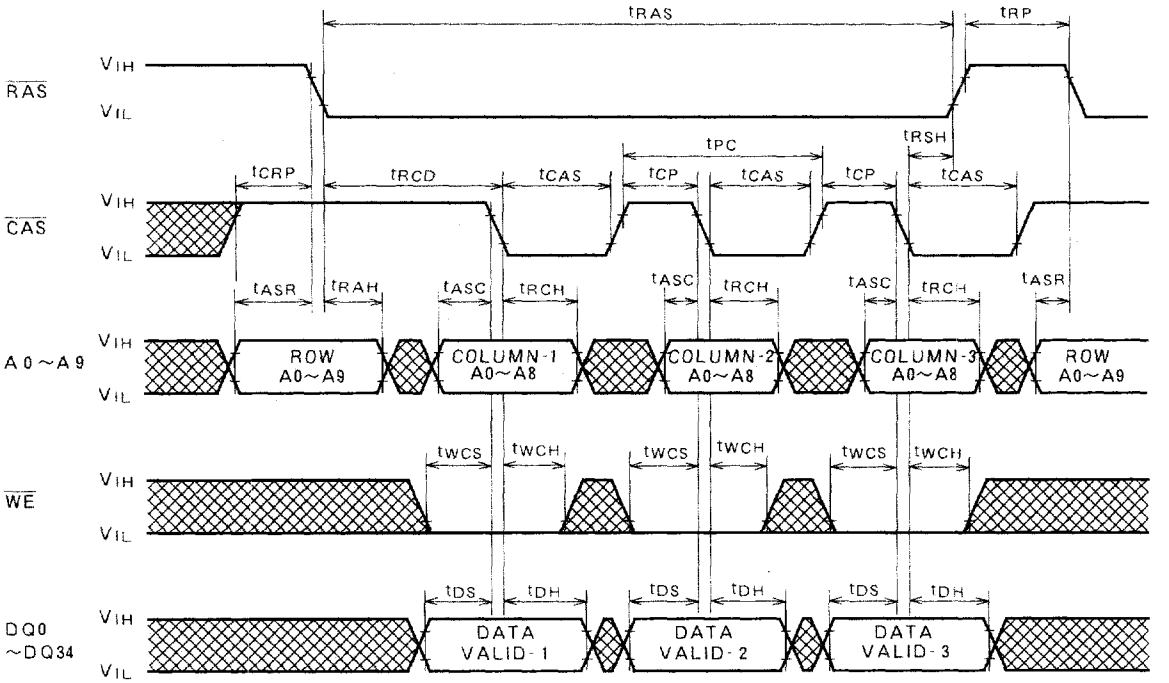


Note 24 : $\overline{WE} = V_{IH}$

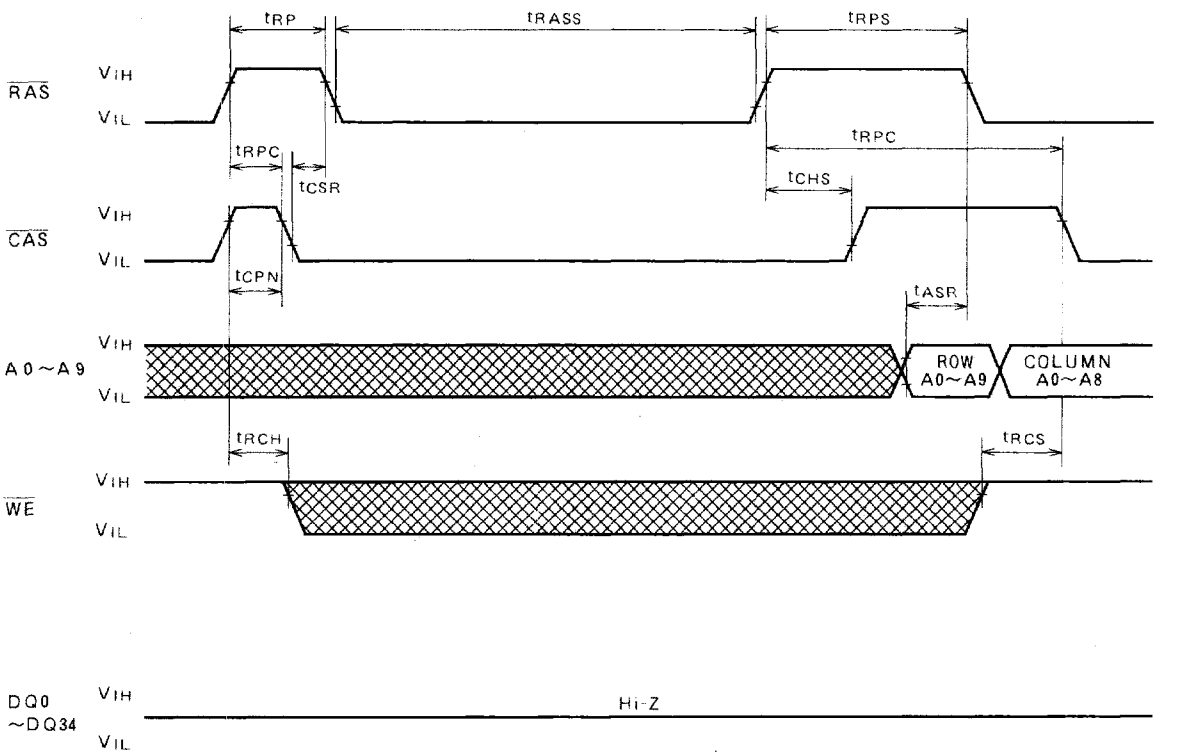
Page-Mode Read Cycle



Page-Mode Early Write Cycle



Self Refresh Cycle (Note 25)



Note 25. Self refresh sequence

Two refreshing methods can be selected depending on the low pulse width (t_{RASS}) of $\overline{RAS}$ signal during the self refresh period.

1. In case of $t_{RASS} < 300ms$

1.1 Distributed refresh during Read/Write operation

(A) Timing diagram

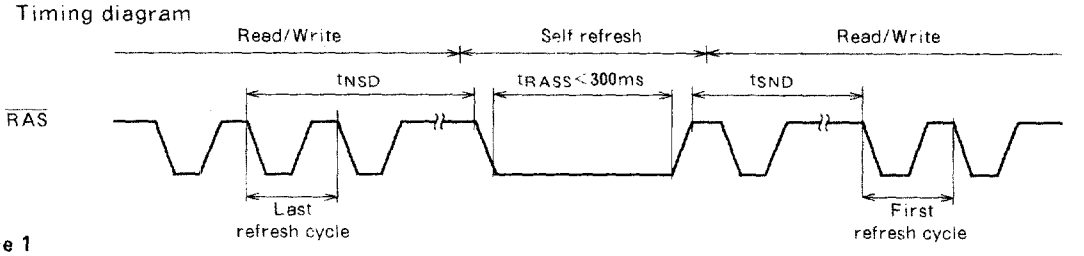
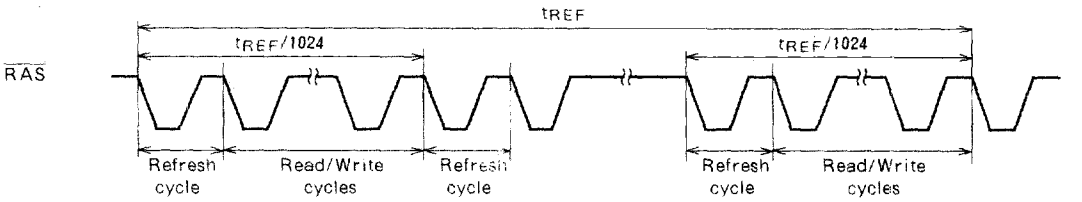


Table 1

Read/Write	Read/Write→ Self refresh	Self refresh→ Read/Write
CBR distributed refresh	$t_{NSD} + t_{SND} \leqq 16.4ms$	
$\overline{RAS}$ only distributed refresh	$t_{NSD} \leqq 16\,\mu s$	$t_{NSD} \leqq 16\,\mu s$

(B) Definition of distributed refresh



Definition of CBR distributed refresh

The CBR distributed refresh performs more than 1024 constant period (125 μs max) CBR cycles within 128ms.

Definition of $\overline{RAS}$ only distributed refresh

All combinations of ten row address signals ($A_0 \sim A_9$) are selected during 1024 constant period (16 μs max) $\overline{RAS}$ only refresh cycles within 16.4ms.

Note :

$\overline{RAS}/\overline{CAS}$ refresh may be used instead of $\overline{RAS}$ only refresh.

1.1.1 CBR distributed refresh

- Switching from read/write operation to self refresh opertion.
  The time interval from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSD} (shown in table 1).
- Switching from self refresh operation to read/write operation.
  The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 1).

1.1.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation.
  The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16 μs.
- Switching from self refresh operation to read/write operation.
  The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16 μs.

1.2 Burst refresh during Read/Write operation

(A) Timing diagram

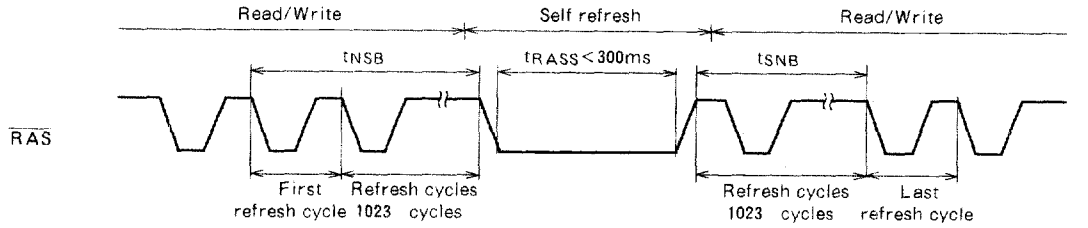
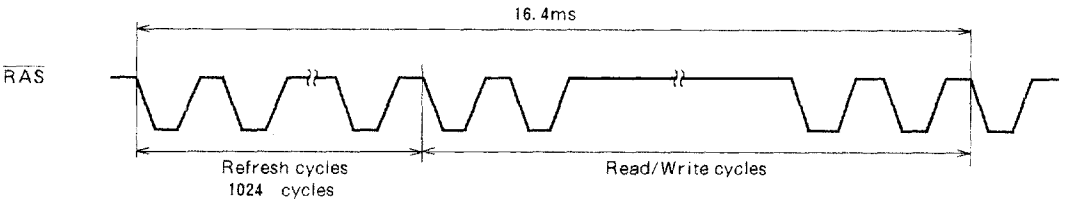


Table 2

Read/Write	Read/Write→ Self refresh	Self refresh→ Read/Write
CBR burst refresh	$t_{NSB} \leqq 16.4$ms	$t_{SNB} \leqq 16.4$ms
$\overline{RAS}$ only burst refresh	$t_{NSB} + t_{SNB} \leqq 16.4$ms	

(B) Definition of burst refresh



Definition of CBR burst refresh

The CBR burst refresh performs more than 1024 comtinuous CBR cycles within 16.4 ms.

Definition of $\overline{RAS}$ only burst refresh

All combinations of ten row address signals (A_0~A_9) are selected during 1024 continuous $\overline{RAS}$ only refresh cycles within 16.4ms.

1.2.1 CBR burst refresh

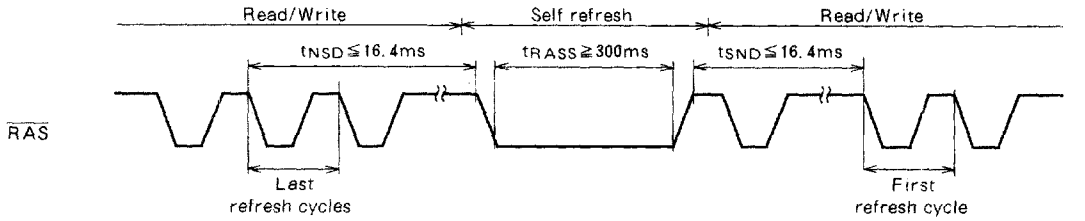
- Switching from read/write operation to self refresh operation.
  The time interval t_{NSB} from the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh opertion should be set within 16.4ms.
- Switching from self refresh operation to read/write operation.
  The time interval t_{SNB} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period should be set within 16.4ms.

1.2.2 $\overline{RAS}$ only burst refresh

- Switching from read/write operation to self refresh operation.
  The time interval from the falling edge of $\overline{RAS}$ signal in the first $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSB} (shown in table 2).
- Switching from self refresh operation to read/write operation.
  The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation th the falling edgs of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period should be set within t_{SNB} (shown in table 2).

2. In case of $t_{RASS} \geqq 300ms$

(A) Timing diagram-A



Timing diagram-B

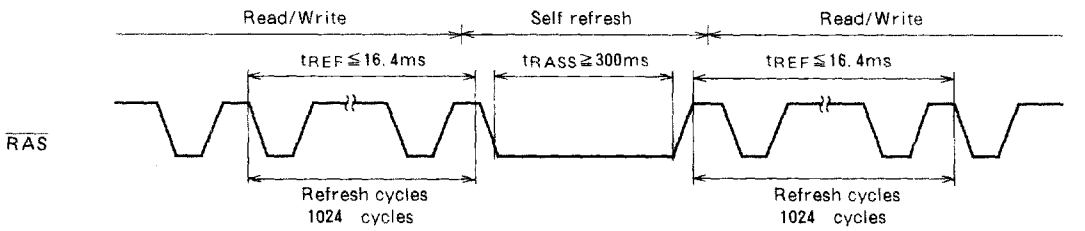


Table 3

Read/Write	Read/Write→Self refresh	Self refresh→Read/Write
CBR distributed refresh	Timing diagram-A	Timing diagram-A
$\overline{RAS}$ only distributed refresh CBR burst refresh $\overline{RAS}$ only burst refresh	Timing diagram-B	Timing diagram-B

(B) Definition of refresh

The same as 1.1−(B) and1.2−(B)

2.1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation.
  The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16.4ms.
- Switching from self refresh operation to read/write operation.
  The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16.4ms.

2.1.2 $\overline{RAS}$ only distributed, CBR burst, $\overline{RAS}$ only burst refresh.

- Before and after the self refresh. 1024 refresh cycles should be executed within 16.4ms for each refresh operation.