Integrated Device Technology, Inc.

2K x 36 CMOS DUAL-PORT STATIC RAM MODULE

IDT7M1012

FEATURES

- High density 2K x 36 CMOS Dual-Port Static RAM module
- Fast access times
  - — Commercial: 25, 30, 40, 50, 60ns
  - — Military: 30, 40, 50, 60, 70ns
- Fully asynchronous read/write operation from either port
- Surface mounted LCC packages allow through-hole module to fit on a 121-pin PGA footprint
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

DESCRIPTION

The IDT7M1012 is a 2K x 36 high speed CMOS Dual-Port static RAM module constructed on a co-fired ceramic substrate using four IDT7012 (2K x 9) Dual-Port RAMs. The IDT7M1012 modules are designed to be used as stand alone 36-bit dual-port RAM where on-chip hardware port arbitration is not needed. It is the users responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports.

This module provides two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory.

The IDT7M1012 module is packaged in a 121-pin ceramic PGA (Pin Grid Array), resulting in package dimensions of only 1.36" x 1.36" x 0.28". Maximum access times as fast as 25ns/30ns are available over the commercial/military temperature range.

All IDT military modules are constructed with semiconductor components manufactured in compliance with the latest revision of MIL-STD-883, Class B making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION[1]

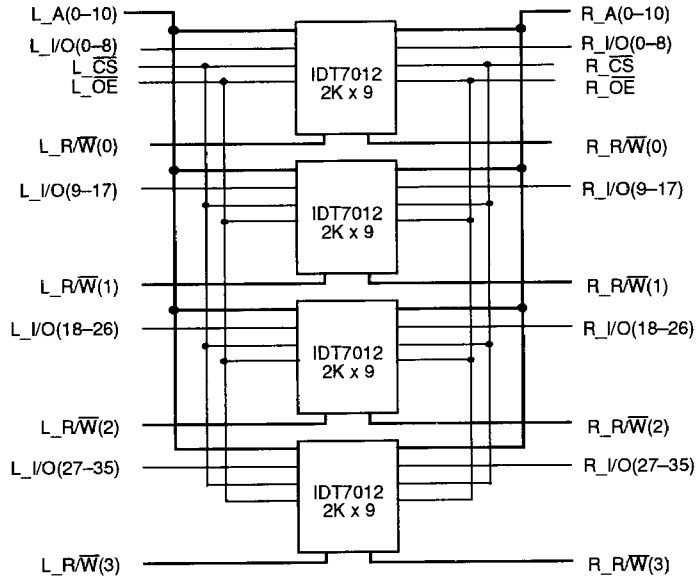
	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	GND	L_R/W(3)	R_R/W(3)	R_I/O(20)	R_I/O(22)	R_I/O(25)	L_I/O(27)	L_I/O(28)	L_I/O(30)	L_I/O(32)	L_R/$\overline{W}$(4)	R_R/$\overline{W}$(4)	R_I/O(35)	A
B	L_I/O(18)	R_I/O(18)	R_I/O(19)	R_I/O(21)	R_I/O(23)	R_I/O(24)	R_I/O(26)	L_I/O(29)	L_I/O(31)	L_I/O(33)	VCC	L_I/O(34)	R_I/O(34)	B
C	L_I/O(19)	L_I/O(23)	VCC	L_A(0)	L_A(9)	L_A(10)	GND	R_A(10)	R_A(9)	R_A(0)	GND	L_I/O(35)	R_I/O(33)	C
D	L_I/O(20)	L_I/O(24)	L_A(1)	GND							R_A(1)	R_I/O(27)	R_I/O(32)	D
E	L_I/O(21)	L_I/O(25)	L_A(2)								R_A(2)	R_I/O(28)	R_I/O(31)	E
F	L_I/O(22)	L_I/O(26)	L_A(3)								R_A(3)	R_I/O(29)	R_I/O(30)	F
G	GND	L_$\overline{CS}$	GND				PGA Top View				GND	R_$\overline{CS}$	GND	G
H	L_R/$\overline{W}$(1)	L_$\overline{OE}$	R_R/$\overline{W}$(1)								L_R/$\overline{W}$(2)	R_$\overline{OE}$	R_R/$\overline{W}$(2)	H
J	L_I/O(0)	R_I/O(3)	L_A(4)								R_A(4)	L_I/O(15)	R_I/O(17)	J
K	L_I/O(1)	R_I/O(2)	L_A(5)								R_A(5)	L_I/O(16)	R_I/O(16)	K
L	L_I/O(2)	R_I/O(1)	GND	L_A(6)	L_A(7)	L_A(8)	GND	R_A(8)	R_A(7)	R_A(6)	VCC	GND	R_I/O(15)	L
M	L_I/O(3)	R_I/O(0)	VCC	R_I/O(4)	R_I/O(5)	R_I/O(7)	R_I/O(8)	L_I/O(11)	L_I/O(12)	L_I/O(13)	L_I/O(14)	L_I/O(17)	R_I/O(14)	M
N	L_I/O(4)	L_I/O(5)	L_I/O(6)	L_I/O(7)	L_I/O(8)	R_I/O(6)	L_I/O(9)	L_I/O(10)	R_I/O(9)	R_I/O(10)	R_I/O(11)	R_I/O(12)	R_I/O(13)	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

NOTES:

2821 drw 01

1. For the IDT7M1011 (1K x 36 version), Pins C6 and C8 (L_A(10) and R_A(10) respectively) must be connected to VCC for proper operation of the module.

FUNCTIONAL BLOCK DIAGRAMS



2821 drw 02

PIN NAMES

Left Port	Right Port	Names
L_CS	R_CS	Chip Selects
L_R/W(1-4)	R_R/W(1-4)	Read/Write Enables
L_OE	R_OE	Output Enables
L_A (0–10)	R_A (0–10)	Address Inputs
L_I/O (0–35)	R_I/O (0–35)	Data Input/Outputs
Vcc		Power
GND		Ground

2821 tbl 01

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	–0.5(1)	—	0.8	V

2821 tbl 02

NOTE:
1. VIL = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2821 tbl 03

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

2821 tbl 04

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

7-6-1

CAPACITANCE TABLE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(1)	Input Capacitance (Address, $\overline{CS}$, $\overline{OE}$)	V_{IN} = 0V	50	pF
C_{IN}(2)	Input Capacitance (Data, R/$\overline{W}$)	V_{IN} = 0V	15	pF
C_{OUT}	Output Capacitance (Data)	V_{OUT} = 0V	15	pF

2821 tbl 05

NOTE:
1. This parameter is guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	40	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS} \geq V_{IH}$, V_{OUT} = GND to V_{CC}	—	40	µA
V_{OL}	Output Low Voltage	V_{CC} = Min. I_{OL} = 4mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min. I_{OH} = -4mA	2.4	—	V

2821 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.(1)	Max.(2)	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	V_{CC} = Max., $\overline{CS} \leq V_{IL}$, Outputs Open, f = f_{MAX}	—	1040	1240	mA
I_{SB}	Standby Supply Current (Both Ports Inactive)	V_{CC} = Max., $\overline{CS}$_L and $\overline{CS}$_R ≥ V_{IH} Outputs Open, f = f_{MAX}	—	260	320	mA
I_{SB1}	Standby Supply Current (One Port Inactive)	V_{CC} = Max., $\overline{CS}$_L o $\overline{CS} \geq V_{IH}$ Outputs Open, f = f_{MAX}	—	700	800	mA
I_{SB2}	Full Standby Supply Current (Both Ports Inactive)	$\overline{CS}$_L and $\overline{CS}$_R ≥ V_{CC} –0.2V $V_{IN} > V_{CC}$ 0.2V or < 0.2V	—	60	120	mA

2821 tbl 07

NOTES:
1. For commercial grade (0°C to +70°C) versions only.
2. For military grade (-55°C to +125°C) versions only.

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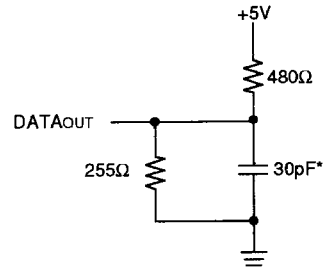
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2821 tbl 08



*Including scope and jig.

Figure 1. Output Load 2821 drw 03

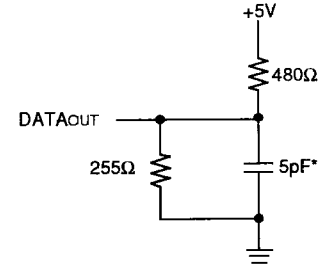


Figure 2. Output Load 2821 drw 04

(For tCHZ, tCLZ, tOHZ, tOLZ, tWHZ, tOW)

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

		7M1012SxxG, 7M1012SxxGB												
		-25[3]		-30		-40		-50		-60		-70		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle														
t_{RC}	Read Cycle Time	25	—	30	—	40	—	50	—	60	—	70	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	40	—	50	—	60	—	70	ns
t_{ACS}	Chip Select Access Time	—	25	—	30	—	40	—	50	—	60	—	70	ns
t_{OE}	Output Enable Access Time	—	12	—	15	—	25	—	30	—	35	—	40	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	10	—	12	—	15	—	20	—	30	—	35	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	10	—	12	—	15	—	20	—	30	—	35	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Down Time	—	50	—	50	—	50	—	50	—	50	—	50	ns
Write Cycle														
t_{WC}	Write Cycle Time	25	—	30	—	40	—	50	—	60	—	70	—	ns
t_{CW}	Chip Select to End of Write	20	—	25	—	30	—	35	—	40	—	50	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	35	—	40	—	50	—	ns
t_{AS}	Address Set-Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	30	—	35	—	40	—	50	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	12	—	15	—	20	—	20	—	20	—	30	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	10	—	12	—	15	—	20	—	30	—	35	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	10	—	12	—	15	—	20	—	30	—	35	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	0	—	ns

2821 tbl 09

NOTES:
1. This parameter is guaranteed by design but not tested.
2. Port-to-Port delay through the RAM cells from the writing port to the reading port.
3. Preliminary specification only.

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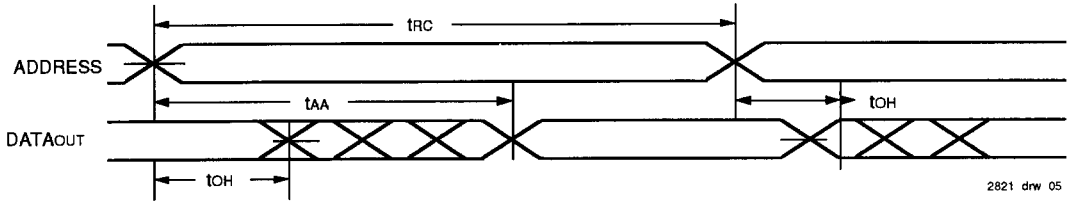
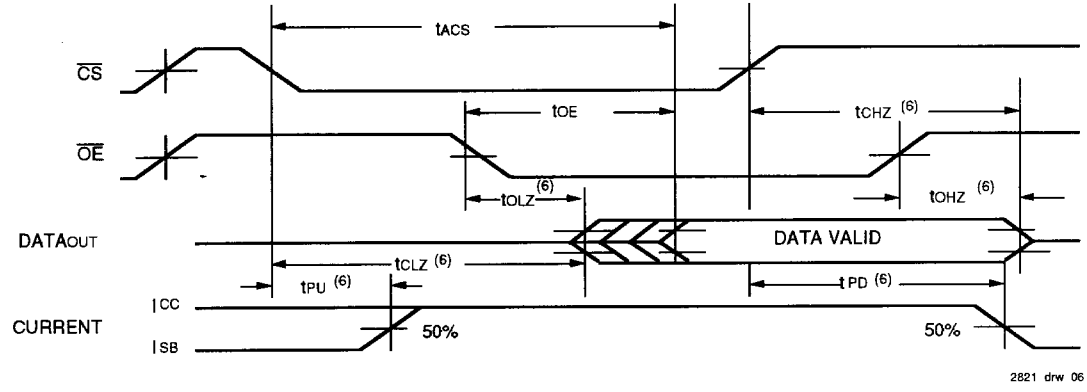
TIMING WAVEFORM OF READ CYCLE NO. 1 (EITHER SIDE) (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 2 (EITHER SIDE) (1, 3, 5)



NOTES:
1. R/$\overline{W}$ is high for Read Cycles
2. Device is continuously enabled, $\overline{CS} \leq V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low
4. $\overline{OE} \leq V_{IL}$
5. To access RAM, $\overline{CS}$ = L.
6. This parameter is guaranteed by design but not tested.

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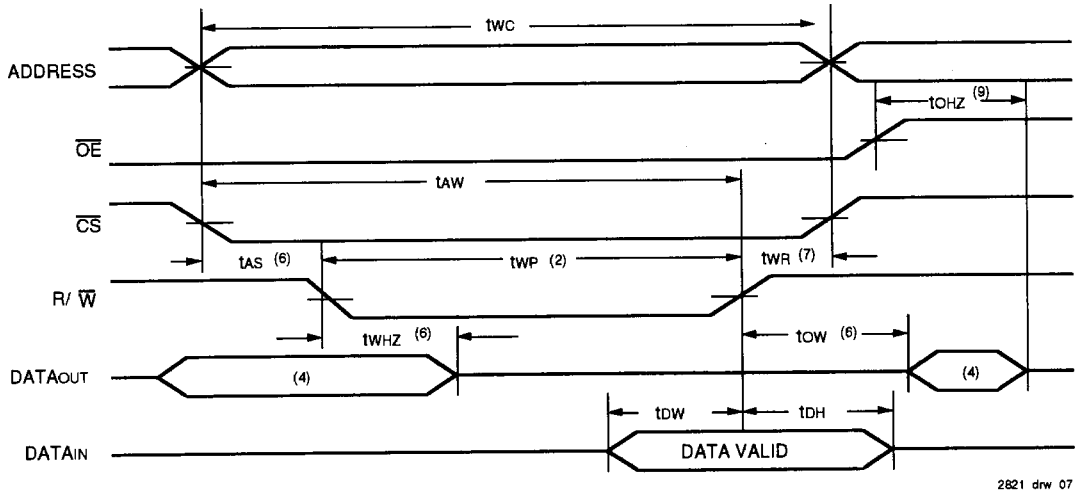
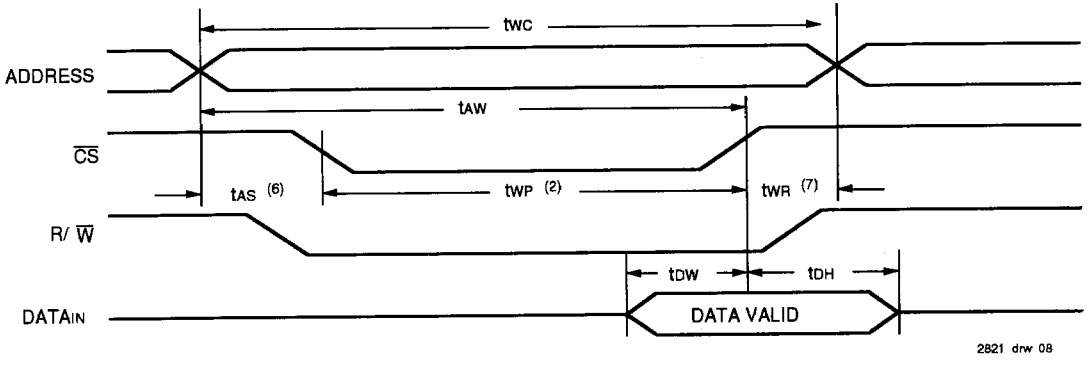
TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING) (1, 3, 5, 8)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING) (1, 3, 5, 8)



NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply. and the write pulse can be as short as the specified tWP.
9. This parameter is guaranteed by design but not tested.

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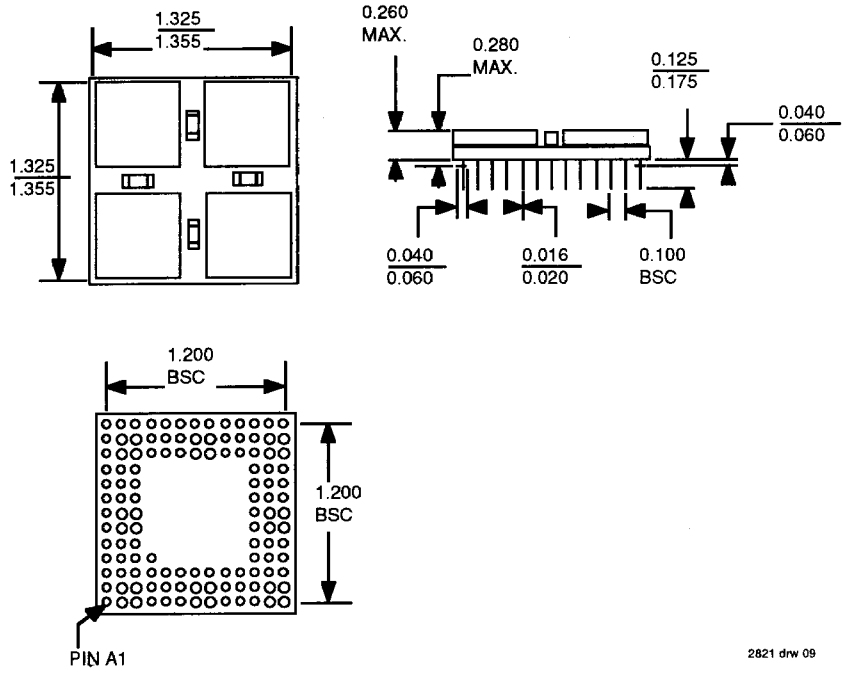
PACKAGE DIMENSIONS



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