2MB SGRAM MODULE

(256Kx64 SODIMM based on 256Kx32 SGRAM)

Unbuffered SGRAM
Graphics
64-bit Non-ECC/Parity
144-pin SODIMM

Revision 2.5

July 1998

Revision History

Revision 2.5 (July 1998)
- Added -7(143MHz) speed product.
- Changed SPD data, Byte #62 from 02h to 00h.

Revision 2.4 (June 1998)
- Added KMM965G256B product which does not support SPD.

Revision 2.3 (March 1998)
- Changed the Current values of ICC1, ICC3N, ICC4, ICC7 in *DC CHARACTERISTICS.*

Revision 2.2 (February 1998)
- Removed KMM966G256B-H/12 product(-H : 100MHz @ CL =2, -12 : 83MHz @ CL=3).
- Changed the Current values of ICC1, ICC4, ICC5, ICC6, ICC7 in *DC CHARACTERISTICS.*
- Changed tSAC from 6 to 6.5 @ 125MHz, tSS from 2 to 2.5 @ 125MHz in *AC PARAMETER*.
- Changed SPD data according to each changed AC Parameters.
- Delete a page including *FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE.*

Revision 2.1 (December 3, 1997)
- Modified an erratum pin name of Pin #65 from CS1 to $\overline{CS1}$, Pin #66 from CS0 to $\overline{CS0}$, Pin #94 from ADD to VDD in *PIN CONFIGURATIONS* - page 3.

Revision 2.0 (November 26, 1997)
- Initial Draft --- Final Spec. (comply with Intel 0.2 spec. which is basically compatible with Intel 0.1 spec. except the changed functionality of *Strapping Resistor* DQ31 from Memory Timing to CAS Latency - page 4.

KMM965G256BQ(P)N / KMM966G256BQ(P)N SGRAM SODIMM

256Kx64 SGRAM SODIMM based on 256Kx32, 1K Refresh, 3.3V Synchronous Graphic RAMs

GENERAL DESCRIPTION

The Samsung KMM965(6)G256BQ(P)N is a 256K bit x 64 Synchronous Graphic RAM high density memory module. The Samsung KMM965(6)G256BQ(P)N consists of two CMOS 256K x 32 bit Synchronous Graphic RAMs in 100pin QFP packages mounted on a 144pin glass-epoxy substrate. Five 0.1uF decoupling capacitors are mounted on the printed circuit board for each Synchronous GRAM.

The KMM965(6)G256BQ(P)N is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies and burst lengths allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part NO.	Max. Freq. (t_{CC})
KMM965(6)G256BQ(P)N-G7	143MHz (7ns) @CL=3
KMM965(6)G256BQ(P)N-G8	125MHz (8ns) @CL=3
KMM965(6)G256BQ(P)N-G0	100MHz (10ns) @CL=3

* KM965(6)G256BQN : based on PQFP Component
KM965(6)G256BPN : based on TQFP Component

- Burst Mode Operation
- BLOCK-WRITE and Write-per-bit capability
- Independent byte operation via DQM0 ~ 7
- Auto & Self Refresh Capability (1024 cycles / 16ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- MRS cycle with address key programs.
  CAS Latency (2, 3)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Optional Serial PD with EEPROM(KMM966G256B)
- Resistor Strapping Options for speed and CAS Latency
- PCB : Height(1000mil **)**, single sided components

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{SS}	2	V_{SS}	Voltage Key				95	DQ31	96	DQ30
3	DQ63	4	DQ62					97	DQ29	98	DQ28
5	DQ61	6	DQ60	51	RSVD	52	RSVD	99	DQ27	100	DQ26
7	DQ59	8	DQ58	53	RSVD	54	RSVD	101	DQ25	102	DQ24
9	DQ57	10	DQ56	55	V_{SS}	56	V_{SS}	103	V_{SS}	104	V_{SS}
11	V_{DD}	12	V_{DD}	57	DSF	58	RFU	105	DQ23	106	DQ22
13	DQ55	14	DQ54	59	RFU	60	RFU	107	DQ21	108	DQ20
15	DQ53	16	DQ52	61	RFU	62	**SBA	109	DQ19	110	DQ18
17	DQ51	18	DQ50	63	V_{DD}	64	V_{DD}	111	DQ17	112	DQ16
19	DQ49	20	DQ48	65	$\overline{CS1}$	66	$\overline{CS0}$	113	V_{DD}	114	V_{DD}
21	V_{SS}	22	V_{SS}	67	$\overline{RAS}$	68	$\overline{CAS}$	115	DQM3	116	DQM2
23	DQM7	24	DQM6	69	$\overline{WE}$	70	CKE	117	DQM1	118	DQM0
25	DQM5	26	DQM4	71	V_{SS}	72	V_{SS}	119	V_{SS}	120	V_{SS}
27	V_{DD}	28	V_{DD}	73	CLK1	74	CLK0	121	DQ15	122	DQ14
29	DQ47	30	DQ46	75	V_{DD}	76	V_{DD}	123	DQ13	124	DQ12
31	DQ45	32	DQ44	77	RSVD	78	RSVD	125	DQ11	126	DQ10
33	DQ43	34	DQ42	79	RSVD (A11)	80	RSVD (A10)	127	DQ9	128	DQ8
35	DQ41	36	DQ40					129	V_{DD}	130	V_{DD}
37	V_{SS}	38	V_{SS}	81	BA(A9)	82	A8/AP	131	DQ7	132	DQ6
39	DQ39	40	DQ38	83	A7	84	A6	133	DQ5	134	DQ4
41	DQ37	42	DQ36	85	V_{SS}	86	V_{SS}	135	DQ3	136	DQ2
43	DQ34	44	DQ34	87	A5	88	A4	137	DQ1	138	DQ0
45	DQ33	46	DQ32	89	A3	90	A2	139	V_{SS}	140	V_{SS}
47	V_{DD}	48	V_{DD}	91	A1	92	A0	141	**SDA	142	**SCL
49	RSVD	50	RSVD	93	V_{DD}	94	V_{DD}	143	V_{DD}	144	V_{DD}

PIN NAMES

Pin Name	Function
A0 ~ A8	Address Input(multiplexed)
BA(A9)	Bank Select Address
DQ0 ~ 63	Data Input / Output
CLK0, *CLK1	Clock Input
CKE	Clock Enable Input
$\overline{CS0}$, *$\overline{CS1}$	Chip Select Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DSF	Define Special Function
DQM0 ~ 7	DQM
V_{DD}	Power Supply (3.3V)
V_{SS}	Ground
**SDA	Serial Address Data I/O
**SBA	EEPROM Device Address
**SCL	Serial Clock
RSVD	Reserved
RFU	Reserved for future use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one clock + t_{SS} prior to new command. Disable input buffers for power down in standby.
A0 ~ A8	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA8, column address : CA0 ~ CA7
BA(A9)	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
DSF	*Define Special Function*	Enables write per bit, block write and special mode register set.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

RESISTOR STRAPPING OPTIONS

Three resistor straps are used to indicate the synchronous clock frequency (period) and memory timing.Timing information for each clock frequency is indicated in the section titled *AC CHARATERISTICS*.

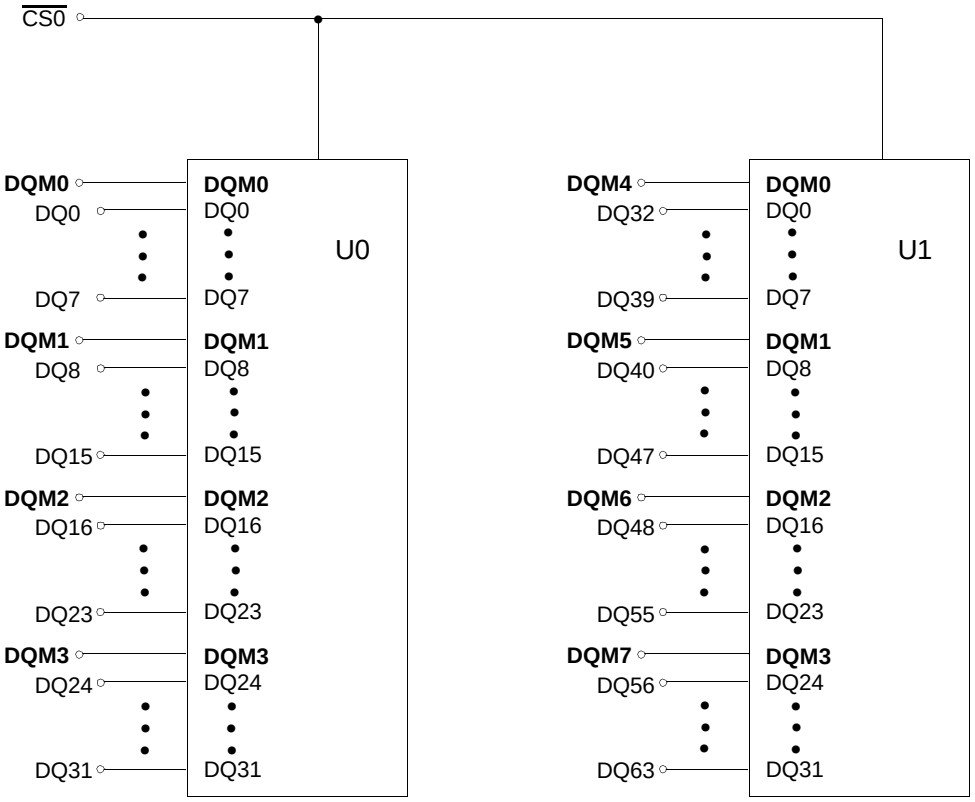
Clock Frequency and Memory Timing

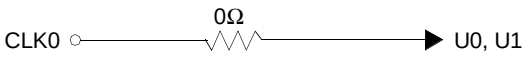
Cycle Time	DQ30	DQ29
10 ns	1	0
8ns	1	1
7ns	0	0

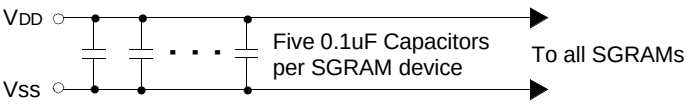
CAS Latency

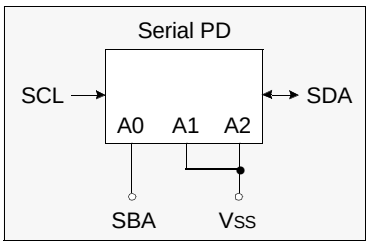
CAS Latency	DQ31
3	0
2 and 3	1

FUNCTIONAL BLOCK DIAGRAM









* Serial PD is optional

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS})

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	2	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	
Input low voltage	V_{IL}	-0.3	0	0.8	V	Note 1
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-10	-	10	uA	Note 2
Output leakage current	I_{OL}	-5	-	5	uA	Note 3
Output loading conditon	See Figure 1					

Note : 1. V_{IL}(min.) = -1.5V AC (pulse width ≤ 5ns)
2. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V.
3. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (V_{CC} = 3.3V, T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A9, BA)	C_{IN1}	-	18	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, DSF)	C_{IN2}	-	18	pF
Input capacitance (CLK0)	C_{IN3}	-	18	pF
Input capacitance ($\overline{CS}$0)	C_{IN4}	-	18	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN5}	-	14	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	15	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C $V_{IH(min)}/V_{IL(max)}$ =2.0V/0.8V)

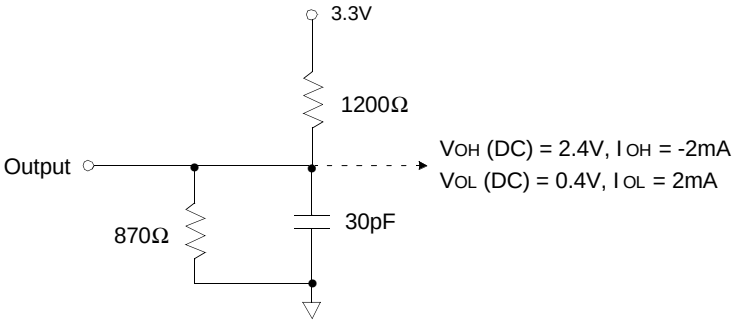
Parameter	Symbol	Test Condition	CAS Latency	Speed			Unit	Note
				-7	-8	-10		
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min), $t_{CC} \geq t_{CC}$(min), I_{OL} = 0 mA		360	320	300	mA	1
Precharge Standby Current in power-down mode	$I_{CC2}P$	CKE ≤ V_{IL}(max), t_{CC} = 15ns		4			mA	
	$I_{CC2}PS$	CKE ≤ V_{IL}(max), CLK ≤ V_{IL}(max), t_{CC} = ∞		4				
Precharge Standby Current in non power-down mode	$I_{CC2}N$	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		70			mA	
	$I_{CC2}NS$	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		30				
Active Standby Current in power-down mode	$I_{CC3}P$	CKE ≤ V_{IL}(max), t_{CC} = 15ns		6			mA	
	$I_{CC3}PS$	CKE ≤ V_{IL}(max), CLK ≤ V_{IL}(max), t_{CC} = ∞		6				
Active Standby Current in non power-down mode (One Bank Active)	$I_{CC3}N$	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		100			mA	
	$I_{CC3}NS$	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		50				
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA, Page Burst All bank Activated, t_{CCD} = t_{CCD}(min)	3	600	560	420	mA	1
			2	360	360	320		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		180	180	180	mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		4			mA	
Operating Current (One Bank Block Write)	I_{CC7}	$t_{CC} \geq t_{CC}$(min), I_{OL}=0mA, t_{BWC}(min)		420	380	300	mA	

Note : 1. Measured with outputs open. Address are changed only one time during tcc(min).

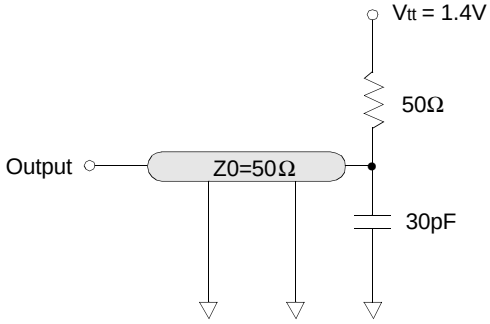
2. Refresh period is 16ms. Address are changed only one time during tcc(min).

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70°C)

Parameter	Value
AC input levels	V_{ih}/V_{il} = 2.4V / 0.4V
Input timing measurement reference level	1.4V
Input rise and fall time(See note 3)	t_R/t_F=1ns/ 1ns
Output timing measurement reference level	1.4V
Output load condition	See Fig. 2



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-7		-8		-10		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS Latency=3	t_{CC}	7	1000	8	1000	10	1000	ns	1
	CAS Latency=2		12		12		13			
CLK to valid output delay	CAS Latency=3	t_{SAC}	-	6	-	6.5	-	7	ns	1, 2
	CAS Latency=2		-	8	-	8	-	9		
Output data hold time		t_{OH}	2.5		2.5		2.5		ns	2
CLK high pulse width		t_{CH}	2.5		3		3.5		ns	3
CLK low pulse width		t_{CL}	2.5		3		3.5		ns	3
Input setup time		t_{SS}	2		2.5		2.5		ns	3
Input hold time		t_{SH}	1		1		1		ns	3
CLK to output in Low-Z		t_{SLZ}	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}	-	6	-	6.5	-	7	ns	
	CAS latency=2		-	8	-	8	-	9		

* All AC parameters are measured from half to half.

Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-7	-8	-10		
Row active to row active delay		$t_{RRD(min)}$	14	16	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	16	16	20	ns	1
Row precharge time		$t_{RP(min)}$	21	20	20	ns	1
Row active time		$t_{RAS(min)}$	49	48	50	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time		$t_{RC(min)}$	70	70	70	ns	1
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Block write data-in to PRE command delay		$t_{BPL(min)}$	1			CLK	
Block write cycle time		$t_{BWC(min)}$	1			CLK	1, 3
Number of valid output data	CAS latency=3		2			CLK	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.

2. Minimum delay is required to complete write.

3. This parameter means minimum $\overline{CAS}$ to $\overline{CAS}$ delay at block write cycle only.

4. In case of row precharge interrupt, auto precharge and read burst stop.

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	DQM	A_9	A_8	A_7~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	L	X	OP CODE			1, 2
	Special Mode Register Set								H					1,2,7
Refresh	Auto Refresh		H	H	L	L	L	H	L	X	X			3
	Self Refresh	Entry		L										3
		Exit	L	H	L	H	H	H	X	X	X			3
					H	X	X	X						3
Bank Active & Row Addr.	Write Per Bit Disable		H	X	L	L	H	H	L	X	V	Row Address		4, 5
	Write Per Bit Enable								H					4,5,9
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	L	X	V	L	Column Address	4
	Auto Precharge Enable											H		4, 6
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	L	X	V	L	Column Address	4, 5
	Auto Precharge Enable											H		4,5,6,9
Block Write & Column Addr.	Auto Precharge Disable		H	X	L	H	L	L	H	X	V	L	Column Address	4, 5
	Auto Precharge Enable											H		4,5,6,9
Burst Stop			H	X	L	H	H	L	L	X	X			7
Precharge	Bank Selection		H	X	L	L	H	L	L	X	V	L	X	
	Both Banks										X	H		
Clock Suspend or Active Power Down		Entry	H	L	L	H	H	H	X	X	X			
					H	X	X	X						
		Exit	L	H	X	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	L	H	H	H	X	X	X			
					H	X	X	X						
		Exit	L	H	L	V	V	V	V	X				
					H	X	X	X	X					
DQM			H	X						V	X			8
No Operation Command			H	X	L	H	H	H	X	X	X			
					H	X	X	X						

(V=Valid, X=Don ′t Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_9 : Program keys. (@MRS)
A_5, A_6 : LMR or LCR select. (@SMRS)
Color register exists only one per DQi which both banks share.
So dose Mask Register.
Color or mask is loaded into chip through DQ pin.
2. MRS can be issued only at both banks precharge state.
SMRS can be issued only if DQ ′s are idle.
A new command can be issued at the next clock of MRS/SMRS.

SIMPLIFIED TRUTH TABLE

3. Auto refresh functions as same as CBR refresh of DRAM.
   The automatical precharge without Row precharge command is meant by "Auto".
   Auto/Self refresh can be issued only at both precharge state.
4. A_9 : Bank select address.
   If "Low" at read, (block) write, Row active and precharge, bank A is selected.
   If "High" at read, (block) write, Row active and precharge, bank B is selected.
   If A_8 is "High" at Row precharge, A_9 is ignored and both banks are selected.
5. It is determined at Row active cycle.
   whether Normal/Block write operates in write per bit mode or not.
   For A bank write, at A bank Row active, for B bank write, at B bank Row active.
   Terminology : Write per bit =I/O mask
   (Block) Write with write per bit mode=Masked(Block) Write
6. During burst read or write with auto precharge, new read/(block) write command cannot be issued.
   Another bank read/(block) write command can be issued at t_{RP} after the end of burst.
7. Burst stop command is valid only at full page burst length.
8. DQM sampled at positive going edge of a CLK.
   masks the data-in at the very CLK(Write DQM latency is 0)
   but makes Hi-Z state the data-out of 2 CLK cycles after.(Read DQM latency is 2)
9. Graphic features added to SDRAM ′s original features.
   If DSF is tied to low, graphic functions are disabled and chip operates as a 8M SDRAM with 32 DQ ′s.

SGRAM vs SDRAM

Function	MRS		Bank Active		Write	
DSF	L	H	L	H	L	H
SGRAM Function	MRS	SMRS	Bank Active with Write per bit Disable	Bank Active with Write per bit Enable	Normal Write	Block Write

If DSF is low, SGRAM functionality is identical to SDRAM functionality

SGRAM can be used as an unified memory by the appropriate DSF control
--> SGRAM=Graphic Memory + Main Memory

MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with MRS

Address	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Function	W.B.L	TM		CAS Latency			BT	Burst Length		

(Note 1)

Test Mode			CAS Latency				Burst Type		Burst Length				
A_8	A_7	Type	A_6	A_5	A_4	Latency	A_3	Type	A_2	A_1	A_0	BT=0	BT=1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential	0	0	0	1	Reserved
0	1	Vendor Use Only	0	0	1	-	1	Interleave	0	0	1	2	Reserved
1	0		0	1	0	2			0	1	0	4	4
1	1		0	1	1	3			0	1	1	8	8
Write Burst Length			1	0	0	Reserved			1	0	0	Reserved	Reserved
A_9	Length		1	0	1	Reserved			1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved			1	1	0	Reserved	Reserved
1	Single Bit		1	1	1	Reserved			1	1	1	256(Full)	Reserved

(Note 2)

Special Mode Register Programmed with SMRS

Address	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Function	X			LC	LM	X				

Load Color		Load Mask	
A_6	Function	A_5	Function
0	Disable	0	Disable
1	Enable	1	Enable

(Note 3)

POWER UP SEQUENCE

1. Apply power and start clock, Attempt to maintain CKE= "H", DQM= "H" and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

cf.) Sequence of 4 & 5 may be changed.

The device is now ready for normal operation.

Note : 1. If A_9 is high during MRS cycle, "Burst Read Single Bit Write" function will be enabled.
2. The full column burst(256bit) is available only at Sequential mode of burst type.
3. If LC and LM both high(1), data of mask and color register will be unknown.

BURST SEQUENCE (BURST LENGTH = 4)

Initial address		Sequential				Interleave			
A_1	A_0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

BURST SEQUENCE (BURST LENGTH = 8)

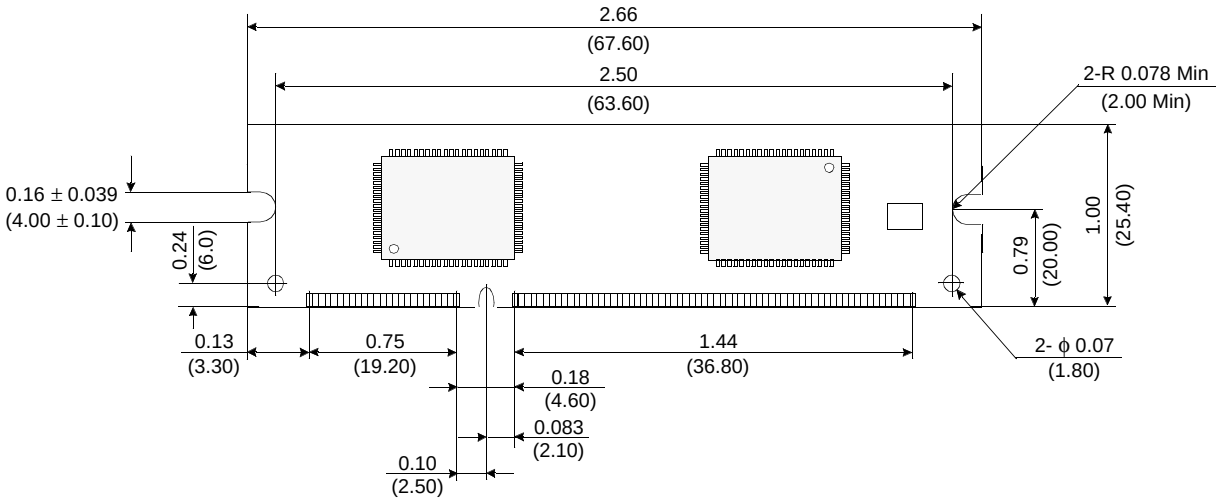
Initial address			Sequential								Interleave							
A_2	A_1	A_0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

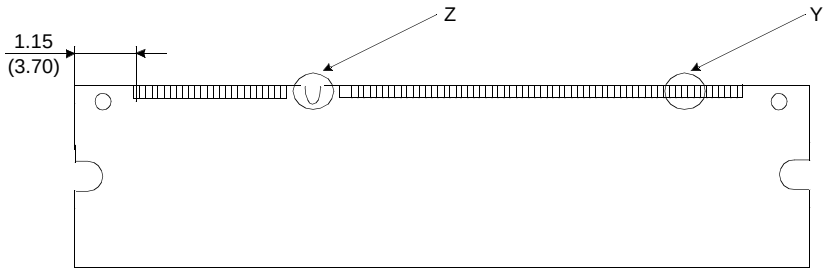
PIXEL to DQ MAPPING(at BLOCK WRITE)

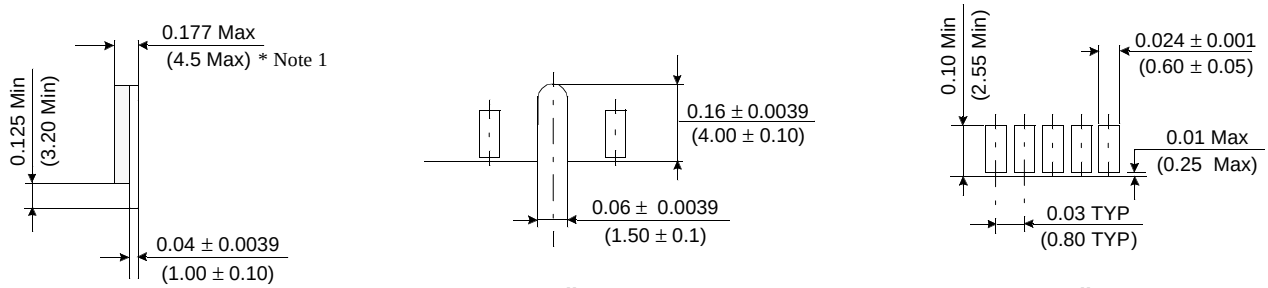
Column address			7 Byte	6 Byte	5 Byte	4 Byte	3 Byte	2 Byte	1 Byte	0 Byte
A_2	A_1	A_0	I/O_{63} - I/O_{56}	I/O_{55} - I/O_{48}	I/O_{47} - I/O_{40}	I/O_{39} - I/O_{32}	I/O_{31} - I/O_{24}	I/O_{23} - I/O_{16}	I/O_{15} - I/O_8	I/O_7 - I/O_0
0	0	0	DQ_{56}	DQ_{48}	DQ_{40}	DQ_{32}	DQ_{24}	DQ_{16}	DQ_8	DQ_0
0	0	1	DQ_{57}	DQ_{49}	DQ_{41}	DQ_{33}	DQ_{25}	DQ_{17}	DQ_9	DQ_1
0	1	0	DQ_{58}	DQ_{50}	DQ_{42}	DQ_{34}	DQ_{26}	DQ_{18}	DQ_{10}	DQ_2
0	1	1	DQ_{59}	DQ_{51}	DQ_{43}	DQ_{35}	DQ_{27}	DQ_{19}	DQ_{11}	DQ_3
1	0	0	DQ_{60}	DQ_{52}	DQ_{44}	DQ_{36}	DQ_{28}	DQ_{20}	DQ_{12}	DQ_4
1	0	1	DQ_{61}	DQ_{53}	DQ_{45}	DQ_{37}	DQ_{29}	DQ_{21}	DQ_{13}	DQ_5
1	1	0	DQ_{62}	DQ_{54}	DQ_{46}	DQ_{38}	DQ_{30}	DQ_{22}	DQ_{14}	DQ_6
1	1	1	DQ_{63}	DQ_{55}	DQ_{47}	DQ_{39}	DQ_{31}	DQ_{23}	DQ_{15}	DQ_7

PACKAGE DIMENSIONS - *Proposal (Based on JEDEC STD.)*

Units : Inches (millimeters)







Detail Z **Detail Y**

Tolerances : ±.0059(.15) unless otherwise specified

* Note 1 : This thickness is when using PQFP package. When using TQFP package, this value is 2.5mmMax.

The used device is 256Kx32, 8M SGRAM, 100pin (T)QFP
SGRAM Component Part No. : KM4132G271BQ : PQFP (Height = 3.0mmMax)
KM4132G271BTQ : TQFP (Height = 1.2mmMax)

SERIAL PRESENCE DETECT INFORMATION

- Serial PD Interface Protocol : I^2C
- Current sink capability of SDA driver $\leq$ 3mA
- Maximum clock frequency : 80KHz

Contents ;

Byte #	Function Described	Function Supported			Hex value			Note
		-7	-8	-10	-7	-8	-10	
0	# of bytes written into serial memory at module manufacturer	128byte			80h			
1	Total # of bytes of SPD memory device	256bytes (2K bit)			08h			
2	Fundamental memory type	SGRAM			06h			TBD
3	# of row address on this assembly	9			09h			1
4	# of column address on this assembly	8			08h			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SGRAM cycle time from clock @CAS latency of 3	7ns	8ns	10ns	70h	80h	A0h	2
10	SGRAM access time from clock @CAS latency of 3	6ns	6.5ns	7ns	60h	65h	70h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SGRAM width	x32			20h			
14	Error checking SGRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SGRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SGRAM device attributes : # of banks on SGRAM device	2 banks			02h			
18	SGRAM device attributes : CAS latency	2 & 3			06h			
19	SGRAM device attributes : CS latency	0 CLK			01h			
20	SGRAM device attributes : Write latency	0 CLK			01h			
21	SGRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SGRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			4Eh			
23	SGRAM cycle time @CAS latency of 2	12ns	12ns	13ns	C0h	C0h	D0h	2
24	SGRAM access time @CAS latency of 2	8ns	8ns	9ns	80h	80h	90h	2
25	SGRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	2
26	SGRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	2
27	Minimum row precharge time (=t RP)	21ns	20ns	20ns	15h	14h	14h	2
28	Minimum row active to row active delay (t RRD)	14ns	16ns	20ns	0Eh	10h	14h	2
29	Minimum RAS to CAS delay (=t RCD)	16ns	16ns	20ns	10h	10h	14h	2
30	Minimum activate to precharge time (=t RAS)	49ns	48ns	50ns	31h	30h	32h	2
31	Module bank density	1 bank of 2MB			80h			TBD
32	Address and Command signal Input setup time (=tSS)	2ns	2.5ns	2.5ns	20h	25h	25h	2
33	Address and Command signal Input hold time (=tSH)	1ns	1ns	1ns	10h	10h	10h	2
34	Data signal Input setup time (=tSS)	2ns	2.5ns	2.5ns	20h	25h	25h	2

Byte #	Function Described	Function Supported			Hex value			Note
		-7	-8	-10	-7	-8	-10	
35	Data signal Input hold time (=tSH)	1ns	1ns	1ns	10h	10h	10h	2
36	Block Write Size	8 Columns			03h			
37~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	Initial Release			00h			TBD
63	Checksum for bytes 0 ~ 62	-			C0h	DFh	34h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	9			39h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	G			47h			
81	Manufacturer part #	Blank			20h			
82	..... Manufacturer part #	2			32h			
83	Manufacturer part #	5			35h			
84	Manufacturer part #	6			36h			
85	Manufacturer part # (Component revision)	B			42h			
86	Manufacturer part # (Package type)	Q(PQFP) / P(TQFP)			51h / 50h			
87	Manufacturer part # (PCB revision)	N			4Eh			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	7	8	0	37h	38h	30h	
91	Manufacturer revision code (For PCB)	N			4Eh			
92	..... Manufacturer revision code (For component)	B			42h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~12	Manufacturer specific data (may be used in future)	-			FFh			
126	Reserved	-			FFh			
127	Reserved	-			FFh			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.