

010511

Am9341 - Am54/74181

Four Bit Arithmetic Logic Unit/Function Generator

Distinctive Characteristics:

- Provides 16 arithmetic operations including add, subtract, double and compare.
- Provides ALL 16 possible logic operations of two variables in typically 19 ns.
- Typical add time for 4 bits of only 19 ns, and typical carry time of 12 ns.
- Full look-ahead for high-speed arithmetic operation on long words.
- 100% reliability assurance testing in compliance with MIL STD 883.
- Mixing privileges for obtaining price discounts. Refer to price list.

FUNCTIONAL DESCRIPTION

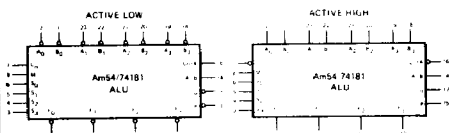
The Am54/74181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU)/Digital Function Generator. When the mode control (M) is held LOW the circuit performs under control of four function select lines 16 arithmetic operations, the most important being add and subtract, on two 4-bit parallel binary words. When the mode control is held HIGH the logic operations on an individual bit basis between the two four-bit parallel words.

An open collector A = B output is provided so that equivalence of two ALU's together.

An internal full look-ahead carry scheme is used for high-speed arithmetic operations and provision made for further look-ahead by providing carry propagate (P) and carry generate (G) outputs. These carry signals can be used as inputs to the Am54/74182 look-ahead carry generator to form long word length high-speed parallel arithmetic logic units. Addition time for sixteen-bit words with four Am54/74181 ALU's and one Am54/74182 look-ahead generator is only 31 ns.

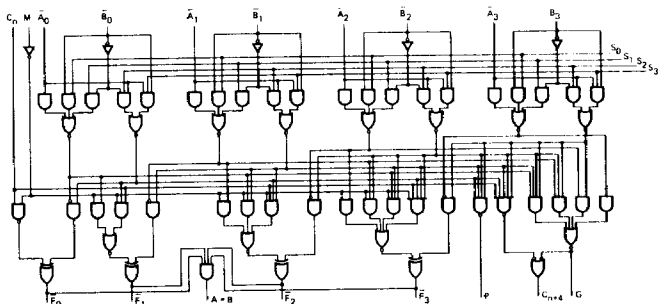
For systems where ultra high-speed is not required, the carry output signal (C_{n+1}) can be used to provide ripple-block arithmetic operations. The ALU can be used with either active HIGH or active LOW inputs and can also be expanded with the Am54/74182 look-ahead carry generator in either mode. The interconnection patterns are identical for both cases.

LOGIC SYMBOLS



V_{CC} = PIN 24
GND = PIN 12

LOGIC DIAGRAM

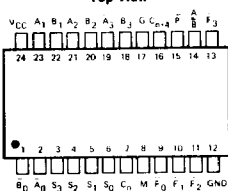


Am54/74181-Am9341 ORDERING INFORMATION

Package Type	Temperature Range	54/74181 Number	9341 Order Number
Molded DIP	0°C to +75°C	SN74181N	Am9341C
Hermetic DIP	0°C to +75°C	SN74181J	U6N934159X
Hermetic DIP	-55°C to +125°C	SN54181J	U6N934151X
Hermetic Flat Pak	0°C to +75°C	SN54181W	U4M934151X
Dice	-55°C to +125°C	SN54181D	UXK9341XXD

NOTE: The package supplied will contain units which meet both 0°C to +75°C and -55°C to +125°C temperature ranges.

CONNECTION DIAGRAM Top View



NOTE: Pin 1 is marked for orientation.

MAXIMUM R/

Storage Temper.

S (Above which the useful life may be impaired)

Temperature (Amb.) Under Bias

Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous

DC Voltage Applied to Outputs for HIGH Output State

DC Input Voltage

Output Current, Into Outputs

DC Input Current

-65°C to +150°C

-55°C to +125°C

-0.5 V to +7 V

-0.5 V to +V_{CC}

-0.5 V to +5.5 V

30 mA

-30 mA to +5 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise noted)

Am74181

T_A = 0°C to +70°CV_{CC} = 5.0V ±5% (COM'L)

MIN. = 4.75V

MAX. = 5.25V

Am54181

T_A = -55°C to +125°CV_{CC} = 5.0V ±10% (MIL)

MIN. = 4.5V

MAX. = 5.5V

Parameters

Description

Test Conditions (Note 1)

Min.

Typ.
(Note 2)

Max.

Units

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
V _{OH}	Output HIGH Voltage (Except A-B Output)	V _{CC} = MIN., I _{OH} = -800μA V _{IN} = V _{IH} or V _{IL}	2.4	3.4		Volts
V _{OL}	Output LOW Voltage	V _{CC} = MIN., I _{OL} = 16mA V _{IN} = V _{IH} or V _{IL}		0.2	0.4	Volts
V _{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2			Volts
V _{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
V _I	Input Clamp Voltage				-1.5	Volts
I _{OH}	Output HIGH Current for A-B Output	V _{CC} = MIN., I _{IN} = -12mA V _{CC} = MIN., V _{OH} = 5.5V V _{IN} = V _{IH} or V _{IL}			250	μA
I _{IL} (Note 3)	Input LOW Current	M			-1.6	mA
		A ₁ or B ₁			-4.8	
		S ₁			-6.4	
		C _n			-8	
		M			40	
I _{IH} (Note 3)	Input HIGH Current	A ₁ or B ₁			120	μA
		S ₁			160	
		C _n			200	
					1	
					-56	
I _I	Input HIGH Current	V _{CC} = MAX., V _{IN} = 5.5V			-57	mA
I _{SC}	Output Short Circuit Current (Note 4) (Except A-B Output)	V _{CC} = MAX.	Am54 -20 Am74 -18		88 127 140 135 150	mA
I _{CC}	Power Supply Current	V _{CC} = MAX.	Note 5 A		88	mA
			Am74		127	
			Note 5 B		94	
			Am54		135	
			Am74		150	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = United Load Current × Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} is measured under two conditions:
A. S₁, M, A₁ at 4.5V; all other inputs grounded; outputs open.
B. S₁, M at 4.5V; all other inputs grounded; outputs open.

DEFINITION OF TERMS**SUBSCRIPT TERMS:**

M HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS:

A_i Active LOW Data A inputs i = 0, 1, 2, 3.

A = B Open collector output. This output can be 'AND' tied to other A = B outputs to form equivalence over complete word length.

B_i Active LOW Data B inputs i = 0, 1, 2, 3.

C_n Active HIGH Carry In to nth ALU bit.

C_{n+4} Active HIGH Carry Out of n+4th ALU bit.

F_i Active LOW Data Outputs of ALU i = 0, 1, 2, 3.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

G Active LOW carry generate output for use in multi-level look-ahead schemes.

2-172M Mode input controls whether arithmetic or logic operation.

P Active LOW carry propagate output for use in multi-level look-ahead schemes.

S_i Control inputs determine the arithmetic or logic function obeyed i = 0, 1, 2, 3.

Unit Load One TTL gate input load. In the HIGH state it is equal 40μA at 2.4V and in the LOW state it is equal to 1.6mA at 0.4V.

OPERATIONAL TERMS:

I_{IL} Forward input load current, for unit input load.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{RM} Reverse input load current with V_{OH} applied to input.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage. Refer to figure 3.

V_{IL} Maximum logic LOW input voltage. Refer to figure 3.

V_{OH} Minimum logic HIGH output voltage with output HIGH current flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current flowing into output.

TEST TABLES

DIFF MODE TEST TABLE

FUNCTION INPUTS: $S_1 = S_2 = 4.5 \text{ V}$, $S_3 = S_4 = M = 0 \text{ V}$

Parameter	Input Under Test	Other Input Same Bit Apply 4.5 V	Other Input Same Bit Apply 0 V	Other Data Inputs Apply 4.5 V	Other Data Inputs Apply 0 V	Output Under Test	Output Wave-form
t_{pd+}	$\bar{A}$	None	$\bar{B}$	Remaining $\bar{A}$	Remaining B, C_n	$F_1(\geq 1)$	1
t_{pd+}	$\bar{B}$	$\bar{A}$	None	Remaining $\bar{A}$	Remaining B, C_n	$F_1(\geq 1)$	2
t_{pd+}	$\bar{A}$	None	$\bar{B}$	Remaining B, C_n	Remaining $\bar{A}$	F_{i+1}	1
t_{pd+}	$\bar{B}$	$\bar{A}$	None	Remaining B, C_n	Remaining $\bar{A}$	F_{i+1}	2
t_{pd+}	$\bar{A}$	None	$\bar{B}$	None	Remaining $\bar{A}$ and B, C_n	$\bar{P}$	1
t_{pd+}	$\bar{B}$	$\bar{A}$	None	None	Remaining $\bar{A}$ and B, C_n	$\bar{P}$	2
t_{pd+}	$\bar{A}$	$\bar{B}$	None	None	Remaining $\bar{A}$ and B, C_n	$\bar{G}$	1
t_{pd+}	$\bar{B}$	None	$\bar{A}$	None	Remaining $\bar{A}$ and B, C_n	$\bar{G}$	2
t_{pd+}	$\bar{A}$	$\bar{B}$	None	Remaining $\bar{A}$	Remaining B, C_n	$A = B$	1
t_{pd+}	$\bar{B}$	$\bar{A}$	None	Remaining $\bar{A}$	Remaining B, C_n	$A = B$	2
t_{pd+}	$\bar{A}$	$\bar{B}$	None	None	Remaining $\bar{A}$ and B, C_n	C_{i+1}	2
t_{pd+}	$\bar{B}$	None	$\bar{A}$	None	Remaining $\bar{A}$ and B, C_n	C_{i+1}	1
t_{pd+}	C_n	None	None	All $\bar{A}$ and $\bar{B}$	None	C_{i+1}	1

Table 1

SUM MODE TEST TABLE

FUNCTION INPUTS: $S_1 = S_2 = 4.5 \text{ V}$, $S_3 = S_4 = M = 0 \text{ V}$

Parameter	Input Under Test	Other Input Same Bit Apply 4.5 V	Other Input Same Bit Apply 0 V	Other Data Inputs Apply 4.5 V	Other Data Inputs Apply 0 V	Output Under Test	Output Wave-form
t_{pd+}	$\bar{A}$	$\bar{B}$	None	Remaining $\bar{A}$ and $\bar{B}$	C	$F_1(\geq 1)$	1
t_{pd+}	$\bar{B}$	$\bar{A}$	None	Remaining $\bar{A}$ and $\bar{B}$	C	$F_1(\geq 1)$	1
t_{pd+}	$\bar{A}$	$\bar{B}$	None	Remaining $\bar{A}$ and $\bar{B}$	C	F_{i+1}	1
t_{pd+}	$\bar{B}$	$\bar{A}$	None	Remaining $\bar{A}$ and $\bar{B}$	C	F_{i+1}	1
t_{pd+}	$\bar{A}$	$\bar{B}$	None	None	Remaining $\bar{A}$ and B, C	$\bar{P}$	1
t_{pd+}	$\bar{B}$	$\bar{A}$	None	None	Remaining $\bar{A}$ and B, C	$\bar{P}$	1
t_{pd+}	$\bar{A}$	None	$\bar{B}$	Remaining $\bar{A}$	Remaining $\bar{A}, C$	$\bar{G}$	1
t_{pd+}	$\bar{B}$	None	$\bar{A}$	Remaining $\bar{A}$	Remaining $\bar{A}, C$	$\bar{G}$	1
t_{pd+}	$\bar{A}$	None	$\bar{B}$	Remaining $\bar{A}$	Remaining $\bar{A}, C$	C_{i+1}	2
t_{pd+}	$\bar{B}$	None	$\bar{A}$	Remaining $\bar{A}$	Remaining $\bar{A}, C$	C_{i+1}	2
t_{pd+}	C_n	None	None	All $\bar{A}$	All $\bar{B}$	Any F or C_{i+1}	1

Table 2

LOGIC MODE TEST TABLE

FUNCTION INPUTS: $S_1 = S_2 = M = 4.5 \text{ V}$, $S_3 = S_4 = 0 \text{ V}$

Parameter	Input Under Test	Other Input Same Bit Apply 4.5 V	Other Input Same Bit Apply 0 V	Other Data Inputs Apply 4.5 V	Other Data Inputs Apply 0 V	Output Under Test	Output Wave-form
t_{pd+}	$\bar{A}$	None	$\bar{B}$	None	Remaining $\bar{A}$ and B, C	$\bar{F}$	1
t_{pd+}	$\bar{B}$	None	$\bar{A}$	None	Remaining $\bar{A}$ and B, C	$\bar{F}$	1

Table 3

SWITCHING CHARACTERISTICS $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$, $N = 10$ ($C_L = 15 \text{ pF}$, $R_i = 400 \Omega$)

Test Conditions See also Tables 1, 2, 3			Min	Typ	Max	Units
Parameter	From (Input)	To (Output)	Test Figure			
t_{pd+}	C_n	C_{i+1}	1 and 2			
t_{pd+}	C_n	F_1				
t_{pd+}	$\bar{A}$ or $\bar{B}$	$\bar{G}$				
t_{pd+}	$\bar{A}$ or $\bar{B}$	$\bar{G}$				
t_{pd+}	$\bar{A}$ or $\bar{B}$	$\bar{P}$				
t_{pd+}	$\bar{A}$ or $\bar{B}$	$\bar{P}$				
t_{pd+}	$\bar{A}$ or $\bar{B}$	$F_1(\geq 1)$				
t_{pd+}	$\bar{A}$ or $\bar{B}$	$F_1(\geq 1)$				
t_{pd+}	$\bar{A}$ or $\bar{B}$	F_{i+1}				
t_{pd+}	$\bar{A}$ or $\bar{B}$	F_{i+1}				
t_{pd+}	$\bar{A}$ or $\bar{B}$	F_i				
t_{pd+}	$\bar{A}$ or $\bar{B}$	C_{i+1}				
t_{pd+}	$\bar{A}$ or $\bar{B}$	C_{i+1}				
t_{pd+}	$\bar{A}$ or $\bar{B}$	$A = B$				
t_{pd+}	$\bar{A}$ or $\bar{B}$	$A = B$				
			M = 0 V, $S_2 = S_3 = 4.5 \text{ V}$, $S_1 = S_4 = 0 \text{ V}$ (SUM mode)			
			M = 0 V, $S_2 = S_3 = 0 \text{ V}$, $S_1 = S_4 = 4.5 \text{ V}$ (DIFF mode)			
			M = 0 V, $S_2 = S_3 = 4.5 \text{ V}$, $S_1 = S_4 = 0 \text{ V}$ (SUM mode)			
			M = 0 V, $S_2 = S_3 = 0 \text{ V}$, $S_1 = S_4 = 4.5 \text{ V}$ (DIFF mode)			
			M = 0 V, $S_2 = S_3 = 4.5 \text{ V}$, $S_1 = S_4 = 0 \text{ V}$ (SUM mode)			
			M = 0 V, $S_2 = S_3 = 0 \text{ V}$, $S_1 = S_4 = 4.5 \text{ V}$ (DIFF mode)			
			M = 4.5 V (LOGIC mode)			
			M = 0 V, $S_2 = S_3 = 4.5 \text{ V}$, $S_1 = S_4 = 0 \text{ V}$ (SUM mode)			
			M = 0 V, $S_2 = S_3 = 0 \text{ V}$, $S_1 = S_4 = 4.5 \text{ V}$ (DIFF mode)			
			M = 0 V, $S_2 = S_3 = 4.5 \text{ V}$, $S_1 = S_4 = 0 \text{ V}$ (SUM mode)			
			M = 0 V, $S_2 = S_3 = 0 \text{ V}$, $S_1 = S_4 = 4.5 \text{ V}$ (DIFF mode)			

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

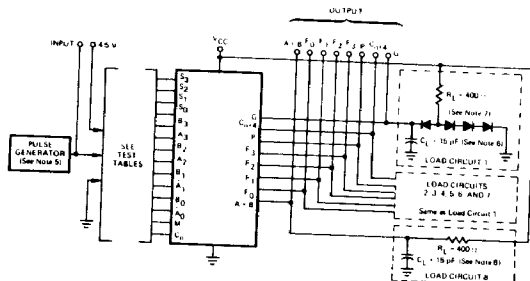


Figure 1

Note 5: The pulse generator has the following characteristics: frequency = 1 MHz, $Z_{out} \approx 50 \Omega$.
 6. C_1 includes probe and jig capacitance.
 7. All diodes are 1N3068.

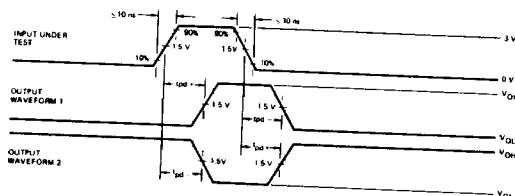
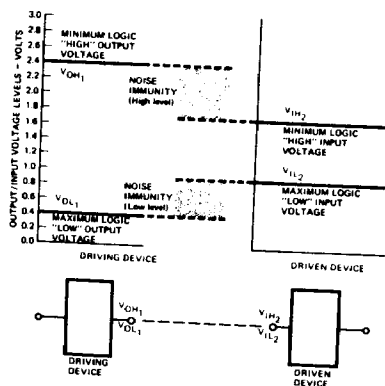


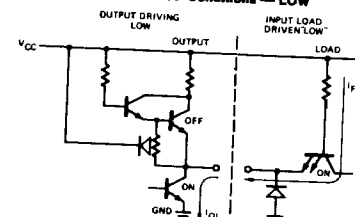
Figure 2

INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW



Current Interface Conditions — HIGH

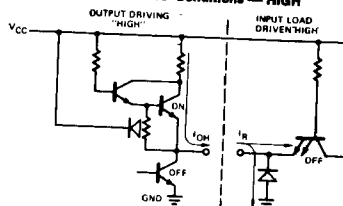


Figure 3

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load	
	HIGH	LOW
Advanced Micro Devices 54/7400 Series	1	1
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
Ti Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Table 4

USER NOTES

- Arithmetic operations are performed on a word basis.
- Logic operations are performed on a bit basis.
- Arithmetic in 1's complement arithmetic requires an end around carry.
- Subtraction in 2's complement arithmetic requires a carry in (C_n = HIGH) active LOW case, ($\bar{C}_n$ = LOW) active HIGH case.

Am54/74181 LOADING RULES (in unit loads)

Input/Output	Pin No.'s	Input Unit Load	Output Drive	
			Output HIGH	Output LOW
$\bar{B}_0$	1	3	—	—
$\bar{A}_0$	2	3	—	—
S_3	3	4	—	—
S_2	4	4	—	—
S_1	5	4	—	—
S_0	6	4	—	—
C_n	7	5	—	—
M	8	1	—	—
$\bar{F}_0$	9	—	20	10
$\bar{F}_1$	10	—	20	10
$\bar{F}_2$	11	—	20	10
GND	12	—	—	—
$\bar{F}_3$	13	—	20	10
$A = B$	14	—	O/C	10
$\bar{P}$	15	—	20	10
C_{n+1}	16	—	20	10
$\bar{G}$	17	—	20	10
$\bar{B}_1$	18	3	—	—
$\bar{A}_1$	19	3	—	—
$\bar{B}_2$	20	3	—	—
$\bar{A}_2$	21	3	—	—
$\bar{B}_3$	22	3	—	—
$\bar{A}_3$	23	3	—	—
V_{CC}	24	—	—	—

O/C = Open Collector

A unit load is defined as 40 μ A at 2.4V and 1.6mA at 0.4V.

Table 5

OPERATION TABLE

Control Inputs S_0, S_1, S_2, S_3	Active LOW Inputs and Outputs		Active HIGH Inputs and Outputs	
	Arithmetic ($M = L, C_n = L$)	Logic ($M = H$)	Arithmetic ($M = L, \bar{C}_n = H$)	Logic ($M = H$)
L L L L	A minus 1	$\bar{A}$	A	$\bar{A}$
H L L L	AB minus 1	$\bar{AB}$	A + B	A + B
L H L L	$\bar{AB}$ minus 1	A + B	A + B	$\bar{AB}$
H H L L	minus 1 (2's comp.)	Logic '1'	minus 1 (2's comp.)	Logic '0'
L L H L	A plus [A + B]	A + B	A plus AB	$\bar{AB}$
H L H L	AB plus [A + B]	$\bar{B}$	$\bar{AB}$ plus [A + B]	$\bar{B}$
L H H L	A minus B minus 1	$A \oplus B$	A minus B minus 1	$A \oplus B$
H H H L	A + B	A + B	$\bar{AB}$ minus 1	$\bar{AB}$
L L L H	A plus [A + B]	$\bar{AB}$	A plus AB	A + B
H L L H	A plus B	$A \oplus B$	A plus B	$A \oplus B$
L H L H	$\bar{AB}$ plus [A + B]	B	AB plus [A + B]	B
H H L H	A + B	A + B	AB minus 1	AB
L L H H	A plus A (2 x A)	Logic '0'	A plus A (2 x A)	Logic '1'
H L H H	A plus AB	$\bar{AB}$	A plus [A + B]	A + B
L H H H	A plus $\bar{AB}$	AB	A plus [A + B]	A + B
H H H H	A	A	A minus 1	A

L = LOW Voltage Level
H = HIGH Voltage Level

Table 6

Am54/74181 APPLICATIONS

Typical addition times for various configurations are given in the table below. Subtraction times are approximately 5 ns longer.

16-Bit ALU Ripple Carry

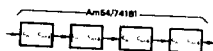


Figure 4

32-Bit ALU Two-Level Look-Ahead Over 16-Bit Groups

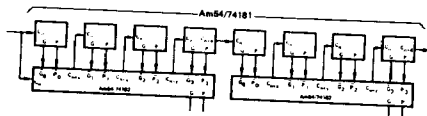


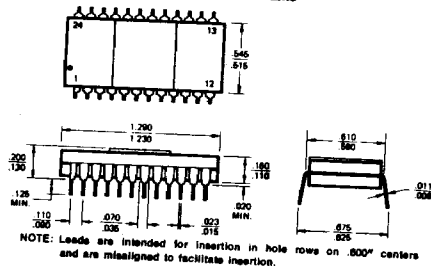
Figure 5

TYPICAL ADDITION TIMES

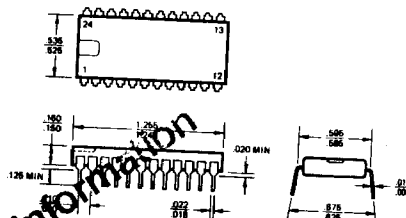
No. of Bits	Total Addition Time (ns)	Add Time Per Bit (ns)	Package Count	
			Am 54/74181	Am 54/74182
4	19	4.8	1	
8	31	3.9	2	
12	43	3.6	3	
12	31	2.6	3	1
16	55	3.5	4	
16	31	2.0	4	1
32	103	3.2	8	
32	79	2.5	8	1
32	56	1.8	8	2
48	151	3.2	12	
48	127	2.6	12	1
48	104	2.2	12	2
48	81	1.7	12	3
48	57	1.2	12	4
64	199	3.1	16	
64	152	2.4	16	2
64	129	2.0	16	3
64	106	1.7	16	4
64	57	0.9	16	5

Table 7

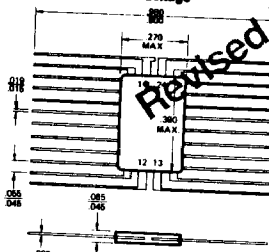
PHYSICAL DIMENSIONS Hermetic Dual-In-Line



PHYSICAL DIMENSIONS Molded Dual-In-Line

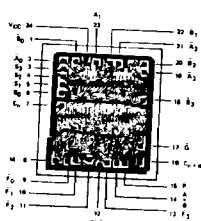


PHYSICAL DIMENSIONS Flat Package

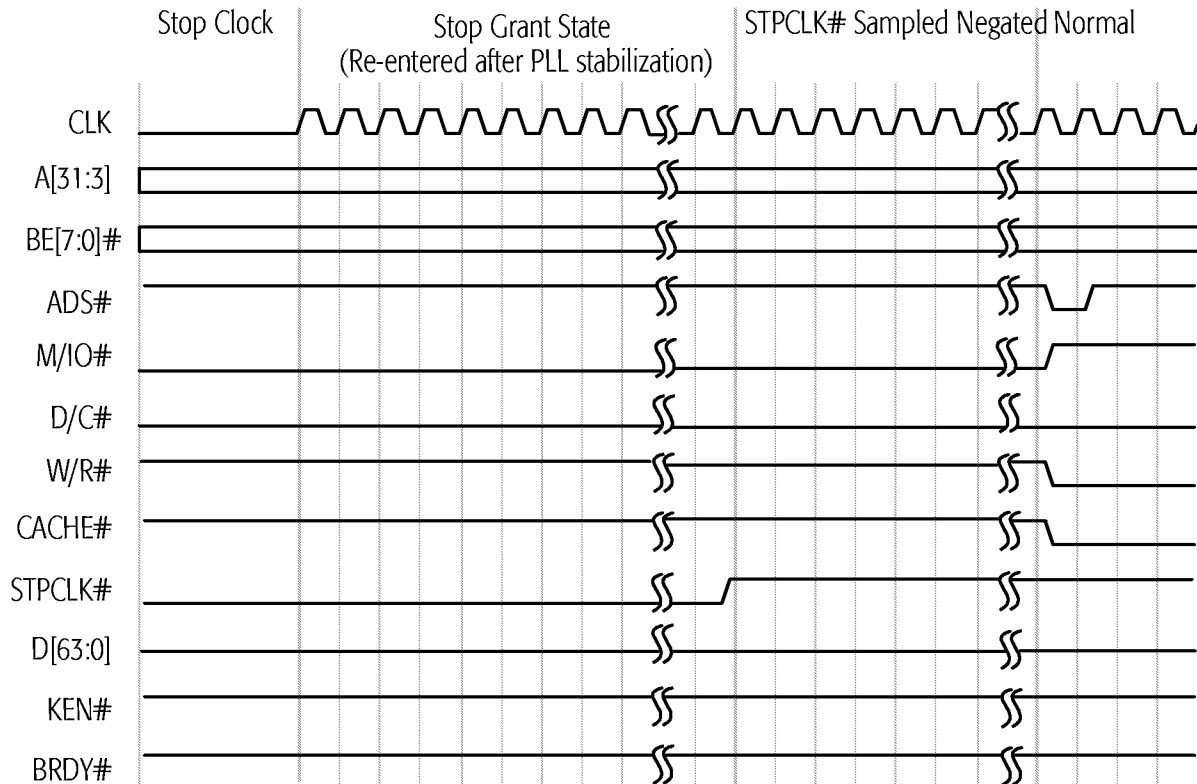


NOTE: Leads are gold plated cover.

Metallization and Pad Layout 90 x 102 Mils



ADVANCED
MICRO
DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280

**Figure 75. Stop Grant and Stop Clock Modes, Part 2**

**INIT-Initiated
Transition from
Protected Mode to
Real Mode**

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

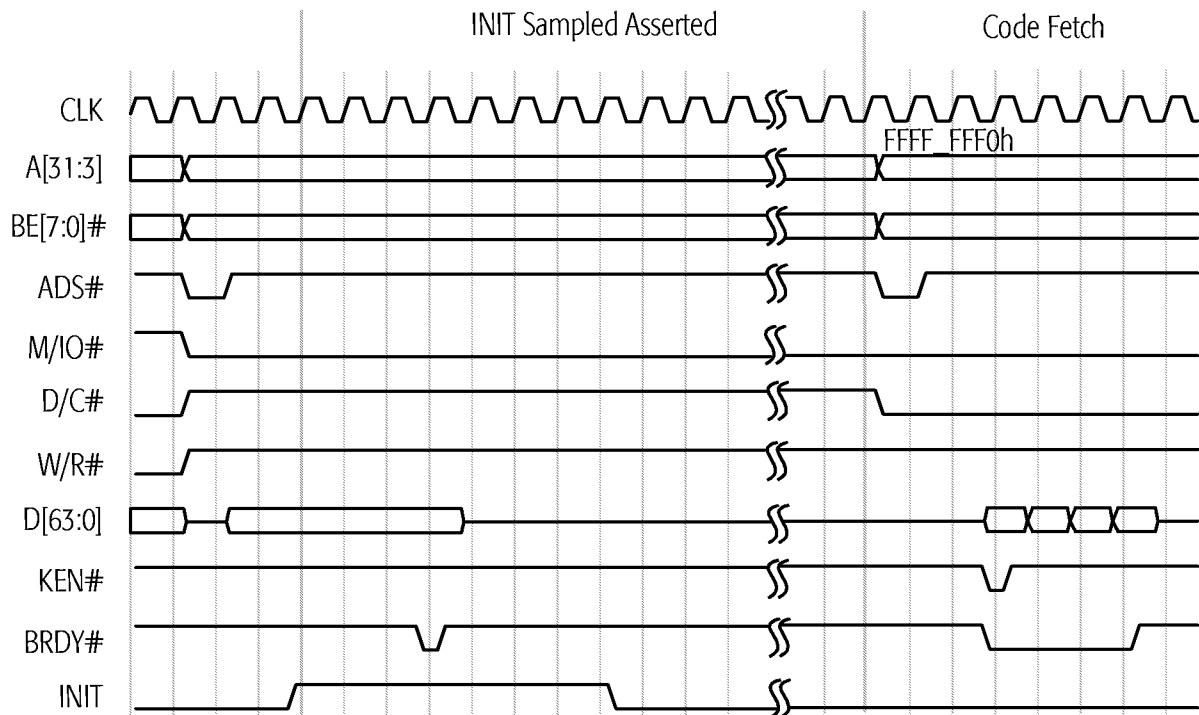


Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode

6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

6.1 Signals Sampled During the Falling Transition of RESET

- FLUSH#** FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See “Built-In Self-Test (BIST)” on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See “Tri-State Test Mode” on page 218 and “FLUSH# (Cache Flush)” on page 103 for more details.)
- BF[2:0]** The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See “BF[2:0] (Bus Frequency)” on page 92 for the processor-clock to bus-clock ratios.)
- BRDYC#** BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See “BRDYC# (Burst Ready Copy)” on page 95 for more details.)

6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification. (See “CLK Switching Characteristics” on page 255 for clock specifications. See “Electrical Data” on page 247 for V_{CC} specifications.)

During a warm reset while CLK and V_{CC} are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

6.3 State of Processor After RESET

Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

Table 31. Output Signal State After RESET

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACK#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	—	—

Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.