

# VRAM

# 256K x 16 DRAM WITH 512 x 16 SAM

NEW  
VRAM

## FEATURES

- Industry-standard pinout, timing and functions
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply (consult factory regarding 3.3V operation)
- Fully TTL and CMOS compatible inputs and TTL compatible outputs
- Refresh modes:  $\overline{RAS}$  ONLY,  $\overline{CAS}$ -BEFORE- $\overline{RAS}$  (CBR) and HIDDEN
- 512-cycle refresh within 16.7ms
- FAST-PAGE-MODE access
- Upper and lower byte  $\overline{CAS}$  control
- Dual-port organization: 256K x 16 DRAM port  
512 x 16 SAM port
- No refresh required for serial access memory
- Fast access times: 70ns random, 17ns serial  
60ns random, 15ns serial\*

## SPECIAL FUNCTIONS

- JEDEC Basic Feature Set, plus:
- PERSISTENT MASKED WRITE
- EIGHT COLUMN BLOCK WRITE (MASK)
- MASKED FLASH WRITE
- MASKED WRITE TRANSFER/SERIAL INPUT
- MASKED SPLIT WRITE TRANSFER
- PROGRAMMABLE SPLIT SAM

## OPTIONS

- Timing (DRAM, SAM [cycle/access])  
60ns, 18/15ns  
70ns, 20/17ns  
80ns, 22/20ns

## MARKING

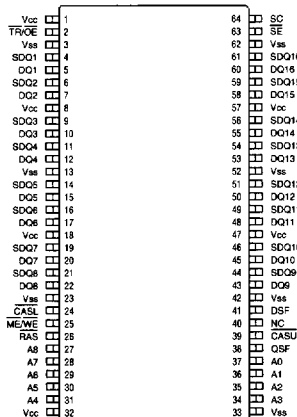
- Packages  
Plastic SOP (12 mm) SG  
Plastic TSOP(400mil) TG\*
- Part Number Example: MT42C256K16C2SG-7

## GENERAL DESCRIPTION

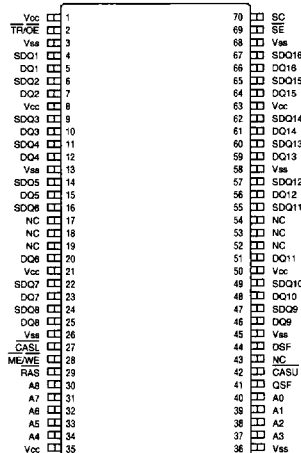
The MT42C256K16C2 is a high-speed, dual-port CMOS dynamic random access memory, or video RAM (VRAM) containing 4,194,304 bits. These bits may be accessed by a 16-bit-wide DRAM port or by a 512 x 16 bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

## PIN ASSIGNMENT (Top View)

### 64-Pin SOP (SDC-1)



### 70-Pin TSOP\* (SDE-4)



\*Consult factory for availability.

The DRAM portion of the VRAM is similar to standard 256K x 16-bit DRAMs, with the addition of BLOCK WRITE and FLASH WRITE. Sixteen 512-bit data registers make up the serial access memory portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths: the 16-bit random access I/O port, the 16 internal 512-bit-wide paths between the DRAM and the SAM, and the 16-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

Each of the ports may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of RAS

addresses are executed at least every 16.7ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C256K16C2 are optimized for high-performance graphics and communication designs. The dual-port architecture is well suited to buffering the sequential data types used in raster graphics display, serial, parallel networking and data communications. Special features such as SPLIT READ TRANSFER, extended data-out and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM

