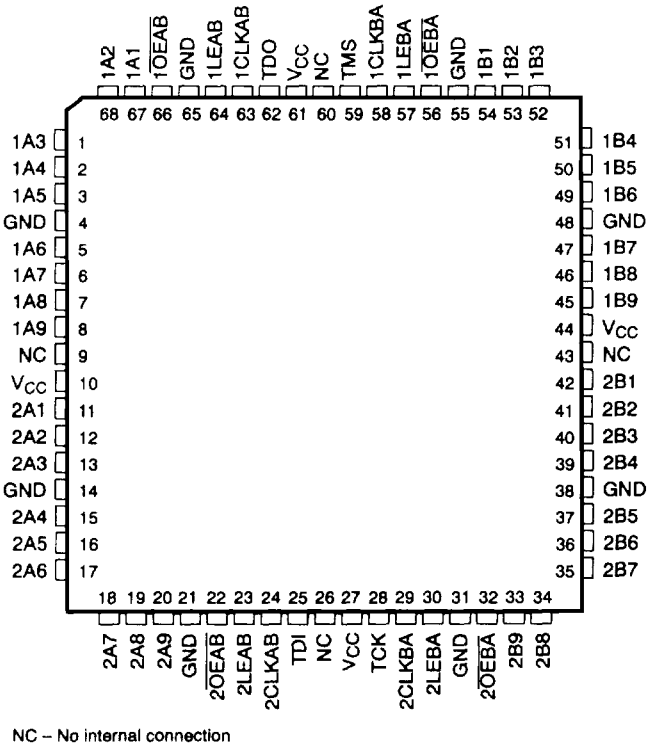
- Members of the Texas Instruments *SCOPE* ™ Family of Testability Products
- Members of the Texas Instruments *Widebus* ™ Family
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- *UBT* ™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Two Boundary-Scan Cells per I/O for Greater Flexibility
- State-of-the-Art *EPIC*-IIB ™ BICMOS Design Significantly Reduces Power Dissipation
- *SCOPE* ™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs With Masking Option
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Shrink Quad Flat Pack (PM) and 68-Pin Ceramic Quad Flat Pack (HV)

SN54ABT18502 . . . HV PACKAGE
(TOP VIEW)



NC – No internal connection

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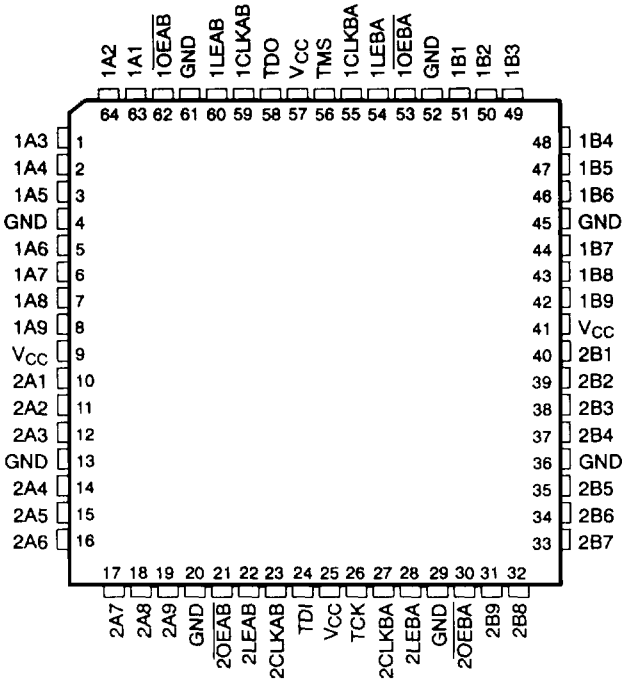
SN74ABT18502 . . . PM PACKAGE
(TOP VIEW)



description

The SN54ABT18502 and SN74ABT18502 scan test devices with 18-bit universal bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are 18-bit universal bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ registered bus transceivers.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low, A-bus data is stored on a low-to-high transition of CLKAB. When $\overline{OEAB}$ is low, the B outputs are active. When $\overline{OEAB}$ is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow but uses the $\overline{OEBA}$, LEBA, and CLKBA inputs.

In the test mode, the normal operation of the SCOPE™ universal bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

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description (continued)

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Additional flexibility is provided in the test mode through the use of two boundary scan cells (BSCs) for each I/O pin. This allows independent test data to be captured and forced at either bus (A or B). A PSA/COUNT instruction is also included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

The SN54ABT18502 is characterized over the full military temperature range of −55°C to 125°C. The SN74ABT18502 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE† (normal mode, each register)

INPUTS				OUTPUT
$\overline{OEAB}$	LEAB	CLKAB	A	B
L	L	L	X	B_0‡
L	L	↑	L	L
L	L	↑	H	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	Z

† A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established.

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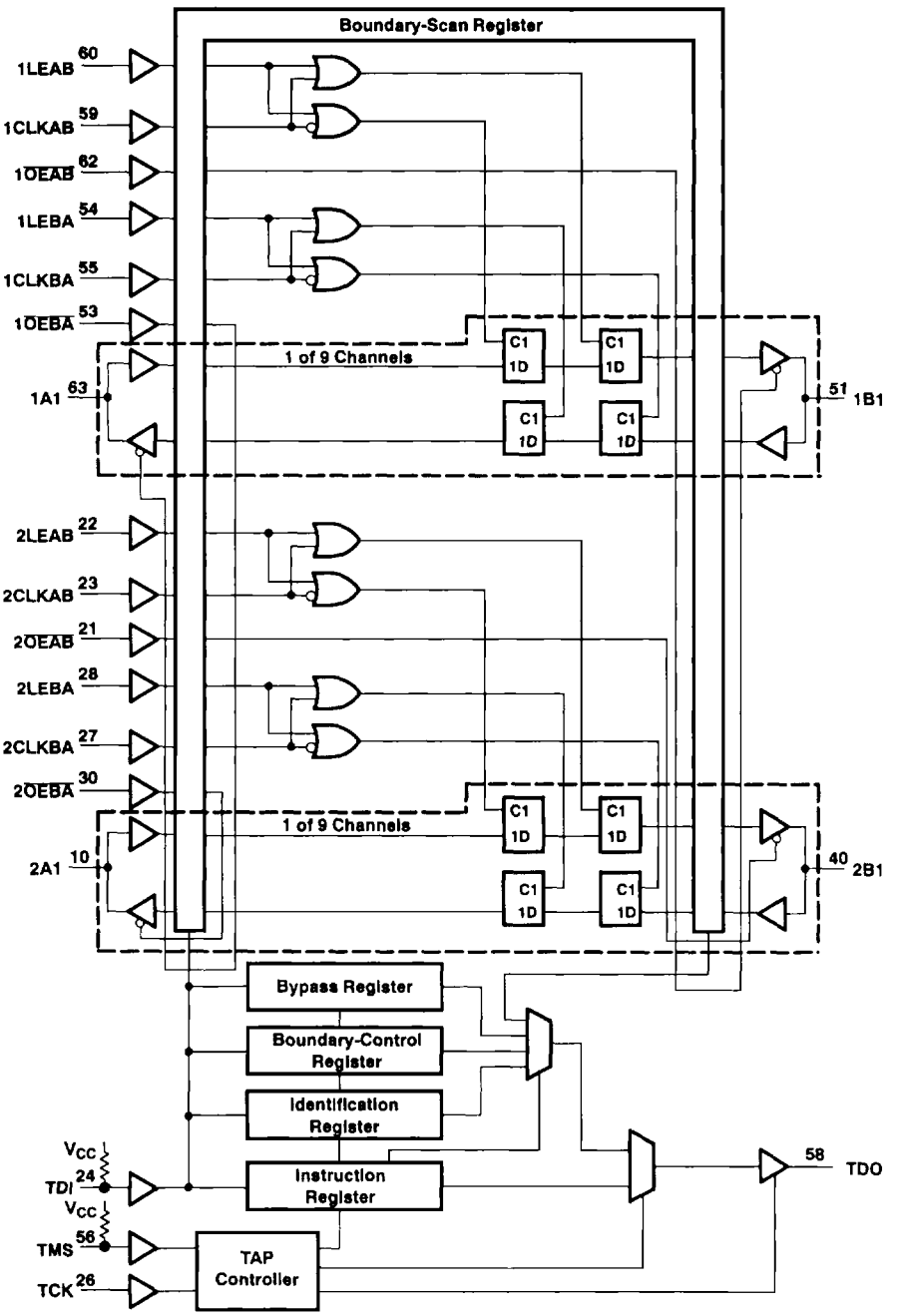
functional block diagram



Pin numbers shown are for the PM package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1) ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT18502 ..... 96 mA
SN74ABT18502 ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Maximum package power dissipation at T_A = 55°C (in still air) (see Note 2) ..... 885 mW
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. For the SN74ABT18502 (PM package), the power derating factor for ambient temperatures greater than 55°C is −10.5 mW/°C.

recommended operating conditions (see Note 3)

		SN54ABT18502		SN74ABT18502		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT18502		SN74ABT18502		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA					−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA			2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = −3 mA			3			3		3		
	V_{CC} = 4.5 V, I_{OH} = −24 mA			2			2				
	V_{CC} = 4.5 V, I_{OH} = −32 mA			2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA					0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA					0.55‡				0.55	
I_I	V_{CC} = 5.5 V,		CLK, LE, $\overline{OE}$, TCK			±1		±1		±1	µA
	V_I = V_{CC} or GND		A or B ports			±100		±100		±100	
I_{IH}	V_{CC} = 5.5 V, V_I = V_{CC}		TDI, TMS			10		10		10	µA
I_{IL}	V_{CC} = 5.5 V, V_I = GND		TDI, TMS			−160		−160		−160	µA
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V					50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V					−50		−50		−50	µA
I_{OFF}	V_{CC} = 0, V_I or V_O ≤ 5.5 V					±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V			−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V,	A or B ports	Outputs high			4		4		4	mA
	I_O = 0,		Outputs low			80		80		80	
	V_I = V_{CC} or GND		Outputs disabled			4		4		4	
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		4						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		10						pF
C_o	V_O = 2.5 V or 0.5 V		TDO		8						pF

NOTE 4: Preliminary specifications based on SPICE analysis

† All typical values are at V_{CC} = 5 V.

‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

§ The parameters I_{OZH} and I_{OZL} include the input leakage current.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 1)

			SN54ABT18502		SN74ABT18502		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA	0	100	0	100	MHz
t_w	Pulse duration	CLKAB or CLKBA high or low			3		ns
		LEAB or LEBA high			3		
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑			5		ns
		A before LEAB↓ or B before LEBA↓			4		
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑			0		ns
		A after LEAB↓ or B after LEBA↓			1		

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 1)

			SN54ABT18502		SN74ABT18502		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	50	0	50	MHz
t_w	Pulse duration	TCK high or low			5		ns
t_{su}	Setup time	A, B, CLK, LE, or $\overline{OE}$ before TCK↑			5		ns
		TDI before TCK↑			6		
		TMS before TCK↑			6		
t_h	Hold time	A, B, CLK, LE, or $\overline{OE}$ after TCK↑			0		ns
		TDI after TCK↑			0		
		TMS after TCK↑			0		
t_d	Delay time	Power up to TCK↑			50		ns
t_r	Rise time	V_{CC} power up			1		µs

NOTE 4: Preliminary specifications based on SPICE analysis

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18502		SN74ABT18502		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA		100	130		100		100		MHz
t_{PLH}	A or B	B or A						1	6	ns
t_{PHL}								1	6	
t_{PLH}	CLKAB or CLKBA	B or A						2	6	ns
t_{PHL}								2	6	
t_{PLH}	LEAB or LEBA	B or A						1.5	7.5	ns
t_{PHL}								1.5	7.5	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A						2	7.5	ns
t_{PZL}								2	7.5	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A						2	7.5	ns
t_{PLZ}								2	7.5	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18502		SN74ABT18502		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		50	90		50		50		MHz
t_{PLH}	TCK↓	A or B						3	12	ns
t_{PHL}								3	12	
t_{PLH}	TCK↓	TDO						2	7	ns
t_{PHL}								2	7	
t_{PZH}	TCK↓	A or B						3	14	ns
t_{PZL}								3	14	
t_{PZH}	TCK↓	TDO						2	8	ns
t_{PZL}								2	8	
t_{PHZ}	TCK↓	A or B						3	14	ns
t_{PLZ}								3	14	
t_{PHZ}	TCK↓	TDO						2	8	ns
t_{PLZ}								2	8	

NOTE 4: Preliminary specifications based on SPICE analysis

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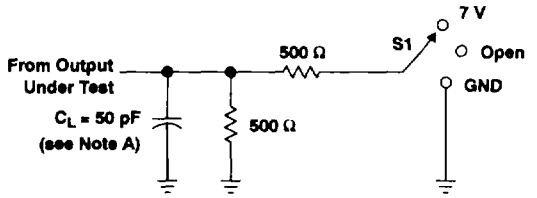
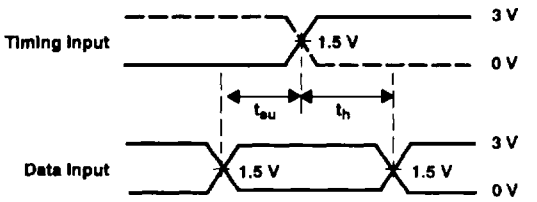
PARAMETER MEASUREMENT INFORMATION

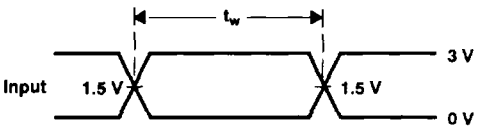


LOAD CIRCUIT FOR OUTPUTS

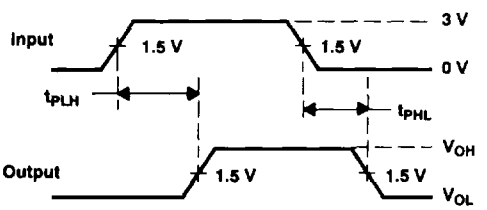
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



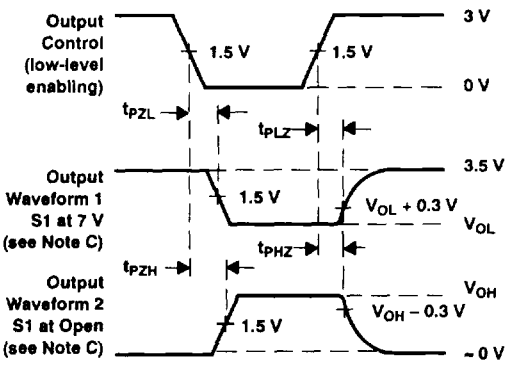
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms