Micro Linear

ML511, ML511R-Series

4, 6, 7, or 8-Channel Ferrite Read/Write Circuits

GENERAL DESCRIPTION

The ML511 is a bipolar monolithic read/write circuit designed for use with center-tapped ferrite recording heads. The ML511 and ML511R are performance upgrades from the ML501 and ML501R. The R designation in the part number indicates that this part has internal head damping resistors.

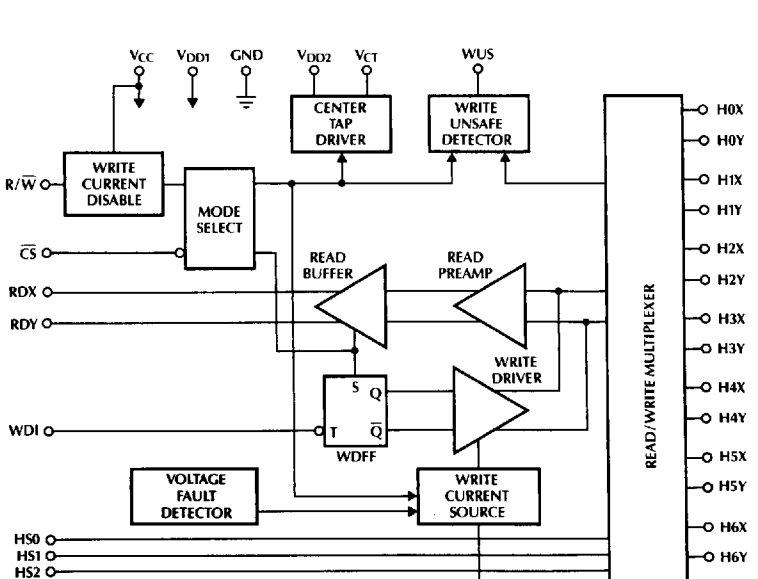
The ML511 provides up to eight multiplexed read/write data channels. These circuits exhibit features not found in similar read/write circuits such as improved write current stability and the elimination of write current "glitches" during power-up. The ML511 also provides a low noise read data path, and data protection circuitry for all of the channels.

FEATURES

- Enhanced write current stability
- ML511, ML511R is replacement for SSI 32R511/511R and is designed for center-tapped ferrite heads
- Single or multi-platter Winchester drives
- Easily multiplexed for larger systems
- Power supply fault protection
- 1.5 nV/ $\sqrt{Hz}$ maximum input noise voltage
- TTL compatible control signals
- Programmable write current source
- Includes write unsafe detection
- Available in a selection of packages
- +5 V, +12 V power supplies

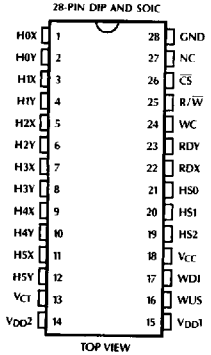
4

BLOCK DIAGRAM

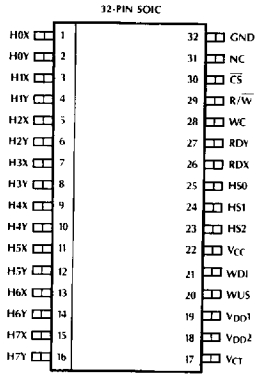


PIN CONNECTIONS

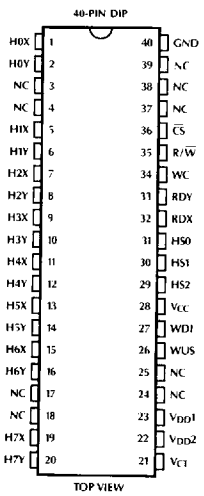
ML511-6 OR ML511R-6
6 Channels



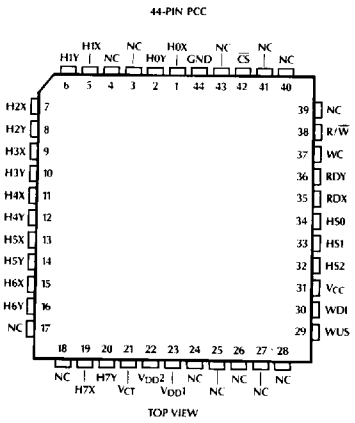
ML511-8 OR ML511R-8
8 Channels



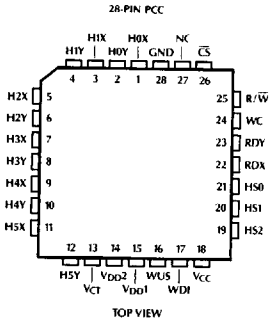
ML511-8 OR ML511R-8
8 Channels



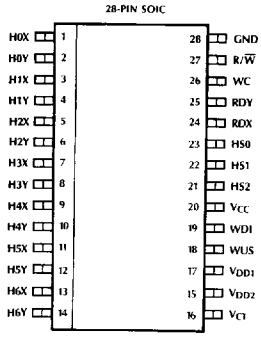
ML511-8 OR ML511R-8
8 Channels



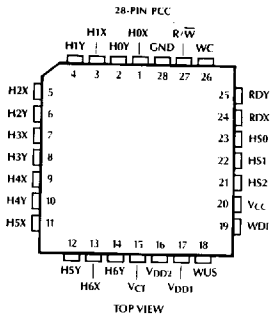
ML511-6 OR ML511R-6
6 Channels



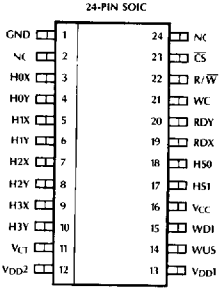
ML511R-7CS
28-Lead SOIC



ML511R-7CQ
28-Lead PCC



ML511-4 OR ML511R-4
4 Channels



PIN DESCRIPTION

NAME	FUNCTION
HS0–HS2	Head Select (eight heads)
$\overline{CS}$	Chip Select (low level enables chip)
R/$\overline{W}$	Read/$\overline{Write}$ (high level selects Read mode)
WUS	Write Unsafe, open collecter output (high level indicates an unsafe writing condition)
WDI	Write Data In (negative transition toggles head current direction)
H0X–H7X	X head connections
H0Y–H7Y	Y head connections

NAME	FUNCTION
RDX, RDY	X, Y Read Data (differential read signal out)
WC	Write Current (used to set the write current magnitude)
V_{CT}	Voltage Center Tap (center tap voltage source)
V_{CC}	+5 volts
$V_{DD}1$	+12 volts
$V_{DD}2$	Positive supply for center tap
GND	Ground

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage Range
- $V_{DD}1$ ..... −0.3 to 14 V_{DC}
- $V_{DD}2$ ..... −0.3 to 14 V_{DC}
- V_{CC} ..... −0.3 to 6 V_{DC}

Input Voltage Range
- Digital Inputs ($\overline{CS}$, R/$\overline{W}$, HS, WDI) ..... −0.3 to V_{CC} +0.3 V_{DC}
- Head Ports (H0X–H7X, H0Y–H7Y .... −0.3 to $V_{DD}1$ +0.3 V_{DC}
- Write Unsafe (WUS) ..... −0.3 to 14 V_{DC}

Write Current (I_W) ..... 60 mA

Output Current
- Read Data (RDX, RDY) ..... −10 mA
- Center Tap Current (I_{CT}) ..... −60 mA
- Write Unsafe (WUS) ..... 12 mA

Storage Temperature ..... −65°C to 150°C

Junction Temperature (T_J) ..... 135°C

Lead Temperature (Soldering 10 sec.) ..... 300°C

OPERATING CONDITIONS

Supply Voltage
- $V_{DD}1$ ..... 12 V ± 10%
- V_{CC} ..... 5 V ± 10%

Head Inductance
- L_H, ML511 or ML511R ..... 5 to 15 µH

Damping Resistor (R_D, ML511 only) ..... 500 to 2000 Ω

RCT Resistor (1/4 Watt) ..... 120 Ω ± 5%

Write Current (I_W) ..... 10 to 40 mA

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $V_{DD}1 = V_{DD}2 = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $R_{CT} = 120\Omega \pm 5\%$, $I_W = 40mA$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC OPERATING CHARACTERISTICS						
POWER SUPPLY						
I_{CC}	V_{CC} Supply Current	Read or Idle Mode			35	mA
		Write Mode			30	mA
I_{DD}	V_{DD} Supply Current	Read Mode			35	mA
		Write Mode			$20+I_W$	mA
		Idle Mode			20	mA
P_D	Power Dissipation	Read Mode			655	mW
		Write Mode $I_W = 40mA$, $R_{CT} = 0\Omega$			960	mW
		Idle Mode			455	mW
DIGITAL INPUTS ($\overline{CS}$, R/$\overline{W}$, HS, WDI)						
V_{IH}	High Voltage		2			V_{DC}
V_{IL}	Low Voltage				0.8	V_{DC}
I_{IH}	High Current	$V_{IH} = 2.0V$			100	µA
I_{IL}	Low Current	$V_{IL} = 0.8V$	−0.4			mA
WUS OUTPUT						
V_{OL}	Output Low Voltage	$I_{OL} = 8mA$ (Safe)			0.5	V_{DC}
I_{OH}	Output High Current	$V_{OH} = 5V$ (Unsafe)			100	µA
CENTER TAP VOLTAGES						
V_{CT}	Read Mode	Read Mode		4		V_{DC}
V_{CT}	Write Mode	Write Mode		6		V_{DC}

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1 = 12\,V \pm 10\%$, $V_{CC} = 5\,V \pm 10\%$, $R_{CT} = 120\Omega \pm 5\%$, $I_W = 35\,mA$, $L_H = 10\,\mu H$, $R_D = 750\Omega$ (ML511), $f_{DATA} = 5\,MHz$, C_L (RDX, RDY) $\leq 20\,pF$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3) (V_{IN} is referenced to V_{CT} for Read Mode Characteristics).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE MODE CHARACTERISTICS						
I_{HCW}	Head Current (per side)	Write Mode $0 \leq V_{CC} \leq 3.7V$ $0 \leq V_{DD}1 \leq 8.7V$	−200		200	μA
I_{WR}	Write Current Range	$I_W = K/R_{WC}$	10		40	mA
K	Write Current Constant		2.375		2.625	
V_{HD}	Differential Head Voltage Swing		7.0			V_{PK}
I_{HU}	Unselected Head Transient Current				2	mA_{PK}
C_{OD}	Differential Output Capacitance				15	pF
R_{OD}	Differential Output Resistance	ML511	10k			Ω
		$T_J = 25°C$ ML511R	600		960	Ω
f_{WDI}	WDI Transition Frequency	WUS = Low	250			kHz
A_I	I_{WC} to Head Current Gain			0.99		mA/mA
I_L	Unselected Head Leakage	Sum of X & Y Side Leakage Current			85	μA
READ MODE CHARACTERISTICS						
A_V	Differential Voltage Gain	$V_{IN} = 1mV_{P-P}$ @ 300 kHz, R_L (RDX, RDY) = 1kΩ	85		115	V/V
DR	Dynamic Range	DC Input Voltage (V_I) Where Gain Falls 10%, $V_{IN} = V_I + 0.5\,mV_{P-P}$ @ 300 kHz	−3		+3	mV
BW	Bandwidth (−3 dB)	$\|Z_S\| < 5\Omega$, $V_{IN} = 1mV_{P-P}$	30			MHz
e_{IN}	Input Noise Voltage	BW = 15 MHz, $L_H = 0$, $R_H = 0$			1.5	nV/ $\sqrt{Hz}$
C_{IN}	Differential Input Capacitance	f = 5 MHz			20	pF
R_{IN}	Differential Input Resistance	f = 5 MHz, $T_J = 25°C$ ML511	2k			Ω
		$V_{IN} = 6mV_{P-P}$ ML511R	460		860	Ω
I_{HCR}	Head Current (per side)	Read or Idle Mode $0 \leq V_{CC} \leq 5.5V$ $0 \leq V_{DD}1 \leq 13.2V$	−200		200	μA
I_{IN}	Input Bias Current (1 side)				45	μA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = V_{CT} + 100\,mV_{P-P}$ @ f = 5 MHz	50			dB
PSRR	Power Supply Rejection Ratio	$100\,mV_{P-P}$ @ 5 MHz on $V_{DD}1$, $V_{DD}2$, or V_{CC}	45			dB
CS	Channel Separation	Unselected Channels: $V_{IN} = 100\,mV_{P-P}$ @ 5 MHz and Selected Channel: $V_{IN} = 0\,mV_{P-P}$	45			dB
V_{OS}	Output Offset Voltage	Read Mode	−460		+460	mV
		Write or Idle Mode	−20		+20	mV
V_{OCM}	Common-Mode Output Voltage	Read Mode	4.5		6.5	V
		Write or Idle Mode		5.3		V
R_{OUT}	Single-Ended Output Resistance	f = 5 MHz			30	Ω
I_L	Leakage Current, RDX, RDY	(RDX, RDY) = 6V Write or Idle Mode	−100		100	μA
I_O	Output Current	AC Coupled Load, RDX to RDY	±2.1			mA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1 = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $R_{CT} = 120\Omega \pm 5\%$, $I_W = 35mA$, $L_H = 10\mu H$, $R_D = 750\Omega$ (ML511), $f_{DATA} = 5MHz$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3).

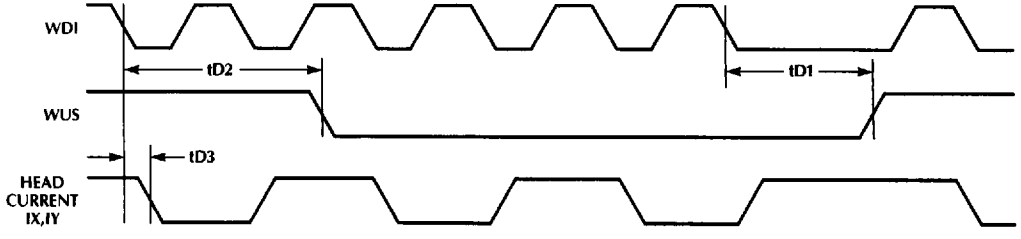
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS						
t_{RW}	R/$\overline{W}$ to Write Switching Delay	To 90% of Write Current Output			1	µs
t_{WR}	R/$\overline{W}$ to Read Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current			1	µs
t_{IW} or t_{IR}	$\overline{CS}$ to Select Switching Delay	To 90% of Write Current or to 90% of 100mV, 10MHz Read Signal Envelope			1	µs
t_{WI} or t_{RI}	$\overline{CS}$ to Unselect Switching Delay	To 90% Decay of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current			1	µs
t_{HS}	Head Select Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope			1	µs
tD1	Safe to Unsafe Write Unsafe Delay	$I_W = 35mA$	1.6		8	us
tD2	Unsafe to Safe Write Unsafe Delay	$I_W = 35mA$			1	us
tD3	Prop. Delay Head Current	$L_H = 0$, $R_H = 0$ From 50% points			25	ns
	Asymmetry Head Current	WDI has 50% Duty Cycle and 1nS Rise/Fall Time			2	ns
	Rise/Fall Head Current	10% and 90% Points			20	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 3: Maximum junction temperature (T_J) should not exceed 135°C.

TIMING DIAGRAM



Write Mode Timing Diagram

FUNCTIONAL DESCRIPTION

CIRCUIT OPERATION

For any selected head, the ML511 functions as a read amplifier when in the Read mode, or as a write current switch when in the Write mode. Pins HS0, HS1 and HS2 determine head selection while pin R/$\overline{W}$ controls the Read/Write mode. A detected "write-unsafe" condition is indicated by pin WUS.

READ MODE

When the ML511 is in the Read Mode, it operates as a low-noise differential amplifier on the selected channel. In Read mode the write data flip-flop is set and both the write unsafe detector and the write current source are deactivated. The center tap voltage is also lowered. Pins RDX and RDY provide differential emitter follower outputs which are in phase with the X and Y head input pins.

Note that during the Read or Chip Deselect mode the internal write current is deactivated, thus making external write current gating unnecessary.

WRITE MODE

The ML511 operates as a write-current switch when in the Write mode. Write current magnitude is determined by the following relationship:

$I_W = K/R_{WC}$

Where: K = Write Current Constant

R_{WC} = Resistance connected between pin WC and GND.

The head current is toggled between the X and Y side of the selected head by a negative transition on WDI (Write Data Input). When switching the ML511 to write mode, the WDFF (Write Data Flip-Flop) is initialized to pass write current through the X-side of the head.

The ML511, ML511R exhibit enhanced write current stability, compared to similar read/write circuits, which reduces the problem of oscillation. This is a result of increased internal write current compensation. Also, write current "glitches" during power-up, common in similar read/write circuits, are eliminated with an exclusive write current disabling function.

The WUS (Write Unsafe) pin is an open collector output that gives a logic high level for any of the following unsafe write conditions:

- Open head
- Open head center-tap
- Too low WDI frequency
- Read mode selected
- Device not selected
- No write current

Two negative transitions on WDI are required to clear WUS after the fault condition is removed.

The ML511 also offers a voltage fault detection circuit that prevents write current during power-loss or power-up.

Table 1.

Head Select

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

0 = Logic Level Low
1 = Logic Level High
X = Don't Care

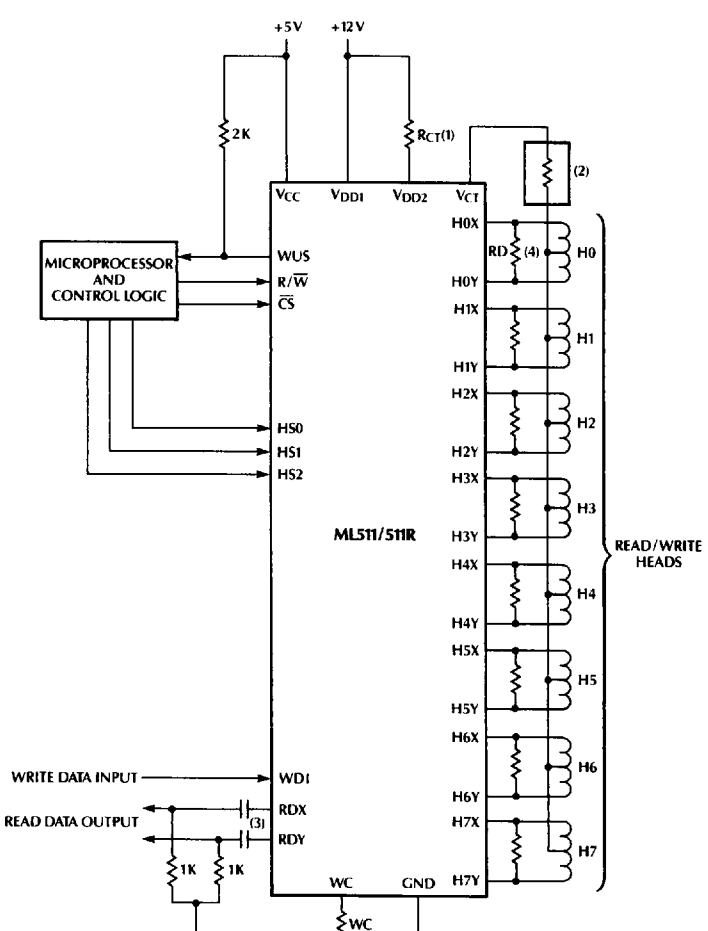
Table 2.

Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

0 = Logic Level Low
1 = Logic Level High
X = Don't Care

TYPICAL APPLICATION



NOTES:

1. RCT is optional and is used to limit internal power dissipation (Otherwise connect $V_{DD}1$ to $V_{DD}2$).
   RCT (1/2 Watt) = 120 (40/I_W) ohms
   where I_W = Write Current, in mA
2. Ferrite bead optional: used to suppress write current overshoot and ringing. Recommend Ferroxcube 3659065/4A6.
3. RDX and RDY load capacitance 20 pF maximum. RDX and RDY output current must be limited to 100 μA.
4. Damping resistors not required on ML511R.

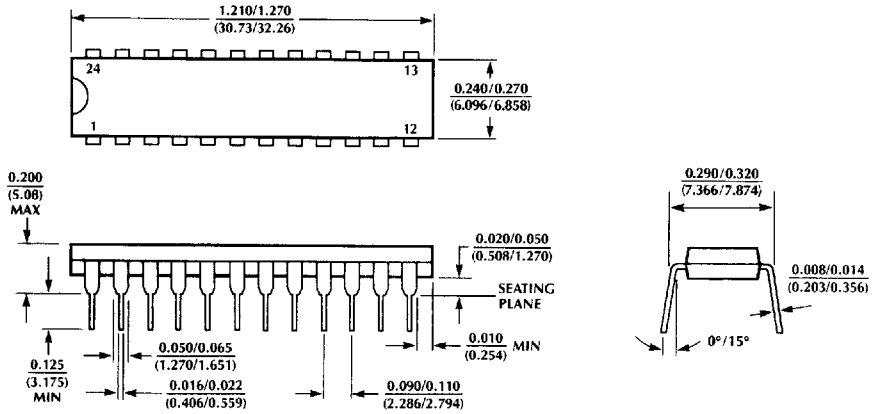
ORDERING INFORMATION

PART NUMBER	NUMBER OF CHANNELS	PACKAGE
ML511CS-4	4	24- Pin SOIC (S24)
ML511R CS-4	4	24- Pin SOIC (S24)
ML511CP-6	6	28- Pin Narrow DIP (P28)
ML511R CP-6	6	28- Pin Narrow DIP (P28)
ML511CQ-6	6	28- Pin PLCC (Q28)
ML511R CQ-6	6	28- Pin PLCC (Q28)
ML511CS-6	6	28- Pin SOIC (S28)
ML511R CS-6	6	28- Pin SOIC (S28)
ML511R CQ-7	7	28- Pin PLCC (Q28)
ML511R CS-7	7	28- Pin SOIC (S28)
ML511CP-8	8	40- Pin DIP (P40)
ML511R CP-8	8	40- Pin DIP (P40)
ML511CQ-8	8	44- Pin PLCC (Q44)
ML511R CQ-8	8	44- Pin PLCC (Q44)
ML511CS-8	8	32- Pin SOIC (S32)
ML511R CS-8	8	32- Pin SOIC (S32)

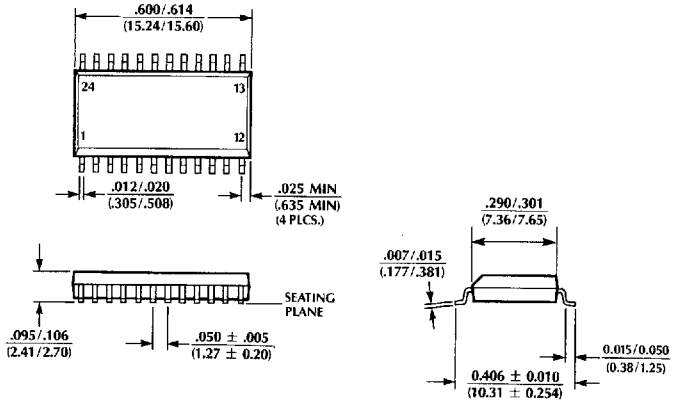
THERMAL CHARACTERISTICS

PIN COUNT	PACKAGE	θ_{JA}
24-Pin	SOIC	75°C/W
28-Pin	PDIP	55°C/W
28-Pin	PLCC	65°C/W
28-Pin	SOIC	70°C/W
32-Pin	SOIC	60°C/W
44-Pin	PLCC	60°C/W
40-Pin	PDIP	45°C/W

Package: P24N
24-Pin Molded DIP (Narrow)

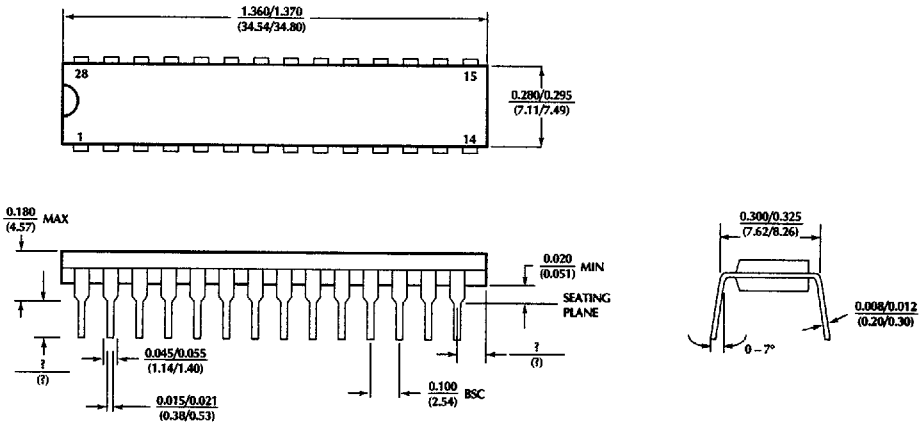


Package: S24W
24-Pin SOIC

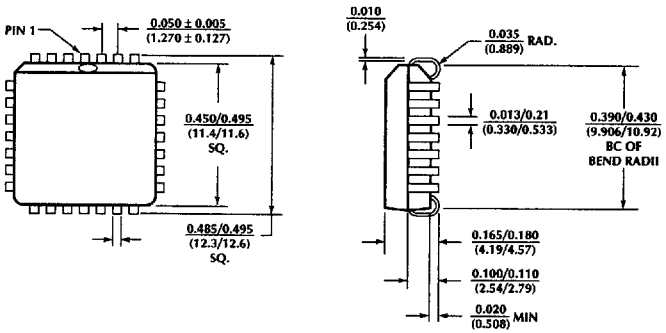


9

Package: P28N
28-Pin Molded DIP (Narrow)

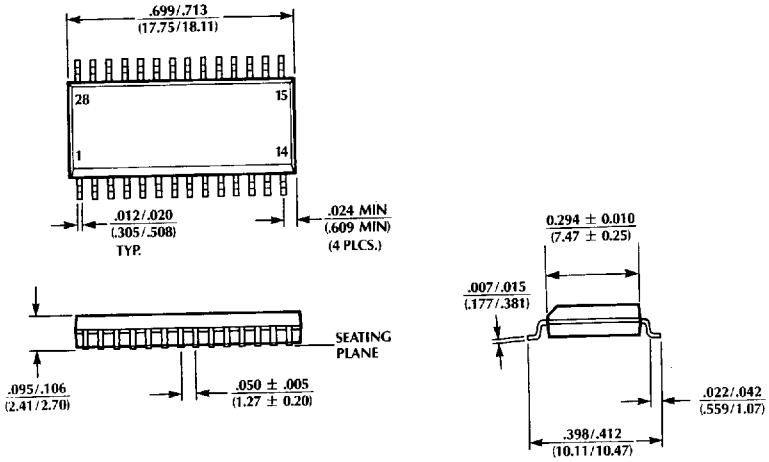


Package: Q28
28-Pin Molded Leaded PCC

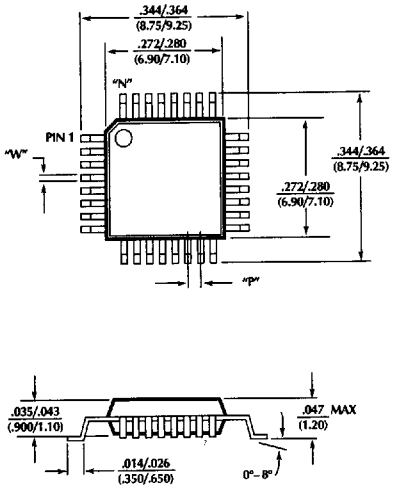


9

Package: S28W
28-Pin SOIC

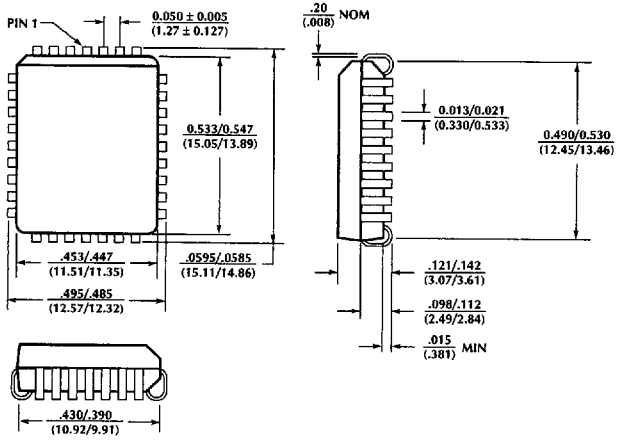


Package: H32, H48
32-Pin TQFP, 48-Pin TQFP

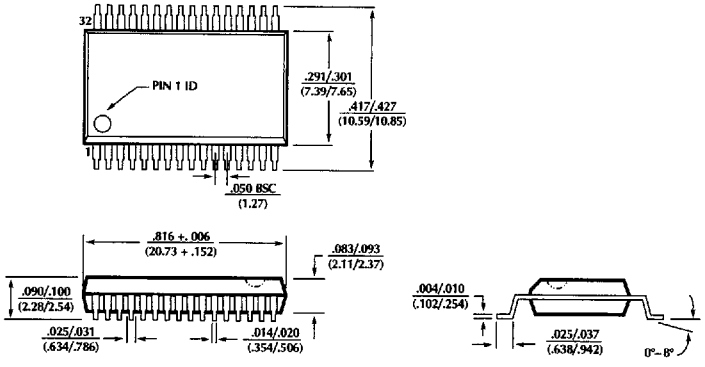


"N"	32L	48L
"P"	.315 BASIC (.80)	.0197 BASIC (.50)
"W"	.009/.015 (.23/.38)	.008/.012 (.20/.30)
PACKAGE ID	H32	H48

Package: Q32
32-Pin Molded Leaded PCC

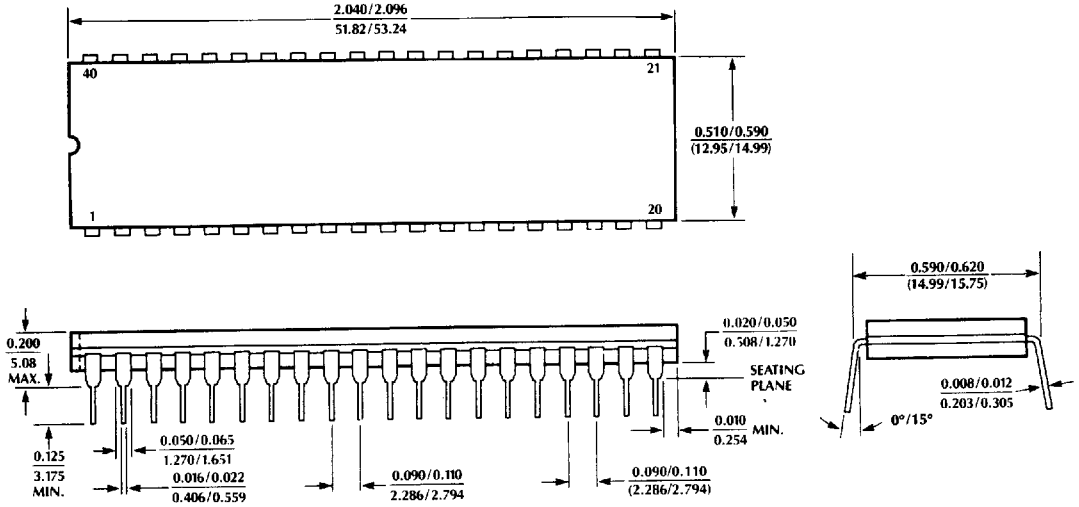


Package: S32W
32-Pin SOIC

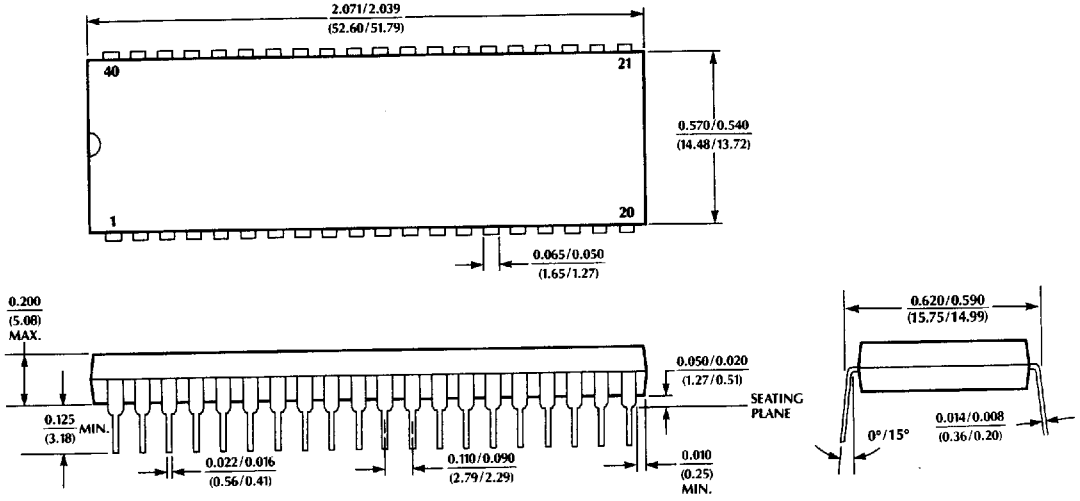


9

Package: J40
40-Pin Hermetic DIP (CERDIP)

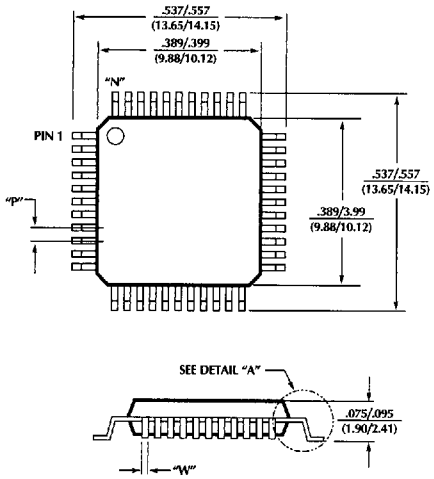


Package: P40
40-Pin Molded Plastic DIP

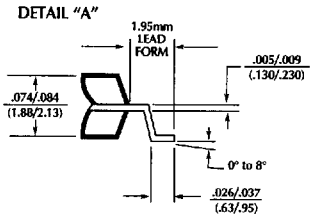


Micro Linear

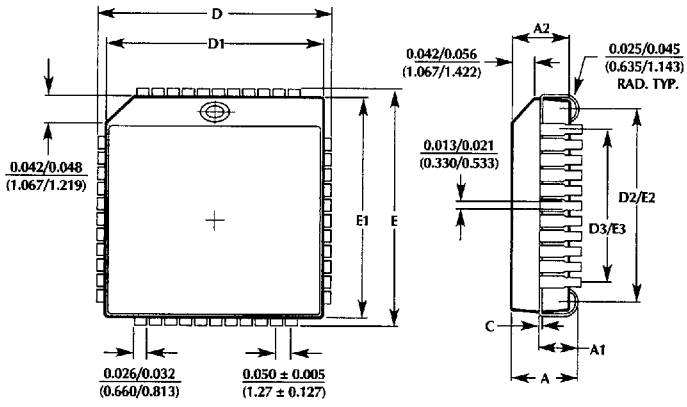
Package: G44, G52
44-Pin PQFP, 52-Pin PQFP



"N"	44L		52L	
"P"	.0315	(.80) BSC	.0265	(.65) BSC
"W"	.012/.018	(.30/.45)	.090/.014	(.22/.35)
PACKAGE ID	G44		G52	



Package: Q44, Q52, Q68, Q84
44-Pin, 52-Pin, 68-Pin and 84-Pin Molded Leaded PCC



Lead Count	44L	52L	68L	84L
A	0.165/0.180 (4.191/4.572)	0.165/0.180 (4.191/4.572)	0.165/0.180 (4.191/4.572)	0.165/0.180 (4.191/4.572)
A1	0.100/0.110 (2.540/2.794)	0.100/0.110 (2.540/2.794)	0.095/0.118 (2.413/2.997)	0.095/0.118 (2.413/2.997)
A2	0.148/0.156 (3.759/3.962)	0.148/0.156 (3.759/3.962)	0.146/0.154 (3.708/3.911)	0.146/0.154 (3.708/3.911)
D	0.685/0.695 (17.39/17.65)	0.785/0.795 (19.94/20.19)	0.985/0.995 (25.02/25.27)	1.185/1.195 (30.09/30.35)
D1	0.650/0.654 (16.51/16.61)	0.750/0.754 (19.05/19.15)	0.950/0.954 (24.13/24.23)	1.150/1.154 (29.21/29.31)
D2	0.590/0.630 (14.99/16.00)	0.690/0.730 (17.53/18.54)	0.890/0.930 (22.61/23.62)	1.090/1.130 (27.69/28.70)
D3	0.500 REF (12.70 REF)	0.600 REF (15.24 REF)	0.800 REF (20.32 REF)	1.00 REF (25.40 REF)
E	0.685/0.695 (17.39/17.65)	0.785/0.795 (19.94/20.19)	0.985/0.995 (25.02/25.27)	1.185/1.195 (30.09/30.35)
E1	0.650/0.654 (16.51/16.61)	0.750/0.754 (19.05/19.15)	0.950/0.954 (24.13/24.23)	1.150/1.154 (29.21/29.31)
E2	0.590/0.630 (14.99/16.00)	0.690/0.730 (17.53/18.54)	0.890/0.930 (22.61/23.62)	1.090/1.130 (27.69/28.70)
E3	0.500 REF (12.70 REF)	0.600 REF (15.24 REF)	0.800 REF (20.32 REF)	1.00 REF (25.40 REF)
C	0.009/0.0103 (0.228/0.261)	0.009/0.0103 (0.228/0.261)	0.007/0.008 (0.178/0.203)	0.007/0.008 (0.178/0.203)
PACKAGE ID	Q44	Q52	Q68	Q84