

LXT2361

Integrated STS-1 Line Interface Transceiver

General Description

The LXT2361 is a line interface transceiver IC intended for STS-1 (51.84 Mbit/s) applications. The receiver has a very wide dynamic range and is designed to accept B3ZS-encoded bipolar inputs; it provides clock, positive data, negative data, and low-level signal detector logical outputs.

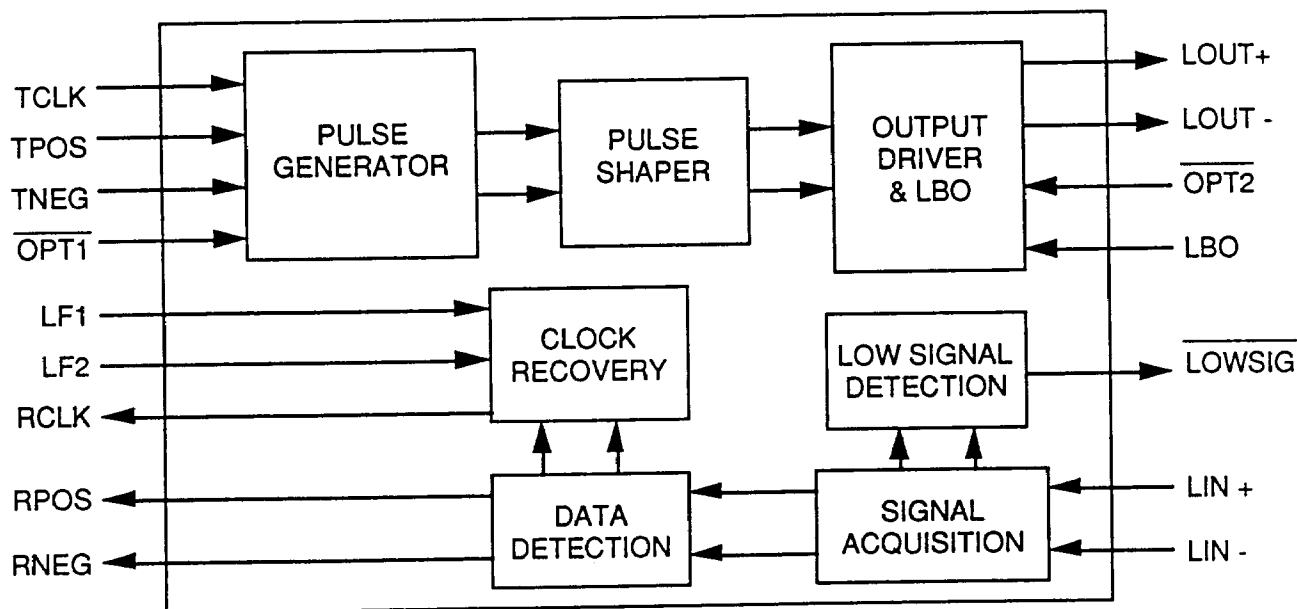
The transmitter converts clock and data input signals into AMI pulses of the appropriate shape for transmission. A line buildout (LBO) equalizer may be selected to shape the outgoing pulses for shorter line lengths.

The LXT2361 requires a single 5-volt supply and is available in DIP and surface mount packages.

Features

- Single chip STS-1 (51.84 Mbps) transmit and receive line interface
- Advanced clock recovery circuit - requires no crystals, tuned components or external clock
- Selectable LBO for shorter line lengths
- Standard CMOS level unipolar POS/NEG data and CLK ports
- Low-level input signal indication
- Pin and function compatible with SSI 78P2361
- Available in DIP and PLCC

LXT2361 Block Diagram



FUNCTIONAL DESCRIPTION

The LXT2361 is a single chip line interface IC designed to work with 51.84 Mbit/s STS-1 signals. The receiver recovers 51.84 MHz clock, positive data and negative data from a bipolar signal which has travelled a maximum of 450 feet from a crosspoint over 75 Ω coaxial cable (cable type WECO 728A, RG-59B or equivalent). The wide dynamic range of LXT2361 allows for additional resistive attenuation. The input STS-1 signal should be B3ZS coded.

The transmitter accepts CMOS level logical clock, positive data and negative data and converts them to the AMI signal to drive a 75 Ω coaxial cable. Programmable internal Line Buildout (LBO) circuitry eliminates the need for external LBO networks. The shape of the transmitted signal through any cable length of 0 to 450 feet will match a scaled DS-3 template. The LXT2361 is designed to work with a B3ZS coded signal. The B3ZS encoding and decoding functions are normally included in the STS-1 framer ICs or can easily be implemented in a PAL.

RECEIVER

The receiver input is normally transformer-coupled to the STS-1 signal. The inputs to the IC are internally referenced to RVCC so that when no transformer is used, a DC blocking capacitor of 0.01 μ F should be used to isolate these pins from the STS-1 signal. Since the input impedance of the LXT2361 is high, the STS-1 line must be terminated in 75 Ω . The input signal to the LXT2361 must be limited to a maximum of two consecutive zeros using a coding scheme such as B3ZS.

The STS-1 signal is input to a variable gain differential amplifier whose output is maintained at a constant voltage level regardless of the input voltage level. The gain of this amplifier is adjusted by detecting the peak of the signal and comparing it to a fixed reference.

The output of the variable gain amplifier is compared to a threshold value which is a fixed percentage of the signal peak. In this way, even though the input signal amplitude may fall below the minimum value that can be regulated by the variable gain circuit, the proper detection threshold is maintained.

Output of the data comparators are connected to the clock recovery circuits. The clock recovery system employs a unique phase locked loop which has an auxiliary frequency-sensitive acquisition loop which is

active only when cycle-slipping occurs between the received signal rate and the internal oscillator.

This system permits the loop to independently lock to the frequency and phase of the incoming data stream without the need for high precision and/or adjustable oscillator or tuned circuits.

The response characteristic for the phase locked loop is established by external filter components, RLF1, RLF2 and CLF1. The values of these components are specified such that the bandwidth of the phase locked loop is greater than 200 kHz.

Figure 2 shows the recovered clock (RCLK), positive data (RPOS) and negative data (RNEG) signals timing. The data is valid on the rising edge of the clock. The minimum setup and hold times allow easy interface to many STS-1 framer circuits. These signals are CMOS-level outputs.

Should the input signal fall below a minimum value, the LOWSIG pin goes active low. A time delay is provided before this output is active so the transient interruptions do not needlessly cause the indication.

TRANSMITTER

The transmitter accepts unipolar CMOS level logical clock, positive data and negative data signals (TCLK, TPOS, TNEG) and generates high current drive pulses on the LOUT+ and LOUT- pins. When properly connected to a center tapped transformer, a bipolar pulse is generated which can drive a 75 Ω coaxial cable (type WE728A or RG59B).

Figure 3 shows the timing for the transmitter logic signals. The output pulse width is internally set and is not sensitive to input clock (TCLK) pulse width.

The LXT2361 incorporates a selectable Line Buildout (LBO) equalizer in the transmitter path. The LBO pin should be set HIGH if the cable is shorter than 225 feet. For longer cable lengths, the LBO pin should be set LOW.

The $\overline{\text{OPT1}}$ pin should be set HIGH for normal operation. Setting the $\overline{\text{OPT1}}$ pin to LOW increases the transmitter power.

The $\overline{\text{OPT2}}$ pin should be set HIGH for normal operation. Setting the $\overline{\text{OPT2}}$ pin to LOW disables the transmitter circuitry and reduces the power consumption of the IC by 125 mW.

PIN DESCRIPTION

RECEIVER

NAME	TYPE	DESCRIPTION
LIN+, LIN-	I	Differential inputs, transformer-coupled from line.
RPOS	O	Unipolar receiver output, active as result of positive pulse at inputs.
RNEG	O	Unipolar receiver output, active as result of negative pulse at inputs.
RCLK	O	Clock pulses recovered from line data.
LOWSIG	O	Low signal logic output indicating that input signal is less than threshold value.

TRANSMITTER

TPOS	I	Unipolar transmitter data input, active high.
TNEG	I	Unipolar transmitter data input, active high.
TCLK	I	Transmitter clock input, active high.
LOUT+	O	Output to transformer for positive data pulses.
LOUT-	O	Output to transformer for negative data pulses.
LBO	I	Line buildout control. Selected for shorter cable lengths.
OPT1	I	Transmit option 1. Set high for STS-1 operation. Selects faster output pulse transition time and higher amplitude when low.
OPT2	I	Transmit option 2. Disables output driver and reduces output bias current when low.

EXTERNAL COMPONENT CONNECTION

RFO	I	Resistor connected to RGND to provide basic center frequency of receiver phase locked loop oscillator.
LF1, LF2	-	Resistor-capacitor loop filter network to establish bandwidth of phase locked loop.

POWER

TVcc	-	5V power supply for transmit circuits.
RVcc	-	5V power supply for receive circuits.
DVcc	-	5V power supply for receive logic circuits.
TGND	-	Ground return for transmit circuits.
RGND	-	Ground return for receive circuits.
DGND	-	Ground return for receive logic circuits.
NC	-	No connect. These pins are not connected to the chip. They should be tied to the appropriate ground pin (see figure 1) to minimize pin-to-pin coupling capacitance.

ELECTRICAL SPECIFICATIONS

(TA = -40°C to 85°C, Vcc = 5V ±5%, unless otherwise noted.) Currents flowing into the chip are positive. Current maximums are currents with the largest absolute value. Operation above absolute maximum ratings may permanently damage the device.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive 5.0V supply: TVcc, RVcc, DVcc	6.0	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Ambient Operating Temperature, TA	-40 to +85	°C
Pin Ratings: LIN+, LIN-, TPOS, TNEG, TCLK, LOUT+, LOUT-, LBO, RFO, LF2, LF1, OPT1, OPT2 Pins	-0.3 to Vcc +0.3	V
Pin Ratings: RPOS, RNEG, RCLK, LOWSIG Pins	-0.3 to Vcc +0.3 or +12	V mA

SUPPLY CURRENTS AND POWER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ICC Supply Current	Outputs Unloaded, normal operation, transmit and receive all 1's pattern		142	174	mA
P Power Dissipation	Outputs unloaded, TA = 85°C			0.93	W

EXTERNAL COMPONENTS (Refer to Figure 1 for location of components.)

RFO	Loop center frequency resistor	1% tolerance		4.53		kΩ
RLF1	Loop filter resistor	1%		20		kΩ
RLF2	Loop filter resistor	5%		100		kΩ
CLF1	Loop filter capacitor	5%		0.22		μF
	Transmit line transformer			TBD		
	Receive line transformer			TBD		
RTR	Receive termination resistor	1%		75		Ω
CTT	Transmit termination capacitor	5%		20		pF

ELECTRICAL SPECIFICATIONS (Continued)

DIGITAL INPUTS AND OUTPUTS

(CMOS-compatible pins: LOWSIG, RPOS, RNEG, RCLK, TPOS, TNEG, TCLK, LBO, OPT1.) Currents flowing into the chip are positive. Current maximums are currents with the largest absolute value.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VIL	Input low voltage	-0.3		1.5	V
VIH	Input high voltage	3.5		V _{CC} +0.3	V
IIL	Input low current	VIL = 1.5V		5.0	μA
IIH	Input high current	VIH = 3.5V		5.0	μA
VOL	Output low voltage	IOL = 0.1 mA		1.0	V
VOH	Output high voltage	IOH = -0.1 mA	4.0		V

OPT2 CHARACTERISTICS

VIL	Input low voltage	IIL = 0.4 mA			0.5	V
VIH	Input high voltage		2.0			V

RECEIVER

All of the measurements for the receiver are made with the following conditions unless otherwise stated:

1. The input signal is transformer coupled as shown in Figure 1.
2. RFO = 4.53 kΩ
3. The circuit is connected as in Figure 1.
4. The maximum cable length (type 728-A or RG-59B) to DSX-3 point is 450 ft.

VIN	Input signal voltage	Input AC-Coupled	±0.045		±1.20	V _{pk}
RIN	Input Resistance	Input at chip's common mode voltage	15	20	30	kΩ
VDTH	Receive data detection threshold	Relative to peak amplitude for 25.92 MHz sinusoidal input		50		%
VLOW	Receive data low signal threshold	Relative to peak amplitude for 25.92 MHz sinusoidal input		±55		mV
VLOWT	Receive data low signal delay	Relative to peak amplitude for 22.37 MHz sinusoidal input		1.5		μs
TRCF	Receive clock period			19.29		ns
TRC	Receive clock pulse width			10.99		ns
TRCPT	Receive clock positive transition time	C _L = 15 pF		4.5	6	ns
TRCNT	Receive clock negative transition time	C _L = 15 pF		4.5	6	ns

RECEIVER (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT	
TRDP TRDN	Positive or negative receive data pulse width		19.29		ns	
TRDPS TRDNS	Receive data set-up time	5	9.65	11.82	ns	
TRDPH TRDNH	Receive data hold time	5	9.65	11.82	ns	
	Receive input jitter tolerance high frequency	sine, 60 kHz	±2.89		ns	
		to 300 kHz	0.3		UIPP	
	Receive input jitter tolerance low frequency	sine, 10 Hz to 2.3 kHz	±48.22		ns	
			5.0		UIPP	
KD	Clock Recovery Phase Detector Gain	All 1's data pattern KD = .418/RFO	83	92	101	µA/Rad
KO	Clock Recovery Phase Locked Oscillator Gain		12	14.5	17	Mrad/ sec. -Volt

TRANSMITTER

All of the measurements for the transmitter are made with the following conditions unless otherwise stated:

1. Transmit pulse characteristics are obtained using a line transformer which has the characteristics TBD.
2. The circuit is connected as in Figure 1.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TTCF	Transmit clock repetition period		19.29		ns
TTC	Transmit clock pulse width	8.20	9.65	11.09	ns
TTCNT	Transmit clock negative transition time		4.5	6	ns
TTCPT	Transmit clock positive transition time		4.5	6	ns
TTPDS TTNDS	Transmit data set-up time	3.5	9.65		ns
TTPDH TTNDH	Transmit data hold time	3.5	9.65		ns
TTPL	Transmit positive line pulse width	Measured at transformer, LBO = Low	9.65		ns

TRANSMITTER (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TTNL	Transmit negative line pulse width		9.65		ns
	Transmit line pulse waveshape				

Note: The pulse template fits a scaled DSX-3 pulse template.

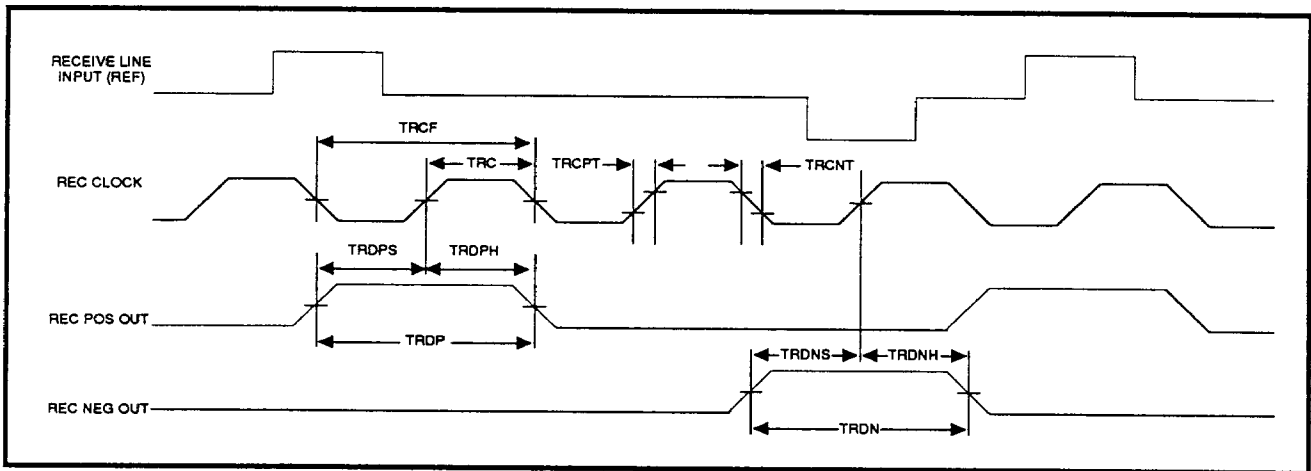


FIGURE 2: Receive Waveforms

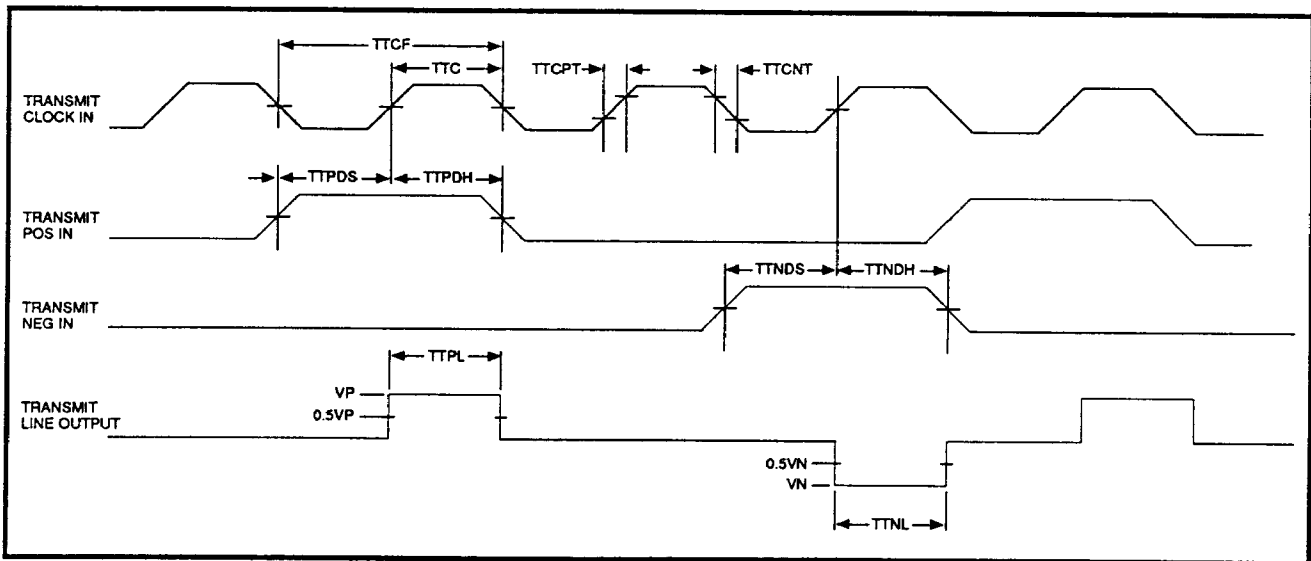
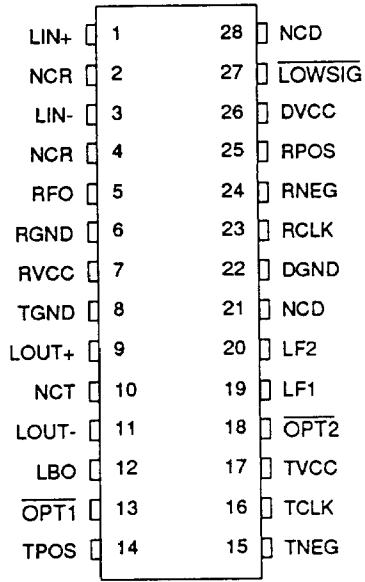


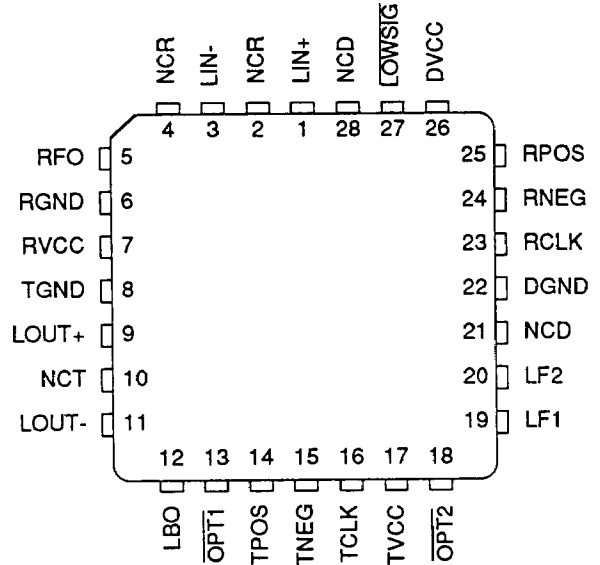
FIGURE 3: Transmit Waveforms

PACKAGE PIN DESIGNATIONS

(Top View)



28-Pin DIP



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
LXT2361, STS-1 Line Interface – 28-pin		
Standard Width Plastic DIP (600 mil)	LXT2361NE	LXT2361NE
Surface Mount 28-pin PLCC	LXT2361PE	LXT2361PE

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