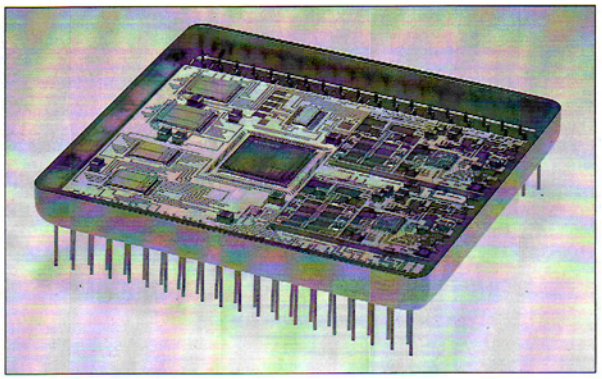
MIL-STD-1553B
INTEGRATED DATABUS MODULE (MIL - LINK) IDM1553

ABRIDGED VERSION - PLEASE REFER TO SEPARATE DATA SHEET FOR FULL INFORMATION

The C-MAC IDM 1553 (MIL-LINK) Integrated Databus Module is a complete MIL-STD 1553B or STANAG 3838 interface, capable of operation in Bus Controller (BC), Remote Terminal (RT) and Bus Monitor (BM) modes, see block diagram fig. 1



- BUS CONTROLLER/REMOTE TERMINAL/BUS MONITOR CAPABILITIES
- LOW POWER +5V ONLY TRANSCEIVERS
- INTERNAL MICROPROCESSOR WITH DEDICATED INSTRUCTION SET
- 8K X 16 SHARED RAM
- PROGRAMMABLE INTERRUPT SELECTION
- MESSAGE TIME TAGGING
- COMPLETE MESSAGE HANDLING PROTOCOL IS FIRMWARE DEPENDENT IN INTERNAL PROM
- INTERFACES TO ALL STANDARD CPUS
- POWERFUL SELFTEST
- DIP OR FLATPACK HYBRID

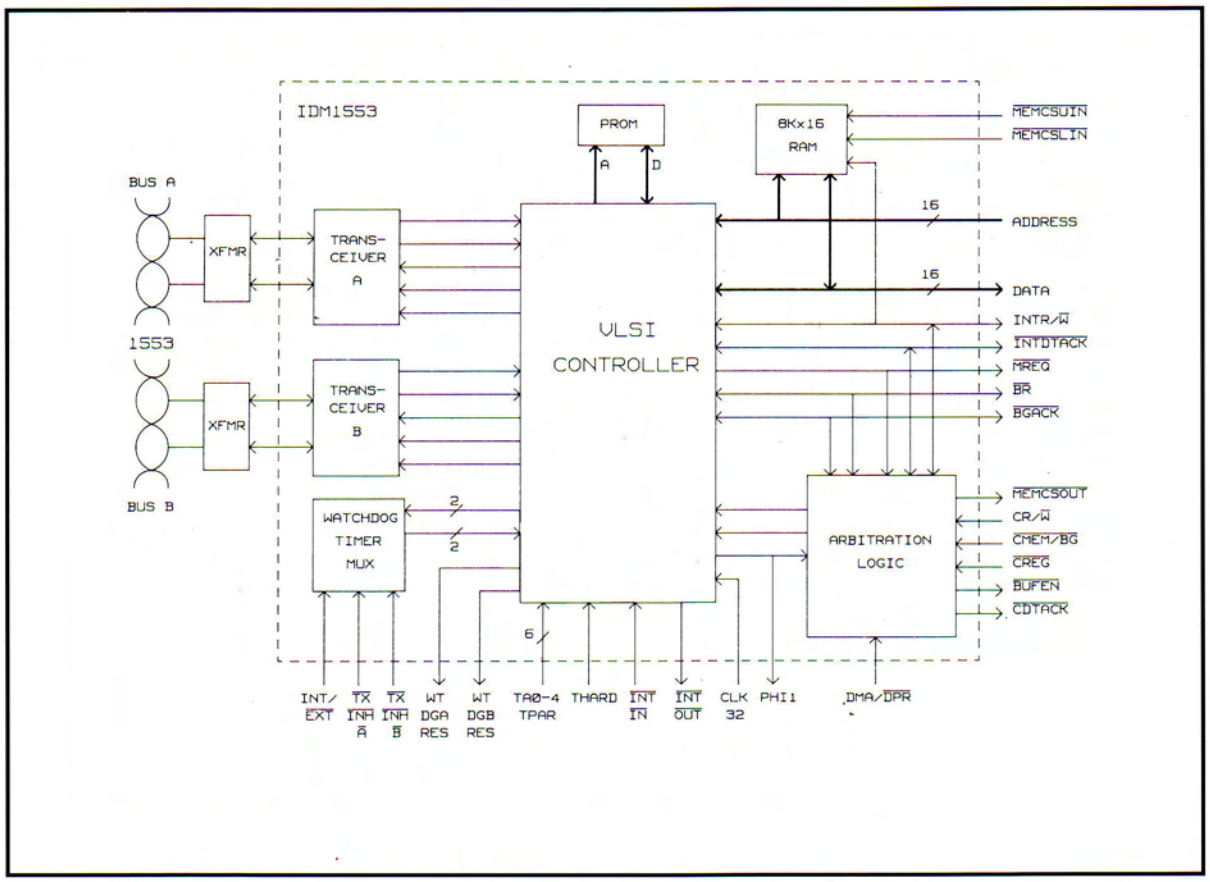


Fig. 1 Block Diagram of IDM1553 (MIL - LINK) Hybrid

Packaged in a 78 pin DIP or 82 pin flatpack package the IDM1553 contains two low power +5V only transceivers, complete BC/RT/BM protocol logic in a single custom chip, a PROM containing firmware defining the structure of the control and data areas to be set up in memory, arbitration logic and 8K X 16 RAM which can be byte addressed and is expandable externally to 64K X 16.

The custom chip within the hybrid also includes a microprocessor with its own dedicated instruction set for use in BC mode. This enables the IDM1553 to operate autonomously, scheduling and linking message lists with minimum host CPU overhead.

All 1553 operations are controlled by CPU access to the shared RAM and the interface can be configured in pseudo-dual port or DMA modes.

The IDM1553 operates over the full military -55°C to +125°C temperature range and is available screened to MIL-STD-883.

CPU INTERFACE

The CPU interface mode is selectable for pseudo-dual port or DMA modes of operation using a discrete pin DMA/$\overline{\text{DPR}}$. With a pseudo dual port interface the address and data lines of the IDM1553 module are isolated from those of the host CPU by external buffers. Arbitration logic within the hybrid decides which access has to be served first when both internal controller and host CPU attempt to access the RAM at the same time and controls the buffers accordingly. In this mode of operation, internal or external RAM or a combination of both up to a maximum size of 64K X 16 can be used as shown in figs. 2, 3 and 4. The internal RAMs can be accessed independently using separate chip select lines allowing easy interfacing with an 8 bit bus.

The CPU is also able to access the registers of the IDM1553 using the $\overline{\text{CREG}}$ line and address lines A0 and A1. Handshaking to the CPU is provided by the single $\overline{\text{CDTACK}}$ line indicating when a transfer is complete.

In the DMA mode of operation the internal arbiter is disabled and the IDM1553 address, data and control lines are connected directly to those of the host CPU as shown in fig. 5. Access to the host's system bus is obtained using the industry standard handshake lines, Bus Request, Bus Grant and Bus Grant Acknowledge. Internal memory would usually be disabled (unless it was to form part of the host's system memory) by connecting the memory chip select lines ($\overline{\text{MEMCSUIN}}$ and $\overline{\text{MEMCSLIN}}$) to a logic high.

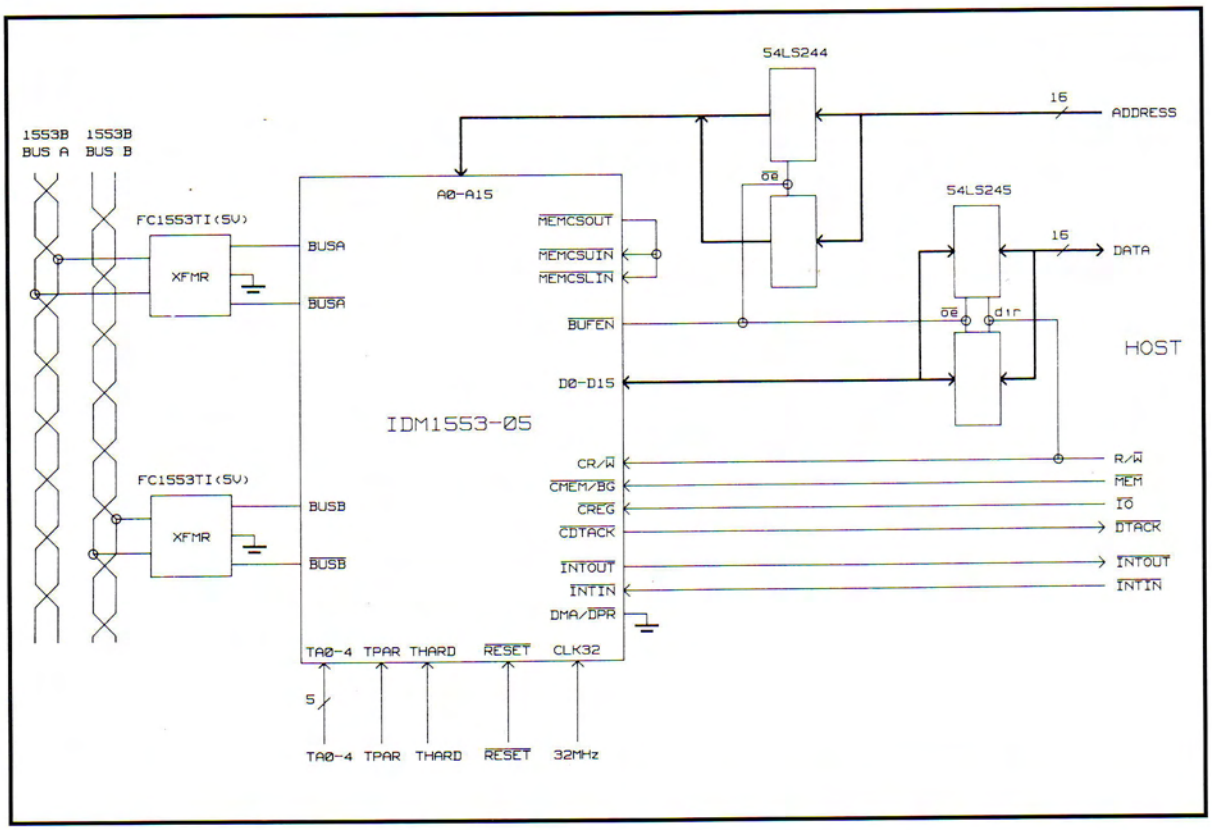


Fig. 2 Typical IDM1553 Pseudo Dual Port Mode configuration using Internal Memory only

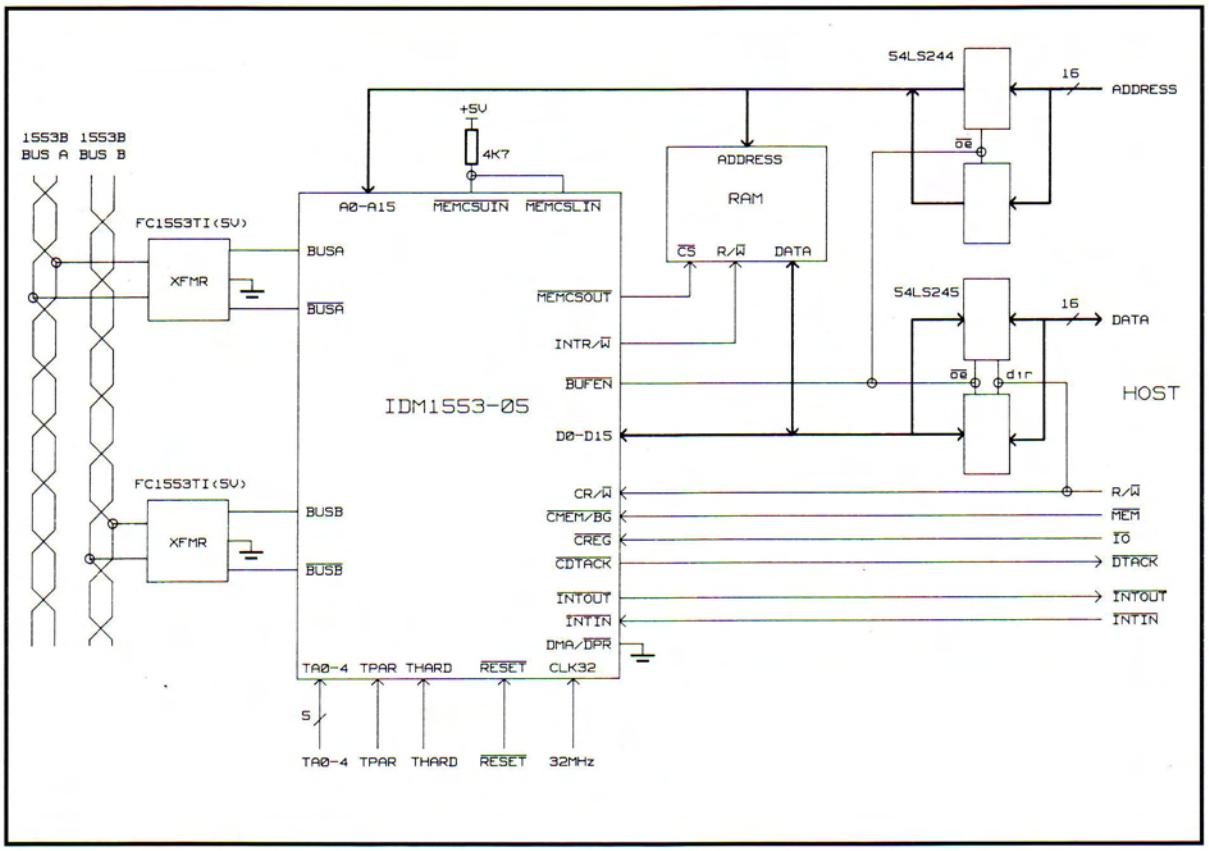


Fig. 3 Typical IDM1553 Pseudo Dual Port Mode configuration using External Memory only

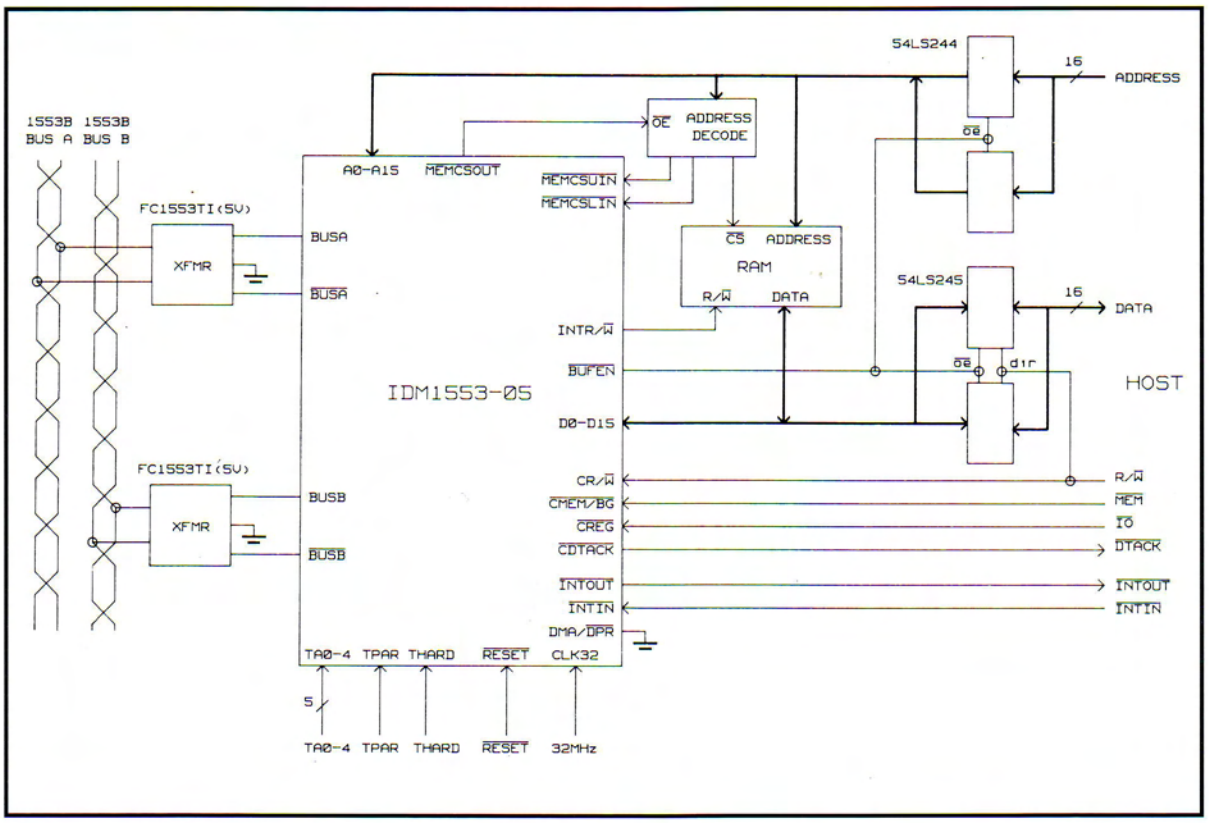


Fig. 4 Typical IDM1553 Pseudo Dual Port Mode configuration using both Internal and External Memory

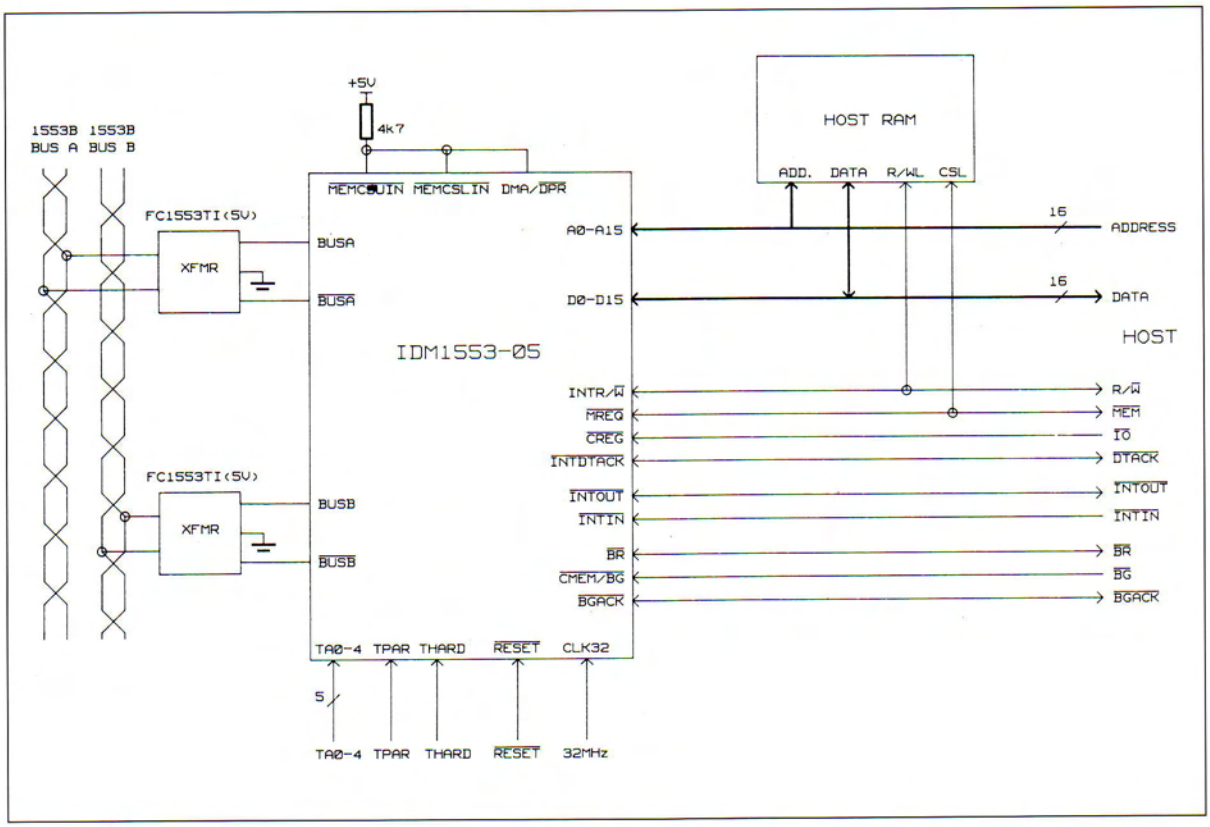


Fig. 5 Typical IDM1553 DMA Mode configuration

MIL-STD-1553B BUS INTERFACE

The IDM1553 provides dual complementary bus lines for connecting directly to a transformer. Either the internal or external watchdog timers can be selected using the INT/EXT line. If external watchdog timers are used the watchdog reset outputs, WTDGARES and WTDGBRES can be used to trigger monostables. Each monostable output should drive the corresponding transmitter inhibit line, TXINHA or TXINHB, high for a period of 680 - 800 µs to enable transmission on the 1553 bus. An example of external watchdog timer connection is shown in fig.6.

The input TXOFF will disable both transmitters if strobed once. This function can be used to inhibit transmissions on the 1553 bus if the host processor's watchdog timer expires.

IDM1553 REGISTERS

In addition to the control and data areas which are implemented in RAM there is also a set of registers which can be accessed from the host CPU using the CREG line and address lines A0 and A1.The definition of these registers changes with the mode of operation.

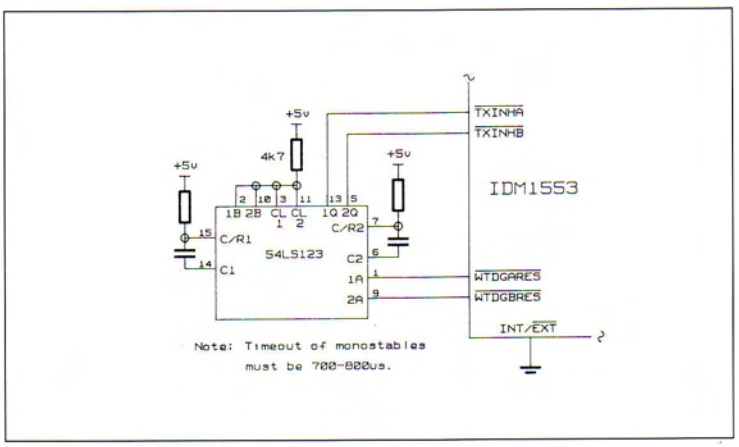


Fig. 6 Example Connection of Optional External Fail-safe Timer

CONTROL BLOCK

The IDM1553 Control Block has a fixed length of 32 words and begins at the address held in the Control Block Pointer at location 0000 in RAM. The Control Block is responsible for overall control of the module and its definition varies according to the mode of operation. The contents of the Control Block are only interrogated by the internal controller during initialisation and altering such information during operation does not affect the current operational mode. An overview of the Control Block's functions is given below.

General

Operational Mode, BC, RT or BM.
Selftest execution.
Time Tag counter update rate.
Global error and status reporting.

RT mode

RT Address (if external THARD pin is at a logic low level).
Addressing of RT Descriptor block.
Mode code illegalisation.
Global interrupt enabling.
Mode code data storage.
Pointers to start and end of monitor stack (if BM mode enabled).

BC mode

Addressing of BC Descriptor tables.
Last message table instruction address.
Acyclic event control.

REMOTE TERMINAL OPERATION

Remote Terminal message handling is based on descriptors. Three descriptors are associated with each subaddress (one for transmit, one for receive and one for broadcast messages). The descriptors reside in memory and are listed sequentially according to subaddress. Each descriptor controls the action carried out by the IDM1553 in response to a message with that subaddress and T/R bit combination. It also reports on the validity of the received message and directs associated data to or from one of two data buffers which can have a maximum size of 32 words. A time tag word is also recorded with each received message. Toggling of the data pointers to the two buffers is controlled by the IDM1553 for receive messages and by the host for transmit messages.

BUS CONTROLLER OPERATION

In BC mode the IDM1553 off-loads the CPU of all routine data transfers involved with 1553B message transfers by providing a wide range of user programmable functions. The Bus Controller architecture consists of a Control Block, one or more message lists, Transfer and Mode code Descriptor Blocks and the Data Buffers all residing in memory. The message list is constructed from a consecutive sequence of Bus Controller instructions beginning at an address contained in the Program Pointer, address 0001 (hex).

BUS MONITOR OPERATION

Bus Monitor mode is an extension of Remote Terminal mode and allows the IDM1553 to act solely as a Bus Monitor, capturing all 1553 bus traffic, or as a combined RT/BM where it acts as a normal Remote Terminal to its own address as well as capturing all other 1553 bus traffic. Monitor mode is enabled by setting the MON bit to 1 in the Interface Control Word of the RT Control Block. Setting the RT address bits (either hardware or software) to all ones will result in the IDM1553 implementing the monitor function only and not responding to any commands.

SELFTEST

The IDM1553 implements a set of internal test procedures, any of which can be enabled by the host CPU. While executing the tests the IDM1553 will not operate as a BC, RT or BM.

Table 1 ABSOLUTE MAXIMUM RATINGS

Supply voltage range	
(+5V) V_{CCA} V_{CCB} V_{CCC}	0.3 to 7Vdc
(-15V) V_{SNA} V_{SNB} (IDM1553 -15 only)	0.3 to -18Vdc
Receiver Differential Voltage	40V pk-pk
Operating Case Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering 10 sec)	+265°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 2 RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	MAX	UNIT
Supply Voltage				
(+5V) V_{CCA} V_{CCB} V_{CCC}		4.5	5.5	Vdc
(-15V) V_{SNA} V_{SNB}		-14.25	-15.75	Vdc
Low Level Output Current				
$\overline{\text{MEMCSOUT}}$, $\overline{\text{BUFEN}}$, $\overline{\text{CDTACK}}$	I_{OL1}		10	mA
All other outputs	I_{OL2}		4	mA
High Level Output Current	I_{OH}		-2	mA

Table 3 POWER SUPPLY CURRENTS

PARAMETER			TYPICAL	MAX	UNIT
IDM1553-05 SERIES					
Total V_{CC}		Standby	235	460	mA
	*	25% Duty Cycle	335	580	mA
	*	100% Duty Cycle	635	940	mA
IDM1553-15 SERIES					
Total V_{CC}		Standby	240	450	mA
	*	25% Duty Cycle	250	470	mA
	*	100% Duty Cycle	280	510	mA
Total V_{SN}		Standby	10	15	mA
	*	25% Duty Cycle	45	65	mA
	*	100% Duty Cycle	175	220	mA

* NOTE: - Supply currents include one channel transmitting with the second channel in standby mode.

Table 3 DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
LOGIC					
High Level Output Voltage	V_{OH}	V_{CC} = min, I_{OH} = -2mA	2.4		V
Low Level Output Voltage	V_{OL1}	V_{CC} = min, I_{OL1} = 10mA ($\overline{\text{MEMCSOUT}}$, $\overline{\text{BUFEN}}$, $\overline{\text{CDTACK}}$)		0.4	V
Low Level Output Voltage	V_{OL2}	V_{CC} = min, I_{OL2} = 4mA (All other outputs)		0.4	V
High Level Input Voltage	V_{IH1}	Guaranteed input high for CLK32 and $\overline{\text{RESET}}$ inputs	3.1		V
High Level Input Voltage	V_{IH2}	Guaranteed input high for all other logic I/P's (not BUSA, $\overline{\text{BUSA}}$, BUSB, $\overline{\text{BUSB}}$)	2.2		V
Low Level Input Voltage	V_{IL}	Guaranteed input low for all logic I/P's (not BUSA, $\overline{\text{BUSA}}$, BUSB, $\overline{\text{BUSB}}$)		0.7	V
High Level Input Current	I_{IH1}	V_{IH} ≥2.2V (TXOFF, TAO-4, TPAR, THARD, SLOW inputs with internal pull down resistor)		200	µA
Low Level Input Current	I_{IL1}	V_{IL} ≤0.7V (TXOFF, TAO-4, TPAR, THARD, SLOW inputs with internal pull down resistor)	-10		µA
High Level Input Current	I_{IH2}	V_{IH} ≥2.2V (address lines A0-A15)	-30	+30	µA
Low Level Input Current	I_{IL2}	V_{IL}≤0.7V (address lines A0-A15)	-30	+30	µA
High Level Input Current	I_{IH3}	V_{IH} ≥2.2V (data lines D0-D15)	-20	+20	µA
Low Level Input Current	I_{IL3}	V_{IL} ≤0.7V (data lines D0-D15)	-20	+20	µA
High Level Input Current	I_{IH4}	V_{IH} ≥2.2V (DMA/$\overline{\text{DPR}}$, CR/$\overline{\text{W}}$ inputs)	-10	+20	µA
Low Level Input Current	I_{IL4}	V_{IL} ≤0.7V (DMA/$\overline{\text{DPR}}$, CR/$\overline{\text{W}}$ inputs)	-10	+20	µA
High Level Input Current	I_{IH5}	V_{IH} ≥2.2V ($\overline{\text{MEMCSUIN}}$, $\overline{\text{MEMCSLIN}}$ inputs)	-10	+10	µA
Low Level Input Current	I_{IL5}	V_{IL} ≤0.7V ($\overline{\text{MEMCSUIN}}$, $\overline{\text{MEMCSLIN}}$ inputs)	-10	+10	µA
High Level Input Current	I_{IH6}	V_{IH} ≥3.1V (CLK32, $\overline{\text{RESET}}$ inputs)	-20	+20	µA
Low Level Input Current	I_{IL6}	V_{IL} ≤0.7V (CLK32, RESET inputs)	-20	+20	µA
High Level Input Current	I_{IH7}	V_{IH} =2.7V ($\overline{\text{TXINHA}}$, $\overline{\text{TXINHB}}$, $\overline{\text{CMEM/BG}}$, $\overline{\text{CREG}}$, $\overline{\text{INTIN}}$ inputs)		20	µA
Low Level Input Current	I_{IL7}	V_{IL} =0.4V ($\overline{\text{TXINHA}}$, $\overline{\text{TXINHB}}$, $\overline{\text{CMEM/BG}}$, $\overline{\text{CREG}}$, $\overline{\text{INTIN}}$ inputs)	-0.4		mA
High Level Input Current	I_{IH8}	V_{IH} =2.7V (INT/$\overline{\text{EXT}}$, $\overline{\text{INTDTACK}}$, $\overline{\text{MREQ}}$, INTR/$\overline{\text{W}}$, $\overline{\text{BR}}$, $\overline{\text{BGACK}}$, inputs with internal pull up resistor)		40	µA
Low Level Input Current	I_{IL8}	V_{IL} =0.4V (INT/$\overline{\text{EXT}}$, $\overline{\text{INTDTACK}}$, $\overline{\text{MREQ}}$, INTR/$\overline{\text{W}}$, $\overline{\text{BR}}$, $\overline{\text{BGACK}}$ inputs with internal pull up resistor)	-0.8		mA
Output Load Capacitance	C_{OUT}	Frequency = 1MHz at 0V		50	pF
Input Load Capacitance	C_{IN}	Frequency = 1MHz at 0V		10	pF
Input Clock Frequency Tolerance		Nominal frequency = 32MHz		100	ppm
Clock High & Low Time			12.5		ns
Clock Rise & Fall Time				5	ns
RECEIVER					
Differential Output				40	Vp-p
Differential Input Impedance				4	Kohm
Common Mode Rejection Ratio			40		dB
Threshold Voltage			0.6	0.82	Vp-p
TRANSMITTER					
Differential O/P Voltage		Transformer coupled	18	27	Vp-p
Differential O/P Voltage		Direct coupled	6	9	Vp-p
Output Rise & Fall Time			100	300	ns

Table 5 IDM1553 - XX - XD PIN-OUT (DUAL-IN-LINE PACKAGE)

PIN	NAME	TYPE	FUNCTIONAL DESCRIPTION
1	D0	I/O	DATA BUS BIT 0
2	D2	I/O	DATA BUS BIT 2
3	D4	I/O	DATA BUS BIT 4
4	D6	I/O	DATA BUS BIT 6
5	D8	I/O	DATA BUS BIT 8
6	D10	I/O	DATA BUS BIT 10
7	D12	I/O	DATA BUS BIT 12
8	D14	I/O	DATA BUS BIT 14
9	TA1	I	TERMINAL ADDRESS BIT 1
10	TA0	I	TERMINAL ADDRESS BIT 0
11	TA4	I	TERMINAL ADDRESS BIT 4
12	THARD	I	HARDWIRED TERMINAL ADDRESS SELECT IF HIGH
13	WTDGBRES	O	EXTERNAL WATCHDOG TIMER RESET ON BUS B
14	V_{CCC}		+5V SUPPLY FOR DIGITAL LOGIC CIRCUITRY
15	$\overline{BR}$	I/O	BUS REQUEST. USED FOR DMA OPERATION
16	$\overline{BGACK}$	I/O	BUS GRANT ACKNOWLEDGE. USED IN DMA MODE
17	PHI1	O	8MHz CLOCK OUT - PHASE 1
18	V_{SNB}		RESERVED FOR -15V TO BUS B TRANSCEIVER
19	GND B		GROUND TO BUS B TRANSCEIVER
20	BUS B		TRANSCEIVER B BUS SIGNAL (TRUE) TO THE TRANSFORMER ON 1553 CHANNEL B
21	LOGIC GND		GROUND FOR THE DIGITAL LOGIC CIRCUITRY
22	A1	I/O	ADDRESS BIT 1
23	A3	I/O	ADDRESS BIT 3
24	A5	I/O	ADDRESS BIT 5
25	A7	I/O	ADDRESS BIT 7
26	A9	I/O	ADDRESS BIT 9
27	A11	I/O	ADDRESS BIT 11
28	A13	O	ADDRESS BIT 13
29	A15	O	ADDRESS BIT 15
30	DMA/$\overline{DPR}$	I	DMA OR DUAL CONFIGURATION SELECT. HIGH - DMA MODE, LOW - DUAL PORT MODE
31	$\overline{MEMCSOUT}$	O	MEMORY CHIP SELECT OUT. MAY BE CONNECTED TO $\overline{MEMCSUIN}$ AND $\overline{MEMCSLIN}$ OR TO EXTERNAL MEMORY
32	CLK32	I	32 MHz CLOCK INPUT
33	$\overline{CREG}$	I	INTERNAL REGISTER SELECT LINE FROM CPU
34	SLOW	I	SLOW CLOCK. WHEN HIGH A 16MHz CLOCK CAN BE USED BUT MEMORY ACCESS TIME IS INCREASED. (C-MAC TEST PIN ONLY)
35	$\overline{TXINHA}$	I	TRANSMITTER INHIBIT A FROM EXTERNAL WATCHDOG TIMER
36	CR/$\overline{W}$	I	READ/WRITE LINE FROM CPU (DUAL PORT MODE). HIGH - READ, LOW - WRITE
37	WTDGARES	O	EXTERNAL WATCHDOG TIMER RESET ON BUS A
38	GND A		GROUND TO BUS A TRANSCEIVER
39	V_{SNA}		RESERVED FOR -15V TO BUS A TRANSCEIVER

Table continued overleaf

Table 5 (Continued) **IDM1553 - XX - XD PIN-OUT (DUAL-IN-LINE PACKAGE)**

PIN	NAME	TYPE	FUNCTIONAL DESCRIPTION
40	BUSA		TRANSCEIVER A BUS SIGNAL (TRUE) TO THE TRANSFORMER ON 1553 CHANNEL A
41	D1	I/O	DATA BUS BIT 1
42	D3	I/O	DATA BUS BIT 3
43	D5	I/O	DATA BUS BIT 5
44	D7	I/O	DATA BUS BIT 7
45	D9	I/O	DATA BUS BIT 9
46	D11	I/O	DATA BUS BIT 11
47	D13	I/O	DATA BUS BIT 13
48	D15	I/O	DATA BUS BIT 15
49	TA3	I	TERMINAL ADDRESS BIT 3
50	TA2	I	TERMINAL ADDRESS BIT 2
51	TPAR	I	TERMINAL ADDRESS PARITY BIT
52	PHI2	O	8 MHz CLOCK OUT - PHASE 2
53	$\overline{\text{TXINHB}}$	I	TRANSMITTER INHIBIT B FROM EXTERNAL WATCHDOG TIMER
54	TXOFF	I	TURNS BOTH TRANSMITTERS OFF WHEN PULSED HIGH
55	$\overline{\text{INTDTACK}}$	I/O	DATA ACKNOWLEDGE TO/FROM CPU (DMA MODE) (NOTE - IN DUAL PORT MODE THIS SIGNAL IS AN O/P)
56	$\overline{\text{MREQ}}$	I/O	MEMORY REQUEST. USED IN DMA MODE
57	INT/$\overline{\text{EXT}}$	I	INTERNAL/EXTERNAL WATCHDOG TIMER SELECT
58	V_{CCB}		+5V SUPPLY TO TRANSCEIVER B
59	$\overline{\text{BUS B}}$		TRANSCEIVER B BUS SIGNAL (INVERTED) TO THE TRANSFORMER ON 1553 CHANNEL B
60	A0	I/O	ADDRESS BIT 0
61	A2	I/O	ADDRESS BIT 2
62	A4	I/O	ADDRESS BIT 4
63	A6	I/O	ADDRESS BIT 6
64	A8	I/O	ADDRESS BIT 8
65	A10	I/O	ADDRESS BIT 10
66	A12	I/O	ADDRESS BIT 12
67	A14	O	ADDRESS BIT 14
68	INTR/$\overline{\text{W}}$	I/O	READ/WRITE LINE TO/FROM CPU (DMA MODE)
69	$\overline{\text{MEMCSUIN}}$	I	UPPER MEMORY CHIP SELECT IN. MAY BE CONNECTED TO $\overline{\text{MEMCSOUT}}$ TO USE INTERNAL MEMORY (D.P. MODE)
70	$\overline{\text{MEMCSLIN}}$	I	LOWER MEMORY CHIP SELECT IN. MAY BE CONNECTED TO $\overline{\text{MEMCSOUT}}$ TO USE INTERNAL MEMORY (D.P. MODE)
71	$\overline{\text{RESET}}$	I	POWER ON RESET SIGNAL FROM CPU
72	$\overline{\text{INTOUT}}$	O	INTERRUPT OUTPUT - 500ns LOW PULSE
73	$\overline{\text{BUFEN}}$	O	EXTERNAL BUFFER ENABLE SIGNAL (D.P. MODE)
74	$\overline{\text{CMEM}}$/BG	I	D.P. MODE - INTERNAL MEMORY SELECT FROM CPU DMA MODE - BUS GRANT FROM CPU
75	$\overline{\text{CDTACK}}$	O	DATA ACKNOWLEDGE FROM ARBITER (D.P. MODE)
76	$\overline{\text{INTIN}}$	I	INTERRUPT INPUT - PULSE TRIGGERED
77	V_{CCA}		+5V SUPPLY TO TRANSCEIVER A
78	$\overline{\text{BUS A}}$		TRANSCEIVER A BUS SIGNAL (INVERTED) TO THE TRANSFORMER ON 1553 CHANNEL A

Table 6 IDM1553 - XX - XFP PIN-OUT (FLAT PACK)

PIN	NAME	PIN	NAME
1	NC	42	NC
2	D0	43	BUS A
3	D1	44	$\overline{\text{BUS A}}$
4	D2	45	V_{SNA}
5	D3	46	V_{CCA}
6	D4	47	GNDA
7	D5	48	$\overline{\text{INTIN}}$
8	D6	49	WTDGARES
9	D7	50	$\overline{\text{CDTACK}}$
10	D8	51	CR/$\overline{\text{W}}$
11	D9	52	$\overline{\text{CMEM/BG}}$
12	D10	53	$\overline{\text{TXINHA}}$
13	D11	54	$\overline{\text{BUFEN}}$
14	D12	55	SLOW
15	D13	56	$\overline{\text{INTOUT}}$
16	D14	57	$\overline{\text{CREG}}$
17	D15	58	$\overline{\text{RESET}}$
18	TA1	59	CLK32
19	TA3	60	$\overline{\text{MEMCSLIN}}$
20	TA0	61	$\overline{\text{MEMCSOUT}}$
21	TA2	62	MEMCSUIN
22	TA4	63	DMA/$\overline{\text{DPR}}$
23	TPAR	64	INTR/$\overline{\text{W}}$
24	THARD	65	A15
25	PHI2	66	A14
26	WTDGBRES	67	A13
27	$\overline{\text{TXINHB}}$	68	A12
28	V_{CCC}	69	A11
29	TXOFF	70	A10
30	$\overline{\text{BR}}$	71	A9
31	$\overline{\text{INTDTACK}}$	72	A8
32	$\overline{\text{BGACK}}$	73	A7
33	$\overline{\text{MREQ}}$	74	A6
34	PHI1	75	A5
35	INT/$\overline{\text{EXT}}$	76	A4
36	V_{SNB}	77	A3
37	V_{CCB}	78	A2
38	GND B	79	A1
39	$\overline{\text{BUS B}}$	80	A0
40	BUS B	81	LOGIC GND
41	NC	82	NC

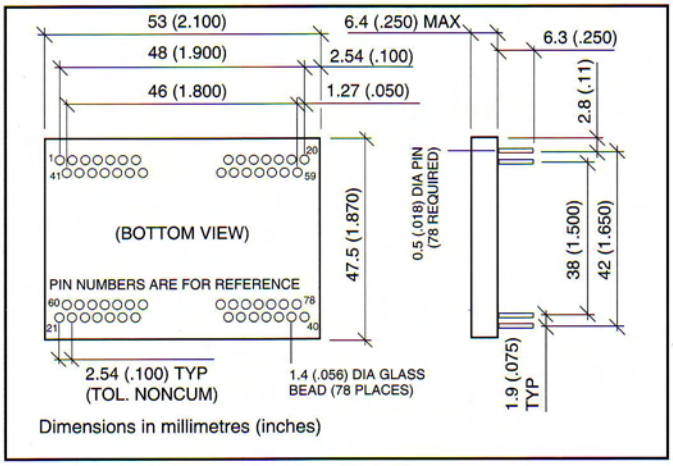


Fig. 7 Mechanical Outline (DDIP)

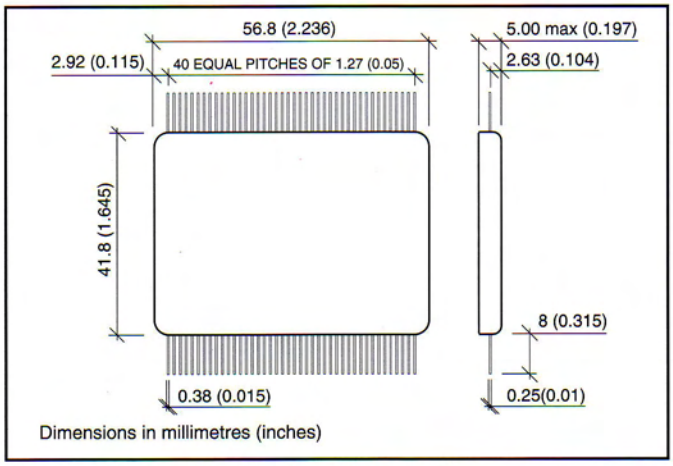


Fig. 8 Mechanical Outline (Flatpack)

ORDERING INFORMATION

IDM1553 – X X – X X

- Case style
  - D = DIL
  - FP = Flat Pack
- PROM firmware revision
  - 1 = Standard
- TRANSCEIVER Voltage type
  - 05 – +5v only
  - 15 – +5v and –15v

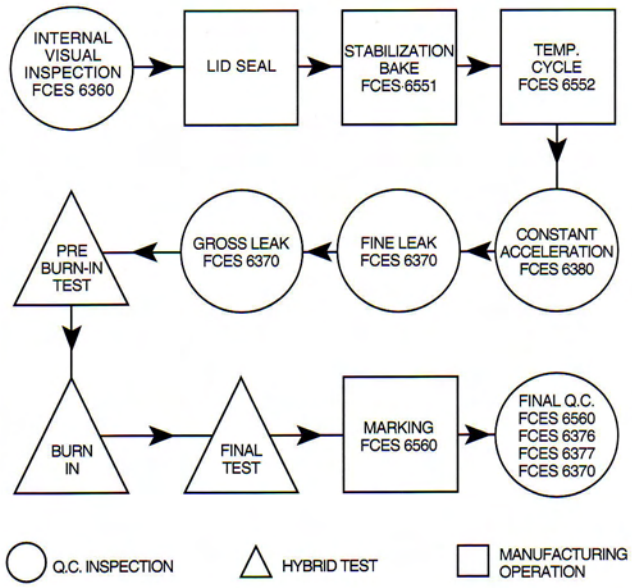
Fig. 9 Ordering Information

The product assurance programme defines manufacturing procedures, establishes quality standards, in line inspection controls and 100% screening tests.

The standard 100% screening performed prior to product shipment is shown in the flow chart.

Manufactured in accordance with procedures laid down within MIL-STD-883 and BS9450 (CECC 63000).

100 per cent Screening



Title	Factory Procedure	BS 9450 Requirement	MIL-STD-883 Requirement
Internal Visual	FCES6360	1.2.10	2017
Lid Seal	Welded	1.2.6.14	none
Stabilization Bake	FCES 6551	1.2.6.3.4	1008
Temperature Cycling	FCES 6552	1.2.6.13	1010
Constant Acceleration	FCES 6380	1.2.6.9	2001
Fine Leak	FCES 6370	1.2.6.14.1	1014
Gross Leak	FCES 6370	1.2.6.14.2	1014
Burn In	FCES 6390	1.2.9.2	1015
Final QC	FCES 6560	1.2.2	2009
	FCES 6376		
	FCES 6377		
	FCES 6370		

Fig. 10 Quality Conformance

C-MAC Microcircuits Limited,
South Denes, Great Yarmouth,
Norfolk, NR30 3PX England
Telephone: +44 (0) 1493 743100
Fax: 44 (0) 1493 858536