55325•75325
MEMORY DRIVER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION—The 55325 and 75325 are Memory Drivers for use in magnetic memories constructed on a silicon chip using the Fairchild Planar* process. The device contains four 600 mA switches, two source switches and two sink switches that can be selected by the appropriate logic input and appropriate strobe. The device has adequate base drive to source currents up to 375 mA with V_{CC2} of 15 V or 600 mA with V_{CC2} voltage of 24 V. In applications requiring drive to source currents greater than 375 mA, an external resistor may be used to regulate the source base current to within ±5% and reduce the power dissipation to allow higher source currents at higher ambient temperatures.

Internal voltage surge protection of each of the output sink transistors is provided for switching inductive loads.

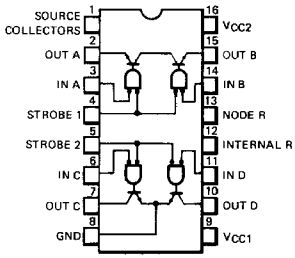
- **600 mA OUTPUT CAPABILITY**
- **FAST SWITCH TIMES**
- **OUTPUT SHORT- CIRCUIT CURRENT**
- **DUAL SINK AND DUAL SOURCE OUTPUTS**
- **MINIMUM TIME SKEW BETWEEN ADDRESS AND OUTPUT CURRENT RISE**
- **24 V CAPABILITY**
- **TTL OR DTL COMPATIBLE**
- **SOURCE BASE DRIVE EXTERNALLY ADJUSTABLE**
- **INPUT CLAMP DIODES**

POSITIVE LOGIC TRUTH TABLE

ADDRESS INPUTS				STROBE INPUTS		OUTPUTS (Note 3)			
SOURCE		SINK		SOURCE	SINK	SOURCE		SINK	
IN A	IN B	IN C	IN D	S1	S2	A	B	C	D
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = HIGH Level, L = LOW Level, X = Don't Care

CONNECTION DIAGRAMS
16-PIN
(TOP VIEW)
PACKAGE OUTLINES 7B 9B 4L
PACKAGE CODES D P F

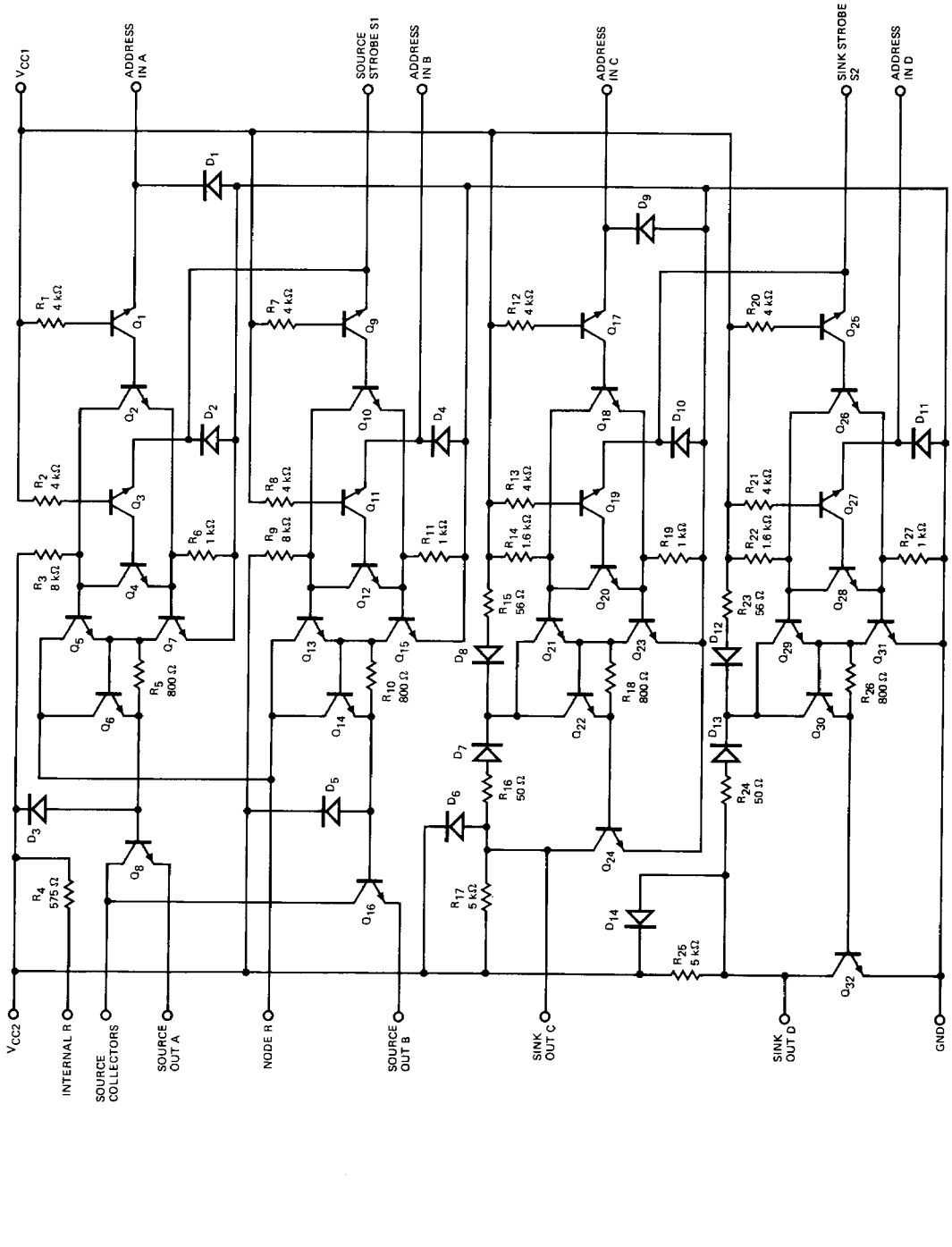


ORDER INFORMATION

TYPE	PART NO.
55325	55325DM
75325	75325DC
55325	55325FM
75325	75325PC

*Planar is a patented Fairchild process.

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC1} (Note 1)	+7.0 V
Supply Voltage V_{CC2} (Note 1)	+25 V
Input Voltage (Any Address or Strobe Input)	+5.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
55325	−55°C to +125°C
75325	0°C to +70°C
Internal Power Dissipation (Note 2)	1 W
Pin Temperature	
Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

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ELECTRICAL CHARACTERISTICS: Ratings apply for $-55°C \leq T_A \leq 125°C$, unless otherwise specified.

SYMBOL	CHARACTERISTICS		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Input HIGH Voltage		Fig. 1 & 2		2.0			V
V_{IL}	Input LOW Voltage		Fig. 3 & 4				0.8	V
V_{CD}	Input Clamp Diode Voltage		V_{CC1} = 4.5 V, V_{CC2} = 24 V I_{IN} = −10 mA, T_A = 25°C Fig. 5			−1.3	−1.7	V
I_{OFF}	Source-collectors Terminal Off-State Current		V_{CC1} = 4.5 V, V_{CC2} = 24 V Fig. 1	Full Range			500	μA
				T_A = 25°C		3.0	150	
V_{OH}	Sink Output HIGH Voltage		V_{CC1} = 4.5 V, V_{CC2} = 24 V I_{OUT} = 0, Fig. 2		19	23		V
V_{SAT}	Saturation Voltage	Source Outputs	V_{CC1} = 4.5 V, V_{CC2} = 15 V R_L = 24 Ω, $I_{source} \approx$ −600 mA See Notes 3 & 4, and Fig. 3	Full Range			0.9	V
				T_A = 25°C		0.43	0.7	
		Sink Outputs	V_{CC1} = 4.5 V, V_{CC2} = 15 V R_L = 24 Ω, $I_{sink} \approx$ 600 mA See Notes 3 & 4 and Fig. 4	Full Range			0.9	V
				T_A = 25°C		0.43	0.7	
I_{IN}	Input Current at Maximum Input Voltage	Address Inputs	V_{CC1} = 5.5 V, V_{CC2} = 24 V V_{IN} = 5.5 V, Fig. 5				1.0	mA
		Strobe Inputs					2.0	
I_{IH}	Input HIGH Current	Address Inputs	V_{CC1} = 5.5 V, V_{CC2} = 24 V V_{IN} = 2.4 V, Fig. 5			3.0	40	μA
		Strobe Inputs				6.0	80	
I_{IL}	Input LOW Current	Address Inputs	V_{CC1} = 5.5 V, V_{CC2} = 24 V V_{IN} = 0.4 V, Fig. 5			−1.0	−1.6	mA
		Strobe Inputs				−2.0	−3.2	
$I_{CC(off)}$	Supply Current, All Sources and Sinks Off	From V_{CC1}	V_{CC1} = 5.5 V, V_{CC2} = 24 V T_A = 25°C, Fig. 6			14	22	mA
		From V_{CC2}				7.5	20	
I_{CC1}	Supply Current from V_{CC1}, Either Sink On		V_{CC1} = 5.5 V, V_{CC2} = 24 V I_{sink} = 50 mA, T_A = 25°C Fig. 7			55	70	mA
I_{CC2}	Supply Current from V_{CC2}, Either Source On		V_{CC1} = 5.5 V, V_{CC2} = 24 V I_{source} = −50 mA, T_A = 25°C Fig. 8			32	50	mA

NOTES:

1. Voltage values are with respect to network ground terminal.
2. Refer to Dissipation Derating Curve, Figure 13.
3. Not more than one output is to be on at any one time.
4. Parameters measured using the following pulse techniques; t_W = 200 μs, duty cycle ≤ 2%.

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ELECTRICAL CHARACTERISTICS: Rating apply for $0°C \leq T_A \leq 70°C$ unless otherwise specified.

SYMBOL	CHARACTERISTICS		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Input HIGH Voltage		Fig. 1 & 2		2.0			V
V_{IL}	Input LOW Voltage		Fig. 3 & 4				0.8	V
V_{CD}	Input Clamp Diode Voltage		V_{CC1} = 4.5 V, V_{CC2} = 24 V I_{IN} = −10 mA, T_A = 25°C Fig. 5			−1.3	−1.7	V
I_{OFF}	Source-collectors Terminal Off-State Current		V_{CC1} = 4.5 V, V_{CC2} = 24 V Fig. 1	Full Range			200	μA
				T_A = 25°C		3.0	200	
V_{OH}	Sink Output HIGH Voltage		V_{CC1} = 4.5 V, V_{CC2} = 24 V I_{OUT} = 0, Fig. 2		19	23		V
V_{SAT}	Saturation Voltage	Source Outputs	V_{CC1} = 4.5 V, V_{CC2} = 15 V R_L = 24 Ω, $I_{source} \approx$ −600 mA See Notes 3 & 4, and Fig. 3	Full Range			0.9	V
				T_A = 25°C		0.43	0.75	
		Sink Outputs	V_{CC1} = 4.5 V, V_{CC2} = 15 V R_L = 24 Ω, $I_{sink} \approx$ 600 mA See Notes 3 & 4, and Fig. 4	Full Range			0.9	V
				T_A = 25°C			0.75	
I_{IN}	Input Current at Maximum Input Voltage	Address Inputs	V_{CC1} = 5.5 V, V_{CC2} = 24 V V_{IN} = 5.5 V, Fig. 5				1.0	mA
		Strobe Inputs					2.0	
I_{IH}	Input HIGH Current	Address Inputs	V_{CC1} = 5.5 V, V_{CC2} = 24 V V_{IN} = 2.4 V, Fig. 5			3.0	40	μA
		Strobe Inputs				6.0	80	
I_{IL}	Input LOW Current	Address Inputs	V_{CC1} = 5.5 V, V_{CC2} = 24 V V_{IN} = 0.4 V, Fig. 5			−1.0	−1.6	mA
		Strobe Inputs				−2.0	−3.2	
$I_{CC(off)}$	Supply Current, All Sources and Sinks Off	From V_{CC1}	V_{CC1} = 5.5 V, V_{CC2} = 24 V T_A = 25°C, Fig. 6			14	22	mA
		From V_{CC2}				7.5	20	
I_{CC1}	Supply Current from V_{CC1}, Either Sink On		V_{CC1} = 5.5 V, V_{CC2} = 24 V I_{sink} = 50 mA, T_A = 25°C Fig. 7			55	70	mA
I_{CC2}	Supply Current from V_{CC2}, Either Source On		V_{CC1} = 5.5 V, V_{CC2} = 24 V I_{source} = −50 mA, T_A = 25°C Fig. 8			32	50	mA

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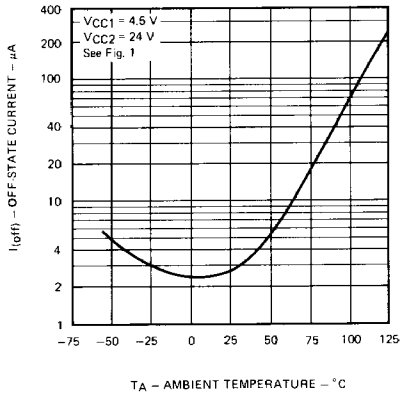
SWITCHING CHARACTERISTICS: V_{CC1} = 5.0 V, T_A = 25°C (See Test Circuit Figures 9 and 10)

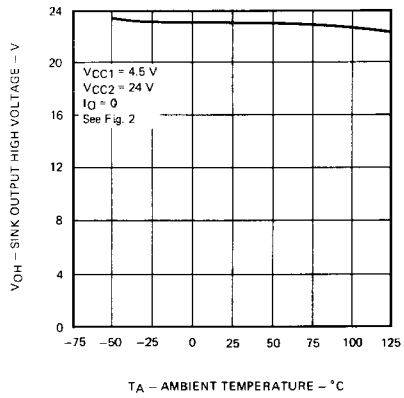
SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time to Source Collectors	9	V_{CC2} = 15 V, R_L = 24 Ω C_L = 25 pF		25	50	ns
t_{PHL}					25	50	
t_{TLH}	Transition Time to Source Outputs	10	V_{CC2} = 20 V, R_L = 1 kΩ C_L = 25 pF		55		ns
t_{THL}					7.0		
t_{PLH}	Propagation Delay Time to Sink Outputs	9	V_{CC2} = 15 V, R_L = 24 Ω C_L = 25 pF		20	45	ns
t_{PHL}					20	45	
t_{TLH}	Transition Time to Sink Outputs	9	V_{CC2} = 15 V, R_L = 24 Ω C_L = 25 pF		7.0	15	ns
t_{THL}					9.0	20	
t_s	Storage Time to Sink Outputs	9	V_{CC2} = 15 V, R_L = 24 Ω C_L = 25 pF		15	30	ns

TYPICAL PERFORMANCE CURVES

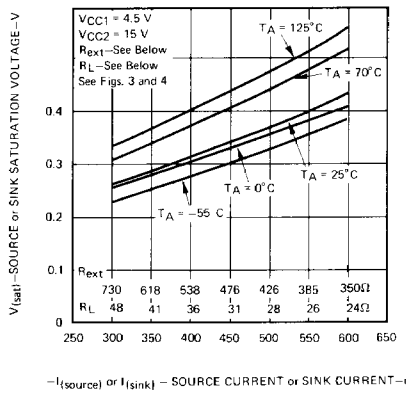
OFF-STATE CURRENT INTO SOURCE COLLECTORS AS A FUNCTION OF AMBIENT TEMPERATURE



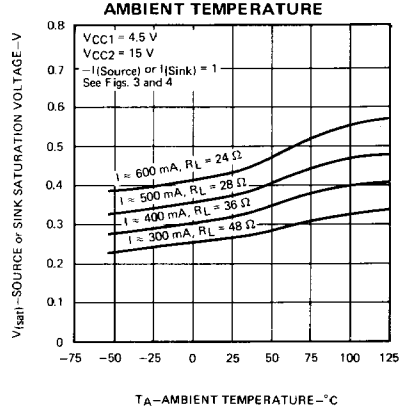
SINK OUTPUT HIGH VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



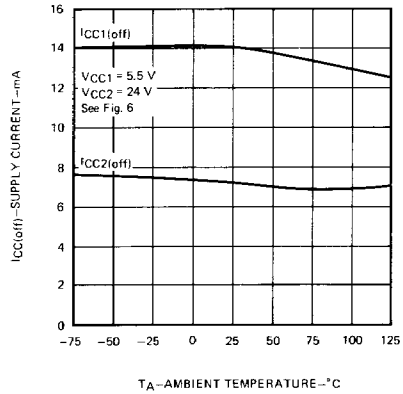
SOURCE OR SINK SATURATION VOLTAGE AS A FUNCTION OF SOURCE CURRENT OR SINK CURRENT



SOURCE OR SINK SATURATION VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



SUPPLY CURRENT, ALL SOURCES AND SINKS OFF AS A FUNCTION OF AMBIENT TEMPERATURE



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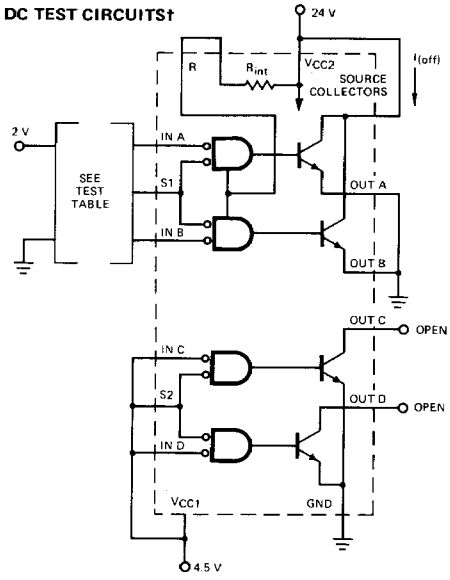
PARAMETER MEASUREMENT INFORMATION

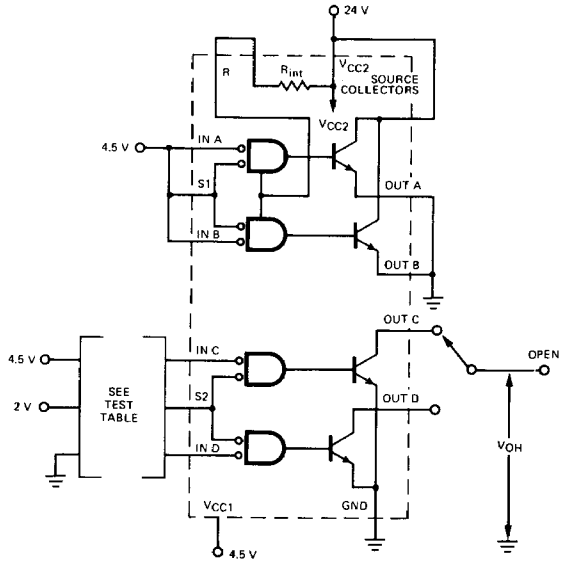
DC TEST CIRCUITS†



TEST TABLE

A	B	S1
GND	GND	2 V
2 V	2 V	GND

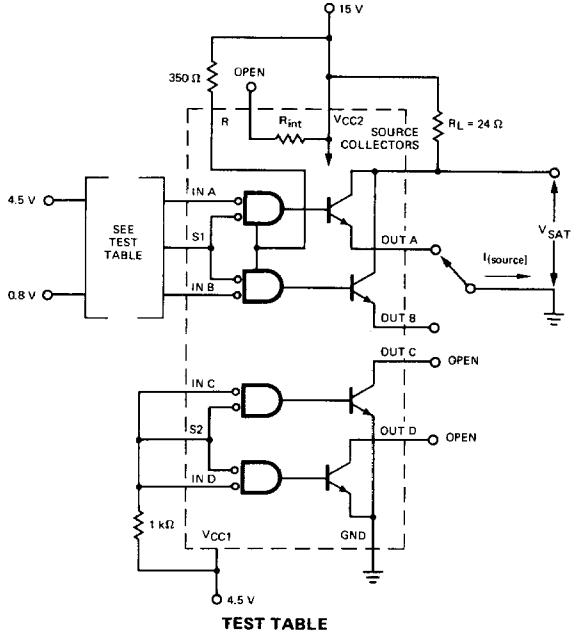
Fig. 1 $I_{(OFF)}$ AND V_{IH}



TEST TABLE

C	D	S2	OUT C	OUT D
2 V	4.5 V	GND	V_{OH}	OPEN
GND	4.5 V	2 V	V_{OH}	OPEN
4.5 V	2 V	GND	OPEN	V_{OH}
4.5 V	GND	2 V	OPEN	V_{OH}

Fig. 2 V_{IH} AND V_{OH}



TEST TABLE

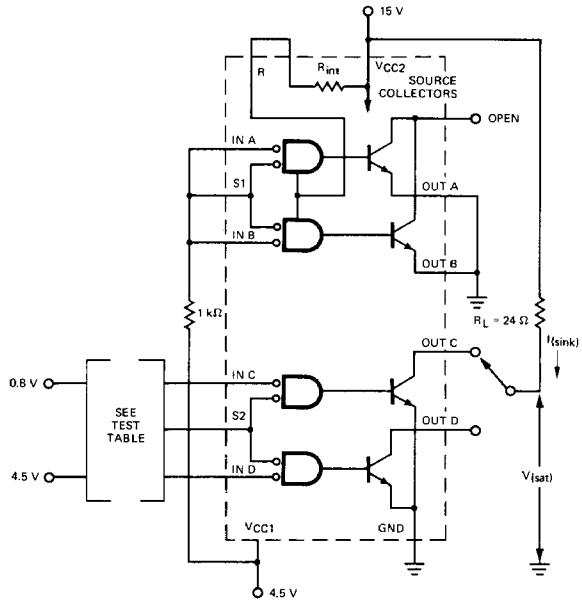
A	B	S1	OUT A	OUT B
0.8 V	4.5 V	0.8 V	GND	OPEN
4.5 V	0.8 V	0.8 V	OPEN	GND

Fig. 3 V_{IL} AND SOURCE $V_{(sat)}$ (Note 4)

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

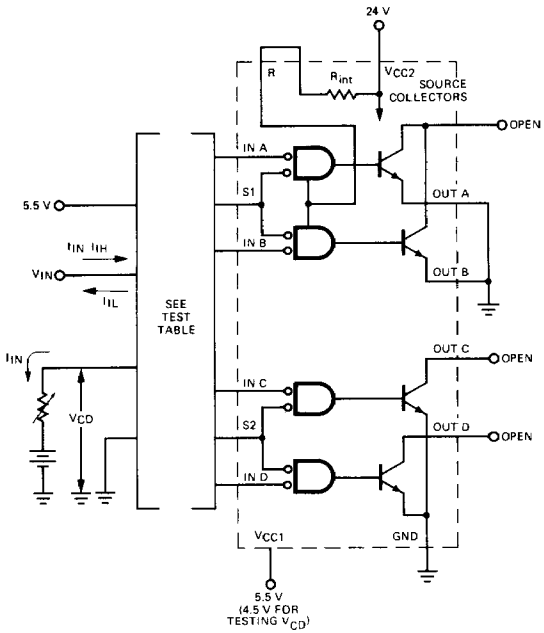
DC TEST CIRCUITS (Cont'd)



TEST TABLE

C	D	S2	OUT C	OUT D
0.8 V	4.5 V	0.8 V	R_L	OPEN
4.5 V	0.8 V	0.8 V	OPEN	R_L

Fig. 4 V_{IL} AND SINK $V_{(sat)}$ (Note 4)



TEST TABLES

I_I, I_{IH}

APPLY V_{IN} = 5.5 V, MEASURE I_{IN} / APPLY V_{IN} = 2.4 V, MEASURE I_{IH}	GROUND	APPLY 5.5 V
A	S1	B, C, S2, D
S1	A, B	C, S2, D
B	S1	A, C, S2, D
C	S2	A, S1, B, D
S2	C, D	A, S1, B
D	S2	A, S1, B, C

V_I, I_{IL}

APPLY V_{IN} = 0.4 V, MEASURE I_{IL} / APPLY I_{IN} = −10 mA MEASURE V_{CD}	APPLY 5.5 V
A	S1, B, C, S2, D
S1	A, B, C, S2, D
B	A, S1, C, S2, D
C	A, S1, B, S2, D
S2	A, S1, B, C, D
D	A, S1, B, C, S2

Fig. 5 V_{CD}, I_{IN}, I_{IH}, AND I_{IL}

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS (Cont'd)

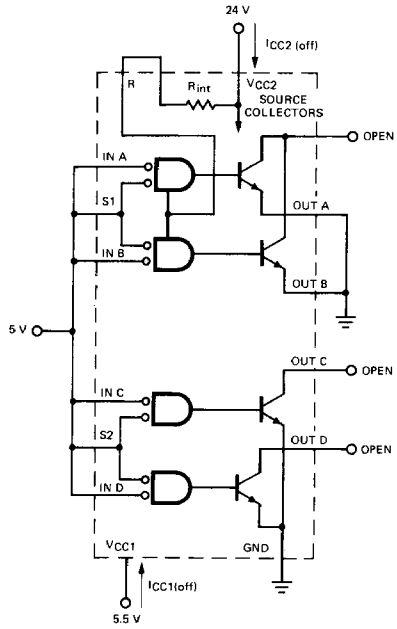
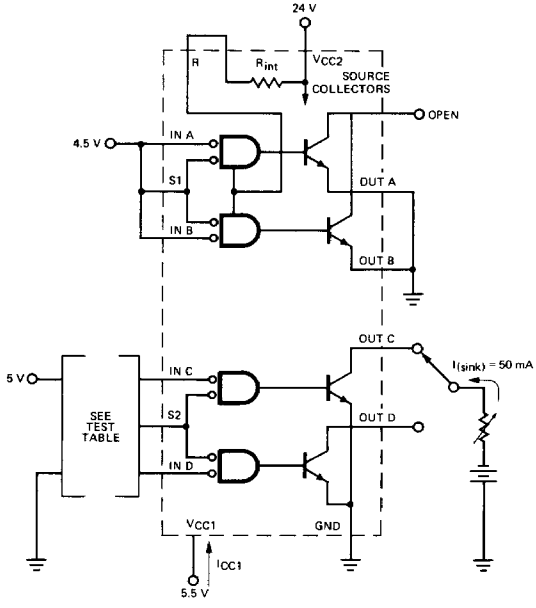


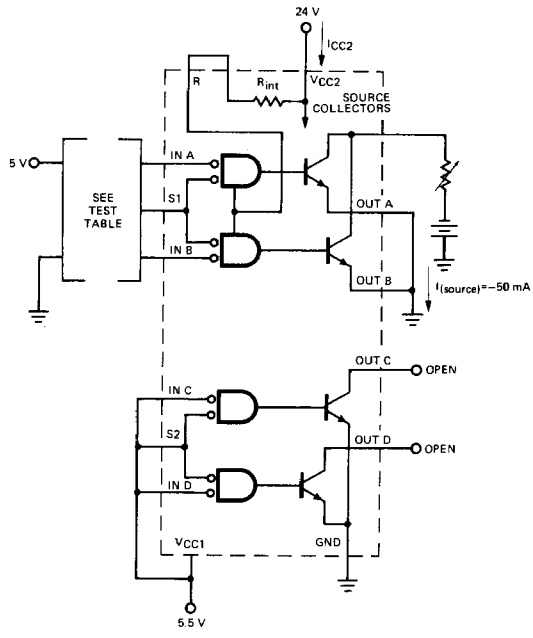
Fig. 6 $I_{CC1(OFF)}$ AND $I_{CC2(OFF)}$



TEST TABLE

C	D	S2	OUT C	OUT D
GND	5 V	GND	I(sink)	OPEN
5 V	GND	GND	OPEN	I(sink)

Fig. 7 I_{CC1}, EITHER SINK ON



TEST TABLE

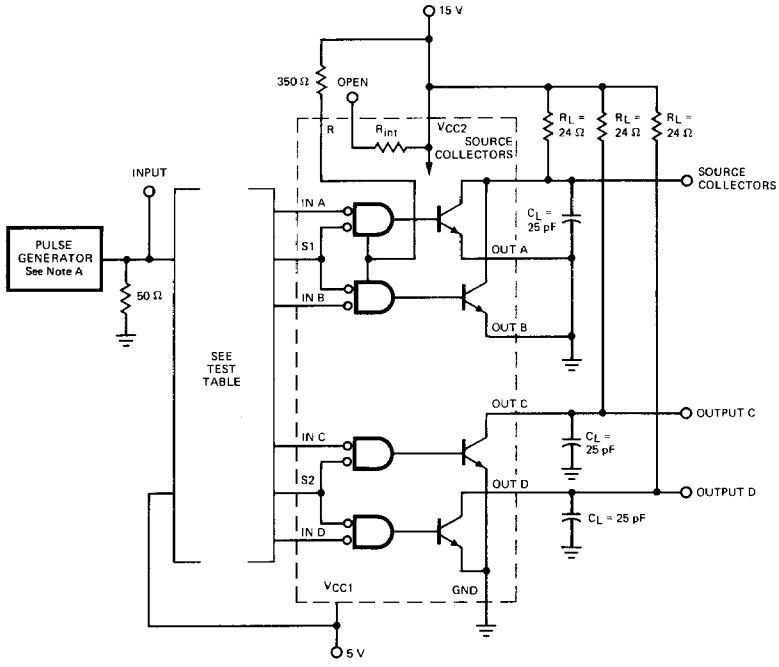
A	B	S1
GND	5 V	GND
5 V	GND	GND

Fig. 8 I_{CC2}, EITHER SOURCE ON

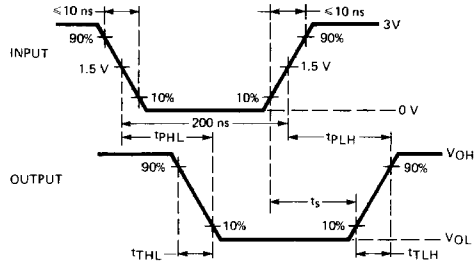
†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS



VOLTAGE WAVEFORMS



TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5 V
t_{PLH} and t_{PHL}	Source collectors	A and S1	B, C, D and S2
		B and S1	A, C, D and S2
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, and t_s	Sink Output C	C and S2	A, B, D and S1
	Sink Output D	D and S2	A, B, C and S1

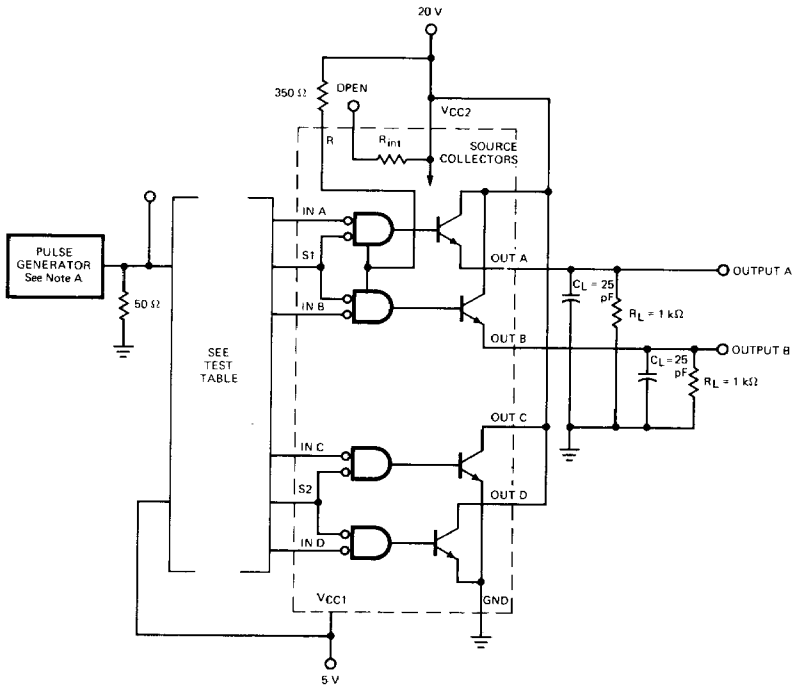
NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, duty cycle ≤ 1%. (f ≤ 50 kHz).
B. C_L includes probe and jig capacitance.

Fig. 9 SWITCHING TIMES

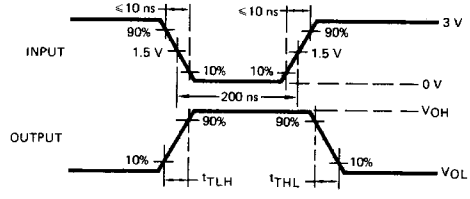
†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Cont'd)



VOLTAGE WAVEFORMS



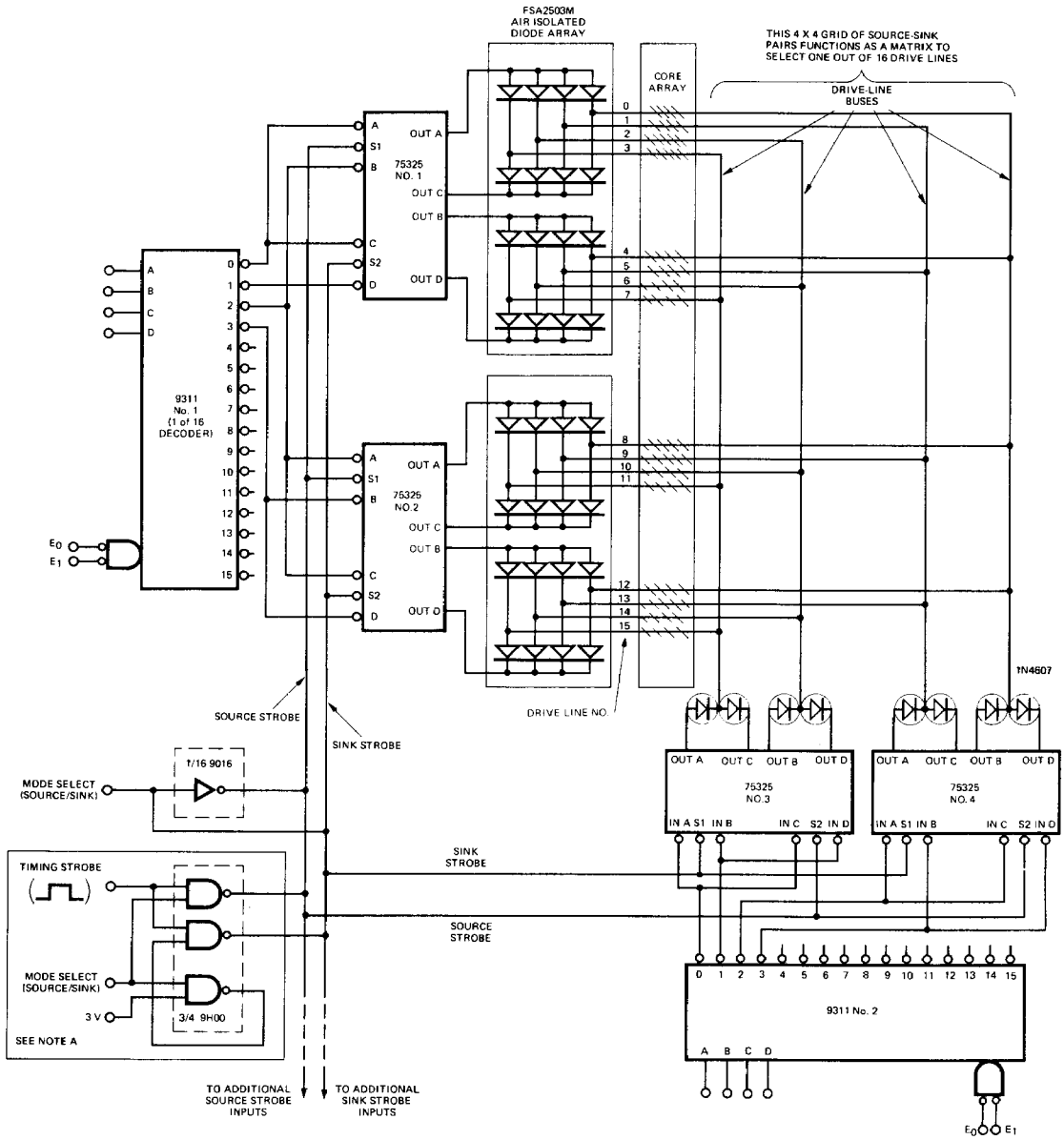
TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5 V
t_{TLH} and t_{THL}	Source Output A	A and S1	B, C, D, and S2
	Source Output B	B and S1	A, C, D, and S2

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, duty cycle ≤ 1%. (f ≤ 50 kHz)
B. C_L includes probe and jig capacitance.

Fig. 10 TRANSITION TIMES OF SOURCE OUTPUTS

APPLICATIONS



In memory-drive applications the 75325 (or for full-temperature operation, the 55325) can be connected in any of several ways. Typically, however, sources and sinks are arranged in pairs from which many drive-lines branch off as shown in Figure 11. Here each drive-line is served by a unique combination of two source/sink pairs so that a selection matrix is formed. To select drive-line 13, 9311 No. 1 must be set to 3 (with mode select HIGH), enabling source B of 75325 No. 2 to drive lines 12 through 15, and 9311 No. 2 must be set to 2, providing a sink at C of 75325 No. 4 for drive-line 13 only. Alternatively, to drive current in drive-line 13 in the opposite direction, only the mode-select voltage would be changed from HIGH to LOW. The size of such a matrix is limited only by the number of drive-lines that a source sink pair can serve. This number in turn depends on the capacitive and inductive load that each drive-line of the particular system imposes on the driver.

NOTE A: This optional mode-select and timing-strobe technique can be used in place of the 9N40 mode-select and 9311 timing-strobe when minimum time skew is desired.

Fig. 11 75325 USED AS A MEMORY DRIVER TO SELECT ONE OF SIXTEEN DRIVE LINES

APPLICATIONS (Cont'd)

EXTERNAL RESISTOR CALCULATION – A typical magnetic-memory word drive requirement is shown in Figure 12. A source-output transistor of one 75325 delivers load current (I_L). The sink-output transistor of another 75325 sinks this current.

The value of the external pull-up resistor (R_{ext}) for a particular memory application may be determined using the following equation:

$$R_{ext} = \frac{16\,[V_{CC2(min)} - V_S - 2.2]}{I_L - 1.6\,[V_{CC2(min)} - V_S - 2.9]} \qquad \text{(Equation 1)}$$

where: R_{ext} is in kΩ,
$V_{CC2(min)}$ is the lowest expected value of V_{CC2} in volts,
V_S is the source output voltage in volts with respect to ground,
I_L is in mA.

The power dissipated in resistor R_{ext} during the load current pulse duration is calculated using Equation 2.

$$P_{Rext} \approx \frac{I_L}{16}\,[V_{CC2(min)} - V_S - 2] \quad \text{where: } P_{Rext} \text{ is in mW.} \qquad \text{(Equation 2)}$$

After solving for R_{ext}, the magnitude of the source collector current (I_{CS}) is determined from Equation 3.

$$I_{CS} \approx 0.94\, I_L \quad \text{where: } I_{CS} \text{ is in mA.} \qquad \text{(Equation 3)}$$

As an example, let $V_{CC2(min)} = 20$ V and $V_L = 3$ V while I_L of 500 mA flows.

Using Equation 1,

$$R_{ext} = \frac{16\,(20 - 3 - 2.2)}{500 - 1.6\,(20 - 3 - 2.9)} = 0.5\ \text{k}\Omega$$

and from Equation 2,

$$P_{Rext} \approx \frac{500}{16}\,[20 - 3 - 2] \approx 470\ \text{mW}$$

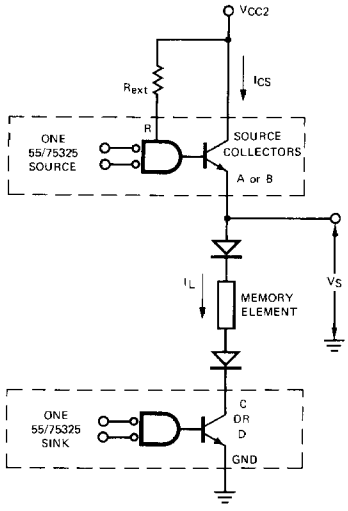
The amount of the memory system current source (I_{CS}) from Equation 3 is:

$$I_{CS} \approx 0.94\,(500) \approx 470\ \text{mA}$$

In this example the regulated source-output transistor base current through the external pull-up resistor (R_{ext}) and the source gate is approximately 30 mA. This current and I_{CS} comprise I_L.

TYPICAL APPLICATION DATA

EXTERNAL RESISTOR CALCULATION (Cont'd)



NOTES: A. For clarity, partial logic diagrams of two 75325's are shown.
B. Source and sink shown are in different packages.

Fig. 12

THERMAL INFORMATION

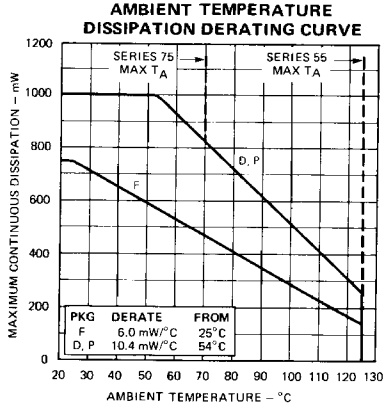


Fig. 13