STSI-144 Scalable Time-Slot Interchanger Hardware Design Guide

Introduction

This document describes the hardware interfaces to Agere Systems Inc. scalable time-slot interchanger (STSI-144) device. Information relevant to the use of the device in a board design is covered. Ball descriptions, dc electrical characteristics, timing diagrams, ac timing parameters, packaging, and operating conditions are included.

Related Documents

More information on the STSI-144 is contained in the following documents:

- STSI-144 Product Description
- STSI-144 Register Description
- STSI-144 Systems Design Guide

Description

Block Diagram and High-Level Interface Definition

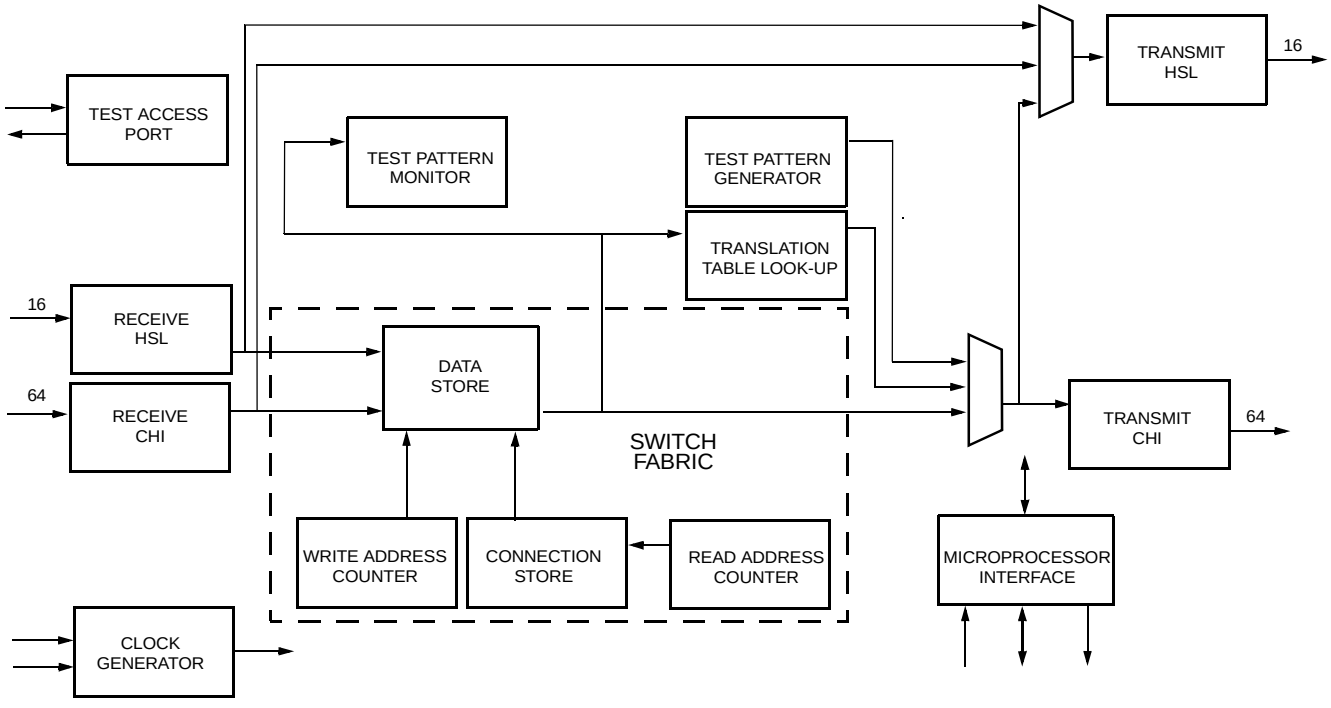

Figure 1. Block Diagram and High-Level Interface Definition

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Ball Diagram

The STSI-144 is housed in a 388-ball plastic ball grid array. Figure 2 shows the ball arrangement viewed from the top of the package. The balls are spaced on a 1.0 mm pitch.

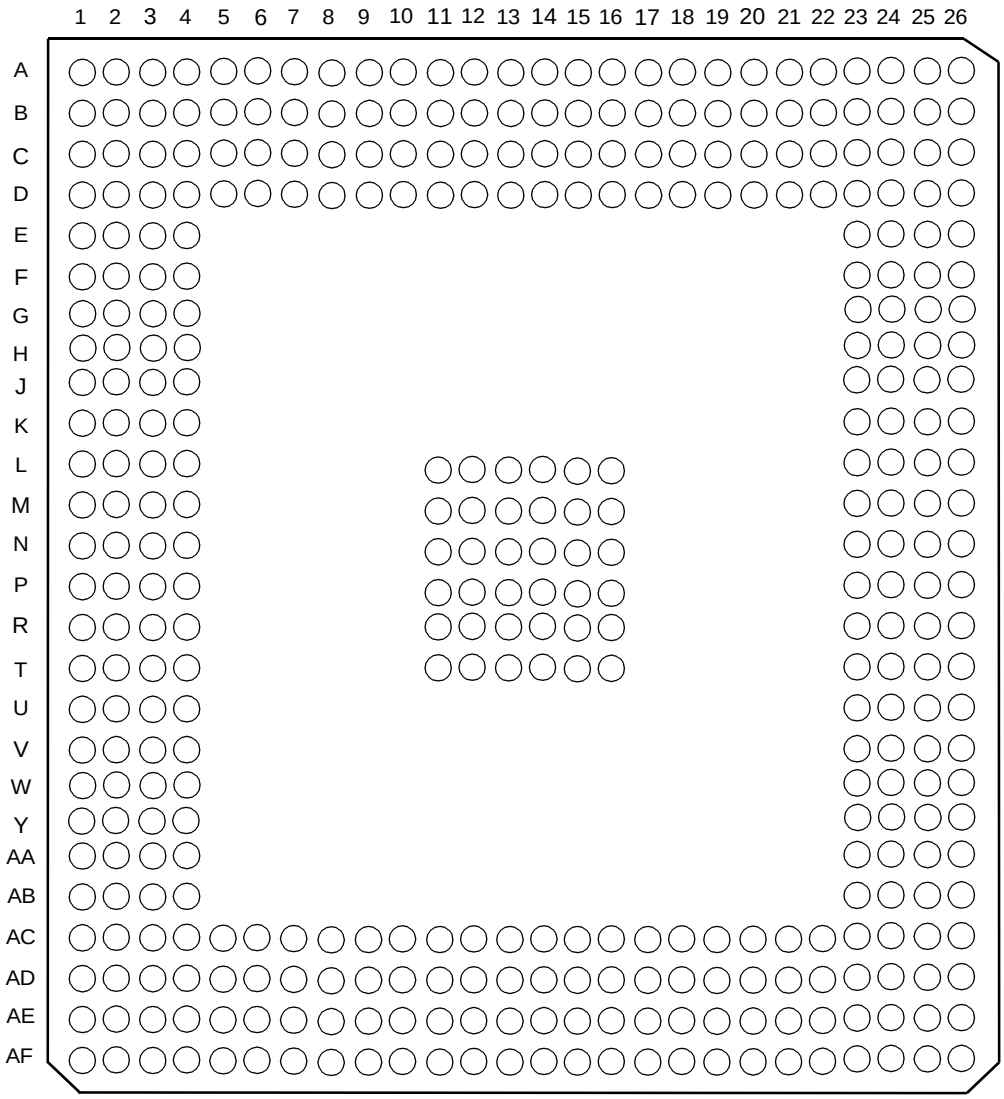


Figure 2. Package Diagram (Top View)

Ball Information (continued)

Package Ball Assignments

Table 1. Package Ball Assignments in Signal Name Order

Symbol	Ball	Symbol	Ball	Symbol	Ball	Symbol	Ball	Symbol	Ball
ADDR00	L24	DATA09	Y25	HSLINP12	A12	MPUCLK	U23	RXD18	AF16
ADDR01	M26	DATA10	Y24	HSLINP13	C12	PAR0	AC26	RXD19	AE16
ADDR02	M25	DATA11	AA26	HSLINP14	B13	PAR1	AB24	RXD20	AF17
ADDR03	M24	DATA12	AA25	HSLINP15	C13	R/$\overline{W}$	L26	RXD21	AF18
ADDR04	N26	DATA13	AA24	HSLOUTN00	A14	REF10	D18	RXD22	AE18
ADDR05	N25	DATA14	AB26	HSLOUTN01	D14	REF14	C18	RXD23	AF19
ADDR06	N24	DATA15	AB25	HSLOUTN02	A15	REFCLK	AD26	RXD24	AF20
ADDR07	P26	$\overline{DT}$	J24	HSLOUTN03	C15	REFSYNC	AF25	RXD25	AE20
ADDR08	P25	FSYNC	AC20	HSLOUTN04	A16	$\overline{RESET}$	K25	RXD26	AF21
ADDR09	P24	$\overline{HIZ}$	AC25	HSLOUTN05	C16	RESHI	C19	RXD27	AF22
ADDR10	R26	HSLINN00	B3	HSLOUTN06	A17	RESLO	D19	RXD28	AE22
ADDR11	R25	HSLINN01	C4	HSLOUTN07	A18	RSV1	G25	RXD29	AF23
ADDR12	R24	HSLINN02	B4	HSLOUTN08	A19	RSV2	G26	RXD30	AF24
ADDR13	T26	HSLINN03	B5	HSLOUTN09	A20	RSV3	F24	RXD31	AE24
ADDR14	T25	HSLINN04	B6	HSLOUTN10	C21	RSV4	F25	RXD32	AD4
ADDR15	T24	HSLINN05	C6	HSLOUTN11	B21	RSV5	F26	RXD33	AE4
$\overline{AS}$	L25	HSLINN06	A7	HSLOUTN12	B22	RSV6	E26	RXD34	AD5
CHICLK	AC24	HSLINN07	A8	HSLOUTN13	C22	RSV7	D26	RXD35	AD6
CK155MHZN	D11	HSLINN08	D8	HSLOUTN14	B23	RSV8	D25	RXD36	AE6
CK155MHZP	C11	HSLINN09	B9	HSLOUTN15	B24	RSV9	D24	RXD37	AD7
CK78MHZ	AC18	HSLINN10	A9	HSLOUTP00	B14	RXD00	AE3	RXD38	AD8
CKSPD0	E24	HSLINN11	C10	HSLOUTP01	C14	RXD01	AF3	RXD39	AE8
CKSPD1	E25	HSLINN12	A11	HSLOUTP02	B15	RXD02	AF4	RXD40	AD9
$\overline{CS}$	K24	HSLINN13	B12	HSLOUTP03	D15	RXD03	AE5	RXD41	AD10
CTAPIN0	D5	HSLINN14	A13	HSLOUTP04	B16	RXD04	AF5	RXD42	AE10
CTAPIN1	D7	HSLINN15	D13	HSLOUTP05	D16	RXD05	AF6	RXD43	AD11
CTAPIN2	D10	HSLINP00	A3	HSLOUTP06	B17	RXD06	AE7	RXD44	AD12
CTAPIN3	D12	HSLINP01	C5	HSLOUTP07	B18	RXD07	AF7	RXD45	AE12
CTAPIN4	B11	HSLINP02	A4	HSLOUTP08	B19	RXD08	AF8	RXD46	AD13
DATA00	U26	HSLINP03	A5	HSLOUTP09	B20	RXD09	AE9	RXD47	AE13
DATA01	U25	HSLINP04	A6	HSLOUTP10	D21	RXD10	AF9	RXD48	AE14
DATA02	V26	HSLINP05	C7	HSLOUTP11	A21	RXD11	AF10	RXD49	AD14
DATA03	V25	HSLINP06	B7	HSLOUTP12	A22	RXD12	AE11	RXD50	AE15
DATA04	V24	HSLINP07	B8	HSLOUTP13	C23	RXD13	AF11	RXD51	AD15
DATA05	W26	HSLINP08	C8	HSLOUTP14	A23	RXD14	AF12	RXD52	AD16
DATA06	W25	HSLINP09	C9	HSLOUTP15	A24	RXD15	AF13	RXD53	AE17
DATA07	W24	HSLINP10	A10	HSLRFSEL	AE26	RXD16	AF14	RXD54	AD17
DATA08	Y26	HSLINP11	B10	$\overline{INT}$	K26	RXD17	AF15	RXD55	AD18

Ball Information (continued)

Package Ball Assignments (continued)

Table 1. Package Ball Assignments in Signal Name Order (continued)

Symbol	Ball	Symbol	Ball	Symbol	Ball	Symbol	Ball	Symbol	Ball
RXD56	AE19	TXD28	AB2	V_{DD15}	N12	V_{IO}	P4	V_{SS}	L11
RXD57	AD19	TXD29	AC1	V_{DD15}	N15	V_{PRE}	AF2	V_{SS}	L12
RXD58	AD20	TXD30	AD1	V_{DD15}	N16	V_{SS}	A1	V_{SS}	L15
RXD59	AE21	TXD31	AD2	V_{DD15}	P11	V_{SS}	A2	V_{SS}	L16
RXD60	AD21	TXD32	D3	V_{DD15}	P12	V_{SS}	A26	V_{SS}	L23
RXD61	AD22	TXD33	D2	V_{DD15}	P15	V_{SS}	AA4	V_{SS}	M11
RXD62	AE23	TXD34	E3	V_{DD15}	P16	V_{SS}	AA23	V_{SS}	M12
RXD63	AD23	TXD35	F3	V_{DD15}	R13	V_{SS}	AC4	V_{SS}	M15
TCK	H25	TXD36	F2	V_{DD15}	R14	V_{SS}	AC6	V_{SS}	M16
TDI	H24	TXD37	G3	V_{DD15}	T13	V_{SS}	AC8	V_{SS}	M23
TDO	H26	TXD38	H3	V_{DD15}	T14	V_{SS}	AC10	V_{SS}	N4
TMS	J26	TXD39	H2	V_{DD33}	A25	V_{SS}	AC11	V_{SS}	N13
TRSTN	J25	TXD40	J3	V_{DD33}	AB4	V_{SS}	AC13	V_{SS}	N14
TXD00	C2	TXD41	K3	V_{DD33}	AB23	V_{SS}	AC15	V_{SS}	P13
TXD01	C1	TXD42	K2	V_{DD33}	AC5	V_{SS}	AC16	V_{SS}	P14
TXD02	D1	TXD43	L3	V_{DD33}	AC7	V_{SS}	AC19	V_{SS}	P23
TXD03	E2	TXD44	M3	V_{DD33}	AC9	V_{SS}	AC23	V_{SS}	R4
TXD04	E1	TXD45	M2	V_{DD33}	AC12	V_{SS}	AD3	V_{SS}	R11
TXD05	F1	TXD46	N3	V_{DD33}	AC14	V_{SS}	AD24	V_{SS}	R12
TXD06	G2	TXD47	N2	V_{DD33}	AC17	V_{SS}	AD25	V_{SS}	R15
TXD07	G1	TXD48	P2	V_{DD33}	C25	V_{SS}	AE1	V_{SS}	R16
TXD08	H1	TXD49	P3	V_{DD33}	C26	V_{SS}	AE2	V_{SS}	T4
TXD09	J2	TXD50	R2	V_{DD33}	D6	V_{SS}	AE25	V_{SS}	T11
TXD10	J1	TXD51	R3	V_{DD33}	D9	V_{SS}	AF1	V_{SS}	T12
TXD11	K1	TXD52	T3	V_{DD33}	D22	V_{SS}	AF26	V_{SS}	T15
TXD12	L2	TXD53	U2	V_{DD33}	E4	V_{SS}	B1	V_{SS}	T16
TXD13	L1	TXD54	U3	V_{DD33}	E23	V_{SS}	B2	V_{SS}	T23
TXD14	M1	TXD55	V3	V_{DD33}	G4	V_{SS}	B25	V_{SS}	U24
TXD15	N1	TXD56	W2	V_{DD33}	H23	V_{SS}	B26	V_{SS}	V4
TXD16	P1	TXD57	W3	V_{DD33}	J4	V_{SS}	C3	V_{SS}	W23
TXD17	R1	TXD58	Y3	V_{DD33}	K23	V_{SS}	C24	V_{SS}	Y4
TXD18	T1	TXD59	AA2	V_{DD33}	M4	V_{SS}	D4	V_{SSCDR0}	D17
TXD19	T2	TXD60	AA3	V_{DD33}	N23	V_{SS}	D23	V_{SSCDR1}	C20
TXD20	U1	TXD61	AB3	V_{DD33}	R23	V_{SS}	F4	V_{SSPLL}	AC21
TXD21	V1	TXD62	AC2	V_{DD33}	U4	V_{SS}	F23		
TXD22	V2	TXD63	AC3	V_{DD33}	V23	V_{SS}	G23		
TXD23	W1	V_{DD15}	L13	V_{DD33}	W4	V_{SS}	G24		
TXD24	Y1	V_{DD15}	L14	V_{DD33}	Y23	V_{SS}	H4		
TXD25	Y2	V_{DD15}	M13	V_{DDCDR0}	C17	V_{SS}	J23		
TXD26	AA1	V_{DD15}	M14	V_{DDCDR1}	D20	V_{SS}	K4		
TXD27	AB1	V_{DD15}	N11	V_{DDPLL}	AC22	V_{SS}	L4		

Ball Information (continued)

Package Ball Assignments (continued)

Table 2. Package Ball Assignments in Ball Number Order

Ball	Symbol	Ball	Symbol	Ball	Symbol	Ball	Symbol	Ball	Symbol
A1	VSS	B19	HSLOUTP08	D11	CK155MHZN	H23	VDD33	M23	VSS
A2	VSS	B20	HSLOUTP09	D12	CTAPIN3	H24	TDI	M24	ADDR03
A3	HSLINP00	B21	HSLOUTN11	D13	HSLINN15	H25	TCK	M25	ADDR02
A4	HSLINP02	B22	HSLOUTN12	D14	HSLOUTN01	H26	TDO	M26	ADDR01
A5	HSLINP03	B23	HSLOUTN14	D15	HSLOUTP03	J1	TXD10	N1	TXD15
A6	HSLINP04	B24	HSLOUTN15	D16	HSLOUTP05	J2	TXD09	N2	TXD47
A7	HSLINN06	B25	VSS	D17	VSSCDR0	J3	TXD40	N3	TXD46
A8	HSLINN07	B26	VSS	D18	REF10	J4	VDD33	N4	VSS
A9	HSLINN10	C1	TXD01	D19	RESLO	J23	VSS	N11	VDD15
A10	HSLINP10	C2	TXD00	D20	VDDCDR1	J24	$\overline{DT}$	N12	VDD15
A11	HSLINN12	C3	VSS	D21	HSLOUTP10	J25	TRSTN	N13	VSS
A12	HSLINP12	C4	HSLINN01	D22	VDD33	J26	TMS	N14	VSS
A13	HSLINN14	C5	HSLINP01	D23	VSS	K1	TXD11	N15	VDD15
A14	HSLOUTN00	C6	HSLINN05	D24	RSV9	K2	TXD42	N16	VDD15
A15	HSLOUTN02	C7	HSLINP05	D25	RSV8	K3	TXD41	N23	VDD33
A16	HSLOUTN04	C8	HSLINP08	D26	RSV7	K4	VSS	N24	ADDR06
A17	HSLOUTN06	C9	HSLINP09	E1	TXD04	K23	VDD33	N25	ADDR05
A18	HSLOUTN07	C10	HSLINN11	E2	TXD03	K24	$\overline{CS}$	N26	ADDR04
A19	HSLOUTN08	C11	CK155MHZP	E3	TXD34	K25	$\overline{RESET}$	P1	TXD16
A20	HSLOUTN09	C12	HSLINP13	E4	VDD33	K26	$\overline{INT}$	P2	TXD48
A21	HSLOUTP11	C13	HSLINP15	E23	VDD33	L1	TXD13	P3	TXD49
A22	HSLOUTP12	C14	HSLOUTP01	E24	CKSPD0	L2	TXD12	P4	VIO
A23	HSLOUTP14	C15	HSLOUTN03	E25	CKSPD1	L3	TXD43	P11	VDD15
A24	HSLOUTP15	C16	HSLOUTN05	E26	RSV6	L4	VSS	P12	VDD15
A25	VDD33	C17	VDDCDR0	F1	TXD05	L11	VSS	P13	VSS
A26	VSS	C18	REF14	F2	TXD36	L12	VSS	P14	VSS
B1	VSS	C19	RESHI	F3	TXD35	L13	VDD15	P15	VDD15
B2	VSS	C20	VSSCDR1	F4	VSS	L14	VDD15	P16	VDD15
B3	HSLINN00	C21	HSLOUTN10	F23	VSS	L15	VSS	P23	VSS
B4	HSLINN02	C22	HSLOUTN13	F24	RSV3	L16	VSS	P24	ADDR09
B5	HSLINN03	C23	HSLOUTP13	F25	RSV4	L23	VSS	P25	ADDR08
B6	HSLINN04	C24	VSS	F26	RSV5	L24	ADDR00	P26	ADDR07
B7	HSLINP06	C25	VDD33	G1	TXD07	L25	$\overline{AS}$	R1	TXD17
B8	HSLINP07	C26	VDD33	G2	TXD06	L26	R/$\overline{W}$	R2	TXD50
B9	HSLINN09	D1	TXD02	G3	TXD37	M1	TXD14	R3	TXD51
B10	HSLINP11	D2	TXD33	G4	VDD33	M2	TXD45	R4	VSS
B11	CTAPIN4	D3	TXD32	G23	VSS	M3	TXD44	R11	VSS
B12	HSLINN13	D4	VSS	G24	VSS	M4	VDD33	R12	VSS
B13	HSLINP14	D5	CTAPIN0	G25	RSV1	M11	VSS	R13	VDD15
B14	HSLOUTP00	D6	VDD33	G26	RSV2	M12	VSS	R14	VDD15
B15	HSLOUTP02	D7	CTAPIN1	H1	TXD08	M13	VDD15	R15	VSS
B16	HSLOUTP04	D8	HSLINN08	H2	TXD39	M14	VDD15	R16	VSS
B17	HSLOUTP06	D9	VDD33	H3	TXD38	M15	VSS	R23	VDD33
B18	HSLOUTP07	D10	CTAPIN2	H4	VSS	M16	VSS	R24	ADDR12

Ball Information (continued)

Package Ball Assignments (continued)

Table 2. Package Ball Assignments in Ball Number Order (continued)

Ball	Symbol	Ball	Symbol	Ball	Symbol	Ball	Symbol
R25	ADDR11	Y23	VDD33	AC25	$\overline{HIZ}$	AE17	RXD53
R26	ADDR10	Y24	DATA10	AC26	PAR0	AE18	RXD22
T1	TXD18	Y25	DATA09	AD1	TXD30	AE19	RXD56
T2	TXD19	Y26	DATA08	AD2	TXD31	AE20	RXD25
T3	TXD52	AA1	TXD26	AD3	VSS	AE21	RXD59
T4	VSS	AA2	TXD59	AD4	RXD32	AE22	RXD28
T11	VSS	AA3	TXD60	AD5	RXD34	AE23	RXD62
T12	VSS	AA4	VSS	AD6	RXD35	AE24	RXD31
T13	VDD15	AA23	VSS	AD7	RXD37	AE25	VSS
T14	VDD15	AA24	DATA13	AD8	RXD38	AE26	HSLRFSEL
T15	VSS	AA25	DATA12	AD9	RXD40	AF1	VSS
T16	VSS	AA26	DATA11	AD10	RXD41	AF2	VPRE
T23	VSS	AB1	TXD27	AD11	RXD43	AF3	RXD01
T24	ADDR15	AB2	TXD28	AD12	RXD44	AF4	RXD02
T25	ADDR14	AB3	TXD61	AD13	RXD46	AF5	RXD04
T26	ADDR13	AB4	VDD33	AD14	RXD49	AF6	RXD05
U1	TXD20	AB23	VDD33	AD15	RXD51	AF7	RXD07
U2	TXD53	AB24	PAR1	AD16	RXD52	AF8	RXD08
U3	TXD54	AB25	DATA15	AD17	RXD54	AF9	RXD10
U4	VDD33	AB26	DATA14	AD18	RXD55	AF10	RXD11
U23	MPUCLK	AC1	TXD29	AD19	RXD57	AF11	RXD13
U24	VSS	AC2	TXD62	AD20	RXD58	AF12	RXD14
U25	DATA01	AC3	TXD63	AD21	RXD60	AF13	RXD15
U26	DATA00	AC4	VSS	AD22	RXD61	AF14	RXD16
V1	TXD21	AC5	VDD33	AD23	RXD63	AF15	RXD17
V2	TXD22	AC6	VSS	AD24	VSS	AF16	RXD18
V3	TXD55	AC7	VDD33	AD25	VSS	AF17	RXD20
V4	VSS	AC8	VSS	AD26	REFCLK	AF18	RXD21
V23	VDD33	AC9	VDD33	AE1	VSS	AF19	RXD23
V24	DATA04	AC10	VSS	AE2	VSS	AF20	RXD24
V25	DATA03	AC11	VSS	AE3	RXD00	AF21	RXD26
V26	DATA02	AC12	VDD33	AE4	RXD33	AF22	RXD27
W1	TXD23	AC13	VSS	AE5	RXD03	AF23	RXD29
W2	TXD56	AC14	VDD33	AE6	RXD36	AF24	RXD30
W3	TXD57	AC15	VSS	AE7	RXD06	AF25	REFSYNC
W4	VDD33	AC16	VSS	AE8	RXD39	AF26	VSS
W23	VSS	AC17	VDD33	AE9	RXD09		
W24	DATA07	AC18	CK78MHZ	AE10	RXD42		
W25	DATA06	AC19	VSS	AE11	RXD12		
W26	DATA05	AC20	FSYNC	AE12	RXD45		
Y1	TXD24	AC21	VSSPLL	AE13	RXD47		
Y2	TXD25	AC22	VDDPLL	AE14	RXD48		
Y3	TXD58	AC23	VSS	AE15	RXD50		
Y4	VSS	AC24	CHICLK	AE16	RXD19		

Ball Information (continued)

Package Ball Assignments (continued)

Table 3. Package Ball Assignments in Ball Number Order (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	VSS	VSS	HSLINP 00	HSLINP 02	HSLINP 03	HSLINP 04	HSLINN 06	HSLINN 07	HSLINN 10	HSLINP 10	HSLINN 12	HSLINP 12	HSLINN 14	HSLOUTN 00	HSLOUTN 02	HSLOUTN 04	HSLOUTN 06	HSLOUTN 07	HSLOUTN 08	HSLOUTN 09	HSLOUTP 11	HSLOUTP 12	HSLOUTP 14	HSLOUTP 15	VDD33A	VSS
B	VSS	VSS	HSLINN 00	HSLINN 02	HSLINN 03	HSLINN 04	HSLINP 06	HSLINP 07	HSLINN 09	HSLINP 11	CTAPIN4	HSLINN 13	HSLINP 14	HSLOUTP 00	HSLOUTP 02	HSLOUTP 04	HSLOUTP 06	HSLOUTP 07	HSLOUTP 08	HSLOUTP 09	HSLOUTN 11	HSLOUTN 12	HSLOUTN 14	HSLOUTN 15	VSS	VSS
C	TXD01	TXD00	VSS	HSLINN 01	HSLINP 01	HSLINN 05	HSLINP 05	HSLINP 08	HSLINP 09	HSLINN 11	CK155 MHZP	HSLINP 13	HSLINP 15	HSLOUTP 01	HSLOUTN 03	HSLOUTN 05	VDDCDR0	REF14	RESHI	VSSCDR1	HSLOUTN 10	HSLOUTN 13	HSLOUTP 13	VSS	VDD33	VDD33
D	TXD02	TXD33	TXD32	VSS	CTAPIN0	VDD33	CTAPIN1	HSLINN 08	VDD33	CTAPIN2	CK155 MHZN	CTAPIN3	HSLINN 15	HSLOUTN 01	HSLOUTP 03	HSLOUTP 05	VSSCDR0	REF10	RESLO	VDDCDR1	HSLOUTP 10	VDD33	VSS	RSV9	RSV8	RSV7
E	TXD04	TXD03	TXD34	VDD33	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD3	CKSPD0	CKSPD1	RSV6
F	TXD05	TXD36	TXD35	VSS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS	RSV3	RSV4	RSV5
G	TXD07	TXD06	TXD37	VDD33	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS	VSS	RSV1	RSV2
H	TXD08	TXD39	TXD38	VSS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD33	TDI	TCK	TDO
J	TXD10	TXD09	TXD40	VDD33	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS	$\overline{DT}$	TRSTN	TMS
K	TXD11	TXD42	TXD41	VSS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD33	$\overline{CS}$	$\overline{RESET}$	$\overline{INT}$
L	TXD13	TXD12	TXD43	VSS	—	—	—	—	—	—	VSS	VSS	VDD15	VDD15	VSS	VSS	—	—	—	—	—	—	VSS	ADDR00	$\overline{AS}$	R/$\overline{W}$
M	TXD14	TXD45	TXD44	VDD33	—	—	—	—	—	—	VSS	VSS	VDD15	VDD15	VSS	VSS	—	—	—	—	—	—	VSS	ADDR03	ADDR02	ADDR01
N	TXD15	TXD47	TXD46	VSS	—	—	—	—	—	—	VDD15	VDD15	VSS	VSS	VDD15	VDD15	—	—	—	—	—	—	VDD33	ADDR06	ADDR05	ADDR04
P	TXD16	TXD48	TXD49	VIO	—	—	—	—	—	—	VDD15	VDD15	VSS	VSS	VDD15	VDD15	—	—	—	—	—	—	VSS	ADDR09	ADDR08	ADDR07
R	TXD17	TXD50	TXD51	VSS	—	—	—	—	—	—	VSS	VSS	VDD15	VDD15	VSS	VSS	—	—	—	—	—	—	VDD33	ADDR12	ADDR11	ADDR10
T	TXD18	TXD19	TXD52	VSS	—	—	—	—	—	—	VSS	VSS	VDD15	VDD15	VSS	VSS	—	—	—	—	—	—	VSS	ADDR15	ADDR14	ADDR13
U	TXD20	TXD53	TXD54	VDD33	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MPUCLK	VSS	DATA01	DATA00
V	TXD21	TXD22	TXD55	VSS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD33	DATA04	DATA03	DATA02
W	TXD23	TXD56	TXD57	VDD33	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS	DATA07	DATA06	DATA05
Y	TXD24	TXD25	TXD58	VSS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD33	DATA10	DATA09	DATA08
AA	TXD26	TXD59	TXD60	VSS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS	DATA13	DATA12	DATA11
AB	TXD27	TXD28	TXD61	VDD33	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD33	PAR1	DATA15	DATA14
AC	TXD29	TXD62	TXD63	VSS	VDD33	VSS	VDD33	VSS	VDD33	VSS	VSS	VDD33	VSS	VDD33	VSS	VSS	VDD33	CK78MHZ	VSS	FSYNC	VSSPLL	VDDPLL	VSS	CHICLK	$\overline{HIZ}$	PAR0
AD	TXD30	TXD31	VSS	RXD32	RXD34	RXD35	RXD37	RXD38	RXD40	RXD41	RXD43	RXD44	RXD46	RXD49	RXD51	RXD52	RXD54	RXD55	RXD57	RXD58	RXD60	RXD61	RXD63	VSS	VSS	REFCLK
AE	VSS	VSS	RXD00	RXD33	RXD03	RXD36	RXD06	RXD39	RXD09	RXD42	RXD12	RXD45	RXD47	RXD48	RXD50	RXD19	RXD53	RXD22	RXD56	RXD25	RXD59	RXD28	RXD62	RXD31	VSS	HSLRFSEL
AF	VSS	VPRE	RXD01	RXD02	RXD04	RXD05	RXD07	RXD08	RXD10	RXD11	RXD13	RXD14	RXD15	RXD16	RXD17	RXD18	RXD20	RXD21	RXD23	RXD24	RXD26	RXD27	RXD29	RXD30	REFSYNC	VSS

Ball Information (continued)

Package Ball Assignments (continued)

Table 4. Package Ball Assignments in Ball Number Order (Bottom View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
AF	VSS	VPRE	RXD01	RXD02	RXD04	RXD05	RXD07	RXD08	RXD10	RXD11	RXD13	RXD14	RXD15	RXD16	RXD17	RXD18	RXD20	RXD21	RXD23	RXD24	RXD26	RXD27	RXD29	RXD30	REFSYNC	VSS
AE	VSS	VSS	RXD00	RXD33	RXD03	RXD36	RXD06	RXD39	RXD09	RXD42	RXD12	RXD45	RXD47	RXD48	RXD50	RXD19	RXD53	RXD22	RXD56	RXD25	RXD59	RXD28	RXD62	RXD31	VSS	HSLRFSEL
AD	TXD30	TXD31	VSS	RXD32	RXD34	RXD35	RXD37	RXD38	RXD40	RXD41	RXD43	RXD44	RXD46	RXD49	RXD51	RXD52	RXD54	RXD55	RXD57	RXD58	RXD60	RXD61	RXD63	VSS	VSS	REFCLK
AC	TXD29	TXD62	TXD63	VSS	VDD33	VSS	VDD33	VSS	VDD33	VSS	VSS	VDD33	VSS	VDD33	VSS	VSS	VDD33	CK78MHZ	VSS	FSYNC	VSSPLL	VDDPLL	VSS	CHICLK	$\overline{HIZ}$	PAR0
AB	TXD27	TXD28	TXD61	VDD33	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD33	PAR1	DATA15	DATA14
AA	TXD26	TXD59	TXD60	VSS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS	DATA13	DATA12	DATA11
Y	TXD24	TXD25	TXD58	VSS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD33	DATA10	DATA09	DATA08
W	TXD23	TXD56	TXD57	VDD33	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS	DATA07	DATA06	DATA05
V	TXD21	TXD22	TXD55	VSS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD33	DATA04	DATA03	DATA02
U	TXD20	TXD53	TXD54	VDD33	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MPUCLK	VSS	DATA01	DATA00
T	TXD18	TXD19	TXD52	VSS	—	—	—	—	—	—	VSS	VSS	VDD15	VDD15	VSS	VSS	—	—	—	—	—	—	VSS	ADDR15	ADDR14	ADDR13
R	TXD17	TXD50	TXD51	VSS	—	—	—	—	—	—	VSS	VSS	VDD15	VDD15	VSS	VSS	—	—	—	—	—	—	VDD33	ADDR12	ADDR11	ADDR10
P	TXD16	TXD48	TXD49	VIO	—	—	—	—	—	—	VDD15	VDD15	VSS	VSS	VDD15	VDD15	—	—	—	—	—	—	VSS	ADDR09	ADDR08	ADDR07
N	TXD15	TXD47	TXD46	VSS	—	—	—	—	—	—	VDD15	VDD15	VSS	VSS	VDD15	VDD15	—	—	—	—	—	—	VDD33	ADDR06	ADDR05	ADDR04
M	TXD14	TXD45	TXD44	VDD33	—	—	—	—	—	—	VSS	VSS	VDD15	VDD15	VSS	VSS	—	—	—	—	—	—	VSS	ADDR03	ADDR02	ADDR01
L	TXD13	TXD12	TXD43	VSS	—	—	—	—	—	—	VSS	VSS	VDD15	VDD15	VSS	VSS	—	—	—	—	—	—	VSS	ADDR00	$\overline{AS}$	R/$\overline{W}$
K	TXD11	TXD42	TXD41	VSS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD33	$\overline{CS}$	$\overline{RESET}$	$\overline{INT}$
J	TXD10	TXD09	TXD40	VDD33	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS	$\overline{DT}$	TRSTN	TMS
H	TXD08	TXD39	TXD38	VSS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD33	TDI	TCK	TDO
G	TXD07	TXD06	TXD37	VDD33	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS	VSS	RSV1	RSV2
F	TXD05	TXD36	TXD35	VSS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS	RSV3	RSV4	RSV5
E	TXD04	TXD03	TXD34	VDD33	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD3	CKSPD0	CKSPD1	RSV6
D	TXD02	TXD33	TXD32	VSS	CTAPIN0	VDD33	CTAPIN1	HSLINN 08	VDD33	CTAPIN2	CK155 MHZN	CTAPIN3	HSLINN 15	HSLOUTN 01	HSLOUTP 03	HSLOUTP 05	VSSCDR0	REF10	RESLO	VDDCDR1	HSLOUTP 10	VDD33	VSS	RSV9	RSV8	RSV7
C	TXD01	TXD00	VSS	HSLINN 01	HSLINP 01	HSLINN 05	HSLINP 05	HSLINP 08	HSLINP 09	HSLINN 11	CK155 MHZP	HSLINP 13	HSLINP 15	HSLOUTP 01	HSLOUTN 03	HSLOUTN 05	VDDCDR0	REF14	RESHI	VSSCDR1	HSLOUTN 10	HSLOUTN 13	HSLOUTP 13	VSS	VDD33	VDD33
B	VSS	VSS	HSLINN 00	HSLINN 02	HSLINN 03	HSLINN 04	HSLINP 06	HSLINP 07	HSLINN 09	HSLINP 11	CTAPIN4	HSLINN 13	HSLINP 14	HSLOUTP 00	HSLOUTP 02	HSLOUTP 04	HSLOUTP 06	HSLOUTP 07	HSLOUTP 08	HSLOUTP 09	HSLOUTN 11	HSLOUTN 12	HSLOUTN 14	HSLOUTN 15	VSS	VSS
A	VSS	VSS	HSLINP 00	HSLINP 02	HSLINP 03	HSLINP 04	HSLINN 06	HSLINN 07	HSLINN 10	HSLINP 10	HSLINN 12	HSLINP 12	HSLINN 14	HSLOUTN 00	HSLOUTN 02	HSLOUTN 04	HSLOUTN 06	HSLOUTN 07	HSLOUTN 08	HSLOUTN 09	HSLOUTP 11	HSLOUTP 12	HSLOUTP 14	HSLOUTP 15	VDD33A	VSS

Ball Information (continued)

Ball Types

This table describes each type of input, output, and I/O ball used on the STSI-144.

Table 5. Ball Types

Type Label	Description
I	CMOS input, TTL switching thresholds.
I pd	CMOS input, TTL switching thresholds with internal pull-down resistor.
I pu	CMOS input, TTL switching thresholds with internal pull-up resistor.
O	CMOS output.
O od	Open-drain output.
LIN	LVDS inputs.
LOUT	LVDS outputs.
I/O	Bidirectional ball; CMOS input with TTL switching thresholds and CMOS output.
None	Analog inputs for external resistors, capacitors, voltage references, etc.
P	Power and ground.

The dc switching and other electrical characteristics are specified later in this document.

Ball Definitions

This section describes the function of each of the device balls. The balls are listed by ball name. Package ball numbers are listed in Table 1 of this document. The static parameters (drive currents, switching thresholds, etc.) for each ball type (input, output, etc.) are described in Table 16 through Table 21.

Table 6. Timing Port

Ball Name	Type	Name/Description
FSYNC	I	**Frame Synchronization.** This signal indicates the beginning of a 125 µs frame event (8 kHz). The FSYNC ball can be programmed as active-low or active-high, but its polarity is the same for all concentration highway interfaces (CHI). FSYNC can be sampled on either the positive or negative edge of CHICLK. Time-slot numbers and bit offsets for each CHI are assigned relative to the detection of FSYNC.
CHICLK	I	**Clock.** This is the master synchronous clock for the transmit and receive concentration highways. The frequency can be 8.192 MHz or 16.384 MHz. It **must** be at least as fast as the highest CHI data rate.
CKSPD0	I	**Clock Speed.** Static control input that should be tied according to the frequency of CHICLK. If CHICLK is connected to an 8.192 MHz source, CKSPD0 should be tied to VSS. If CHICLK is connected to a 16.384 MHz source, CKSPD0 should be tied to VDD33.
CKSPD1	I pd	**Clock Speed.** Reserved, leave disconnected. 20 kΩ pull-down resistor.

Ball Information (continued)

Ball Definitions (continued)

Table 7. Transmit and Receive Concentration Highways

Ball Name	Type	Name/Description
RXD[63:00]	I pd	**Receive Data [63:0].** Receive concentration highways. These are serial, synchronous data streams that may be individually programmed to operate at 2.048 Mbits/s, 4.096 Mbits/s, 8.192 Mbits/s, or 16.384 Mbits/s. They carry 32, 64, 128, or 256 time slots (respectively), each occupying eight contiguous bits. 20 kΩ pull-down resistor.
TXD[63:32]	I/O	**Transmit Data [63:32].** Normally these are output concentration highway data streams with data rate options identical to the RXD inputs. These balls can be configured to operate as bidirectional multiplex ports. Further information can be found in the system design guide. 20 kΩ pull-down resistor.
TXD[31:00]	I/O	**Transmit Data [31:00].** Normally these are output concentration highway data streams with data rate options identical to the RXD inputs. These balls can be configured to operate as bidirectional multiplex ports such as H.110. Further information can be found in the system design guide. 20 kΩ resistor connected to VPRE.

Table 8. Control Port

Ball Name	Type	Name/Description
MPUCLK	I	**Processor Clock.** This clock is used to sample address, data, and control signals from the microprocessor. This clock must be within the range of 0 MHz—66 MHz. Required for operation.
$\overline{CS}$	I	**Chip Select.** Active-low chip select. This input is held low for the duration of any read or write access to the STSI-144. Required for operation.
$\overline{AS}$	I	**Address Strobe.** Active-low address strobe that is one MPUCLK cycle wide at the start of a microprocessor access cycle to the STSI-144. This is used to initiate a microprocessor access. Required for operation.
R/$\overline{W}$	I	**Read/Write.** Cycle selection. R/$\overline{W}$ is set high during a read cycle, or set low for a write cycle. Required for operation.
ADDR [15:00]	I pu	**Address [15:00].** ADDR[15] is the most significant bit and ADDR[00] is the least significant bit for addressing all the internal registers during microprocessor access cycles. All addresses are 16-bit word addresses; hence, in a typical application ADDR[00] of the STSI-144 device would be connected to address bit 1 of a byte addressable system address bus. Required for operation. 200 kΩ pull-up resistor. **Note:** The STSI-144 is little-endian; the least significant byte is stored in the lowest address and the most significant byte is stored in the highest address. Care must be exercised in connection to microprocessors that use big-endian byte ordering.
DATA [15:00]	I/O	**Data [15:00].** Data bus for all transfers between the microprocessor and the internal registers. The balls are inputs during write cycles and outputs during read cycles. DATA15 is the most significant bit, and DATA00 is the least significant bit. Required for operation.
PAR[1:0]	I/O	**Control Port Parity [1:0].** Byte-wide parity bits for data. PAR[1] is the parity for DATA [15:8], and PAR[0] is the parity for DATA [7:0]. The parity sense (even or odd) is application programmable via a register bit in the STSI-144. **Not** required for operation.
$\overline{DT}$	O	**Data Transfer Acknowledge.** Active-low for one MPUCLK cycle. Indicates that data has been written during write cycles or that data is valid during read cycles. High impedance when $\overline{CS}$ is a 1 and driven when $\overline{CS}$ is 0. Required for operation.
$\overline{INT}$	O od	**Interrupt.** This output is asserted low to indicate that an interrupt condition has occurred. This signal remains active-low until the interrupt status register has been cleared or masked.

Ball Information (continued)

Ball Definitions (continued)

Table 9. High-Speed Serial Link Signals

Ball Name	Type	Name/Description
HSLIN[P,N] [15:00]	LIN	**High-Speed Serial Link Input.** 622.08 Mbits/s LVDS data input. Unused inputs may be left disconnected.
HSLOUT[P,N] [15:00]	LOUT	**High-Speed Serial Link Output.** 622.08 Mbits/s LVDS data output.
CK155MHZ[P,N]	LIN	155.52 MHz LVDS reference clock input.*
CK78MHZ	I pu	77.76 MHz CMOS reference clock input. 200 kΩ pull-up resistor.*
HSLRFSEL	I pd	**High-Speed Serial Link Reference Select.** HSL clock reference select. 50 kΩ pull-down resistor. 0 = 78 MHz. The CK78MHZ input is used as the reference. 1 = 155 MHz. The CK155MHZ[P,N] input is used as the reference.
REFCLK	O	**Reference Clock Output.** 8 kHz, 16.384 MHz, or 38.88 MHz derived from an HSL input stream. (See Reference_Clock_Select in the Global_Control register in the STSI-144 Register Description.)
REFSYNC	O	**Reference Synchronization Output.** Active-high 8 kHz sync pulse, one REFCLK period wide, derived from an HSL input stream.
RESHI	None	**External 100 Ω Resistor Pin 1.** A 100 Ω ± 1% resistor is required as a reference for LVDS buffers.
RESLO	None	**External 100 Ω Resistor Pin 2.**
REF10	None	**External 1.0 V Reference.** (Optional) Selected by Power_Control register bit 2.
REF14	None	**External 1.4 V Reference.** (Optional) Selected by Power_Control register bit 2.
CTAP[4:0]	None	**LVDS Termination Center Taps.** (Optional) Bypass to ground with 0.01 µF capacitor.

* One of either CK78MHZ or CK155MHZ[P,N] is required; the other may be left unconnected.

Table 10. Initialization and Test Access

Ball Name	Type	Name/Description
$\overline{\text{RESET}}$	I pu	**Reset.** Global reset, active-low. Initializes all internal registers to their default state. The reset occurs asynchronously, but $\overline{\text{RESET}}$ should be held low for at least 1 µs. 20 kΩ pull-up resistor.
TCK	I pu	**Test Clock.** This signal provides timing for the boundary scan and test access port (TAP) controller. Should be static except during boundary-scan testing. 20 kΩ pull-up resistor.
TDI	I pu	**Test Data In.** Data input for the boundary scan. Sampled on the rising edge of TCK. 20 kΩ pull-up resistor.
TMS	I pu	**Test Mode Select (Active-Low).** Controls boundary-scan test operations. TMS is sampled on the rising edge of TCK. 20 kΩ pull-up resistor.
TRSTN	I pd	**Test Reset (Active-Low).** This signal is an asynchronous reset for the TAP controller. 20 kΩ pull-down resistor.
TDO	O	**Test Data Out.** Updated on the falling edge of TCK. The TDO output is high impedance except when scanning out test data.
$\overline{\text{HIZ}}$	I pu	**Output Enable.** All output and bidirectional buffers will be high impedance when this input is low unless boundary scan is enabled (TRSTN = 1). 20 kΩ pull-up resistor.
RSV[9:1]	—	**Reserved [9:1].** These balls are used by Agere Systems during the manufacturing process. They must be left unconnected.

Ball Information (continued)

Ball Definitions (continued)

Table 11. Power Balls

Symbol	Type	Name/Description
V_{DD33}	P	**I/O Power.** Power supply balls for the I/O pads (3.3 V ± 5%).
V_{DD15}	P	**Core Power.** Power supply balls for the core (1.5 V ± 5%).
VSS	P	**Ground.** Common ground balls for 3.3 V and 1.5 V supplies.
V_{PRE}	P	**Precharge.** Precharge voltage to support H.110 hot insertion on TXD[31:00]. If the device is used in an H.110 hot insertion applications, the signal should be connected to backplane early voltage; otherwise, connect this signal to ground.
V_{IO}	P	**PCI Buffer Voltage Select.** For an H.110 application using TXD[31:00] in a 5 V signaling environment, connect this signal to 5 V. For an H.110 application using TXD[31:00] in a 3 V signaling environment, connect this signal to V_{DD33}. For all other applications, connect this signal to V_{DD33}.
V_{DDPLL}	P	**PLL Power.** 1.5 V power supply for the internal phase-locked loop. Must include local 0.01 µF capacitor to V_{SSPLL}.
V_{SSPLL}	P	**PLL Ground.** Isolated ground for the internal phase-locked loop.
$V_{DDCDR[1,0]}$	P	**Isolated Clock/Data Recovery 1.5 V ± 5% Power.** These pins require a dedicated inductor/capacitor (L/C) pi filter with local bypass capacitors.
$V_{SSCDR[1,0]}$	P	**Isolated Clock/Data Recovery Ground.**

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 12. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage (V_{DD33})	–0.5	4.2	V
Supply Voltage (V_{DD15})	–0.5	1.8	V
Input Voltage: TXD[63:00] All Other Inputs	 –0.5 –0.3	 5.5 V_{DD33} + 0.3	V
Storage Temperature	–40	125	°C
Junction Temperature	—	125	°C

Handling Precautions

Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. Agere employs both a human-body model (HBM) and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114 (HBM) and JESD22-C101 (CDM) standards.

ESD Tolerance

Table 13. ESD Tolerance

Device	Voltage	Type
STSI-144	2,000 V	HBM (human-body model)
	500 V	CDM (charged-device model)

Package Thermal Characteristics

Table 14. Power Consumption

- Θ_{JA} = 20 °C/W.

Supply Voltage	Typ*	Max
V_{DD33}	750 mW at 3.3 V	900 mW at 3.47 V
V_{DD15}	750 mW at 1.5 V	900 mW at 1.6 V

* MPUCLK = 66 MHz, CHICLK = 16.384 MHz, T_A = 25 °C, all CHIs active, all outputs loaded with 50 pF. All HSLs active.

Recommended Operating Conditions

Table 15. Operating Conditions

Parameter	Min	Typ	Max	Unit
Supply Voltage (V_{DD33})	3.14	3.3	3.47	V
Supply Voltage (V_{DD15})	1.4	1.5	1.6	V
Ambient Temperature	–40	—	85	°C

dc Electrical Characteristics

This section describes all the static parameters associated with all the ball types used in the STSI-144 device.

Table 16. CMOS Inputs

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Leakage Current	I_{IL}	$V_{SS} < V_{IN} < V_{DD33}$	—	—	1*	µA
High-input Voltage	V_{IH}	—	2.0	—	V_{DD33} + 0.3	V
Low-input Voltage	V_{IL}	—	–0.3	—	0.8	V
Input Capacitance	C_I	—	—	2.5	—	pF

* Excludes current due to pull-up or pull-down resistors.

Table 17. CMOS Outputs

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage Low	V_{OL}	I_{OL} = –10 mA	—	—	0.4	V
Output Voltage High	V_{OH}	I_{OL} = 10 mA	2.4	—	—	V
Output Current Low	I_{OL}	—	—	—	10	mA
Output Current High	I_{OH}	—	—	—	10	mA
Output Capacitance	C_O	—	—	3	—	pF
HIZ Output Leakage Current	I_{OZ}	—	—	—	10	µA

Table 18. CMOS Bidirectionals (Excluding TXD[63:00])

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Leakage Current	I_L	$V_{SS} < V_{IN} < V_{DD33}$	—	—	11	µA
High-input Voltage	V_{IH}	—	2.0	—	V_{DD33} + 0.3	V
Low-input Voltage	V_{IL}	—	–0.3	—	0.8	V
Biput Capacitance	C_{IB}	—	—	5.0	—	pF
Output Voltage Low	V_{OL}	I_{OL} = –10 mA	—	—	0.4	V
Output Voltage High	V_{OH}	I_{OL} = 10 mA	2.4	—	—	V

Table 19. CMOS Bidirectionals (TXD[63:00])

Parameter	Symbol	Conditions	Min	Max	Unit
Leakage Current	I_L	$V_{SS} < V_{IN} < V_{DD33}$	—	10	µA
High-input Voltage	V_{IH}	VIO = 5.0 V VIO = 3.3V	2.0 0.5 V_{DD33}	5.5 V_{DD33} + 0.5	V
Low-input Voltage	V_{IL}	VIO = 5.0 V VIO = 3.3V	–0.5 –0.5	0.8 0.3 V_{DD33}	V
Biput Capacitance	C_{IB}	—	—	10	pF
Output Voltage Low	V_{OL}	I_{OL} = 1.5 mA, VIO = 3.3 V I_{OL} = 6.0 mA, VIO = 5.0 V	— —	0.1 V_{DD33} 0.55	V
Output Voltage High	V_{OH}	I_{OL} = –0.5 mA, VIO = 3.3 V I_{OL} = –2.0 mA, VIO = 5.0 V	0.9 V_{DD33} 2.4	— —	V
Positive-going Threshold	V_{t+}	—	1.2	2.0	V
Negative-going Threshold	$V_{t–}$	—	0.6	1.6	V
Hysteresis ($V_{t+} – V_{t–}$)	V_{HYS}	—	0.4	—	V

dc Electrical Characteristics (continued)

Table 20. LVDS Receiver dc Parameters

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Common-mode Input Range	V_{CM}	$\|V_{GPD}\|$ < 925 mV, dc – 1 MHz	0.0	1.2	2.4	V
Input Differential Threshold	V_{IDTH}	$\|V_{GPD}\|$ < 925 mV, 450 MHz	–100	—	100	mV
Input Differential Hysteresis	V_{HYST}	$(+V_{IDTHH}) – (–V_{IDTHL})$	25	—	—	mV
Receiver Differential Input Impedance	R_{IN}	Built-in center-tapped termination	80	100	120	Ω

Table 21. LVDS Transmitter dc Parameters

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage High, P or N	V_{OH}	R_{LOAD} = 100 Ω ± 1%	—	—	1.475*	V
Output Voltage Low, P or N	V_{OL}	R_{LOAD} = 100 Ω ± 1%	0.925*	—	—	V
Output Differential Voltage	$\|V_{OD}\|$	R_{LOAD} = 100 Ω ± 1%	0.25	—	0.45*	V
Output Offset Voltage	V_{OS}	R_{LOAD} = 100 Ω ± 1%	1.125*	—	1.275*	Ω
Output Impedance, Differential	R_O	V_{CM} = 1.0 V and 1.4 V	80	100	120	Ω
Change in Differential Voltage Between Complementary States	$\|\Delta V_{OD}\|$	R_{LOAD} = 100 Ω ± 1%	—	—	25	mV
Change in Output Offset Voltage Between Complementary States	$\|\Delta V_{OS}\|$	R_{LOAD} = 100 Ω ± 1%	—	—	25	mV
Output Current	I_{SA}, I_{SB}	Driver shorted to GND	—	—	24	mA
Output Current	I_{SAB}	Driver shorted together	—	—	12	mA
Power-off Output Leakage	$\|I_{XA}\|$, $\|I_{XB}\|$	HSL disabled, V_{PAD}, V_{PADN} = 0 V—2.5 V	—	—	10	mA

* External references selected (LVDS_Voltage_Reference_Select = 1), REF10 = 1.0 V ± 3%, REF14 = 1.4 V ± 3%.

Timing Diagrams and ac Characteristics

Figure 3 and Figure 4 describe the timing specifications for the input clocks on the STSI-144.

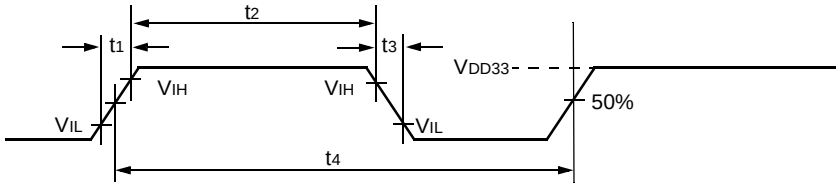


Figure 3. CHICLK Timing Specifications

Table 22. CHICLK Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
t1	CHICLK Rise Time	—	2	7	ns
t2	CHICLK Width (8.192 MHz)*	48.84	—	73.24	ns
t2	CHICLK Width (16.384 MHz)*	24.42	—	36.62	ns
t3	CHICLK Fall Time	—	2	7	ns
t4	CHICLK Period (8.192 MHz)	—	122.07	—	ns
t4	CHICLK Period (16.384 MHz)	—	61.03	—	ns

* VIH to VIH or VIL to VIL.

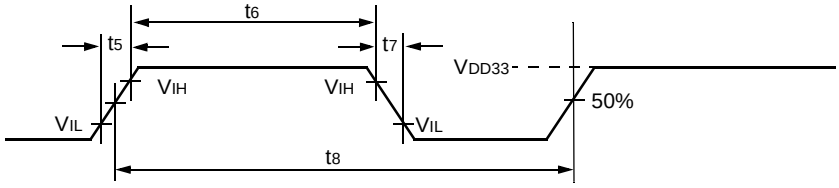


Figure 4. MPUCLK Timing Specifications

Table 23. MPUCLK Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
t5	MPUCLK Rise Time	—	2	7	ns
t6	MPUCLK Width*	6.06	—	—	ns
t7	MPUCLK Fall Time	—	2	7	ns
t8	MPUCLK Period	15.2	—	—	ns

* VIH to VIH or VIL to VIL.

Timing Diagrams and ac Characteristics (continued)

Figure 5 shows the ac timing specifications for the STSI-144. All timing parameters are referenced to V_{IHmin} and V_{ILmax}. The reference signal polarity may be inverted for some timing parameters.

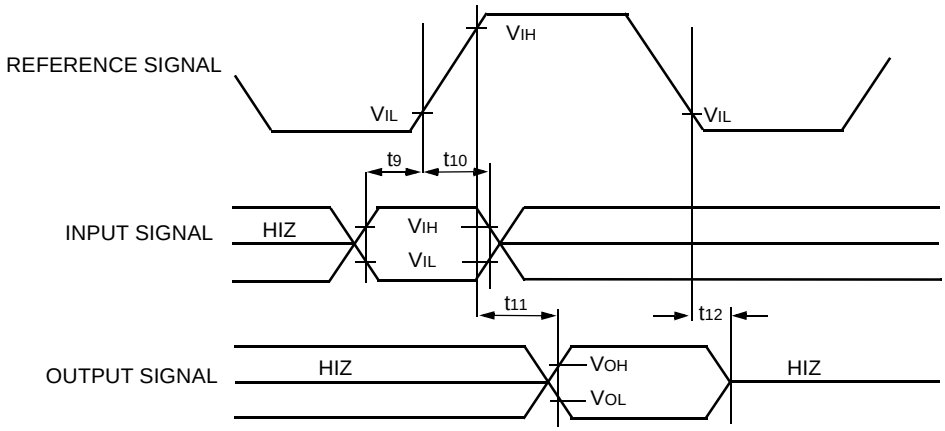
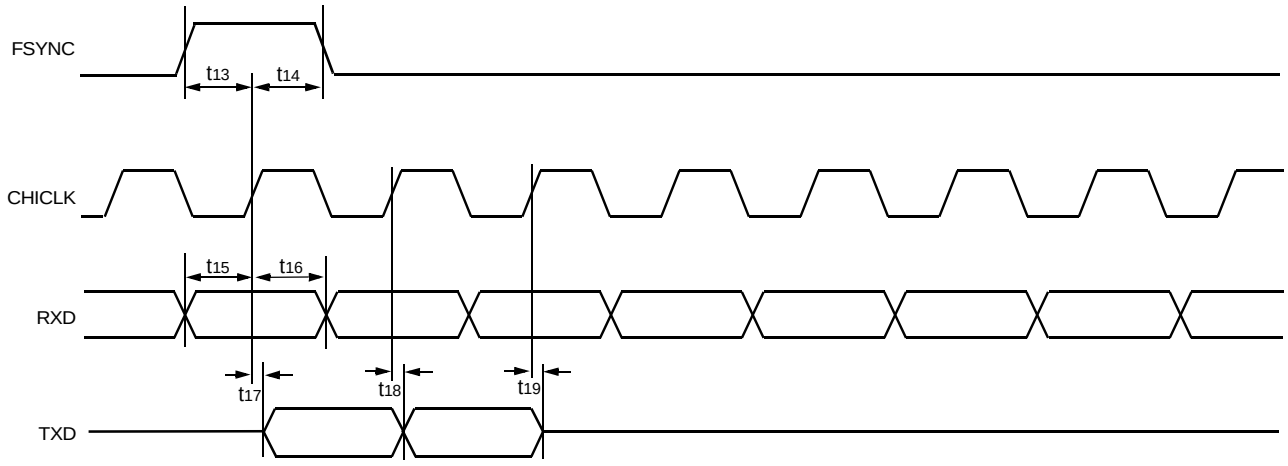


Figure 5. ac Timing Measurement Specification

Table 24. ac Timing Measurement Specification

Parameter	Description
t_9	Setup Time
t_{10}	Hold Time
t_{11}	Output Delay
t_{12}	Output 3-State Time

Timing Diagrams and ac Characteristics (continued)



Note: This figure assumes STSI-144 is programmed to sample FSYNC on rising edge of CHICLK.

Figure 6. CHI Interface Timing

Table 25. CHI Interface Timing

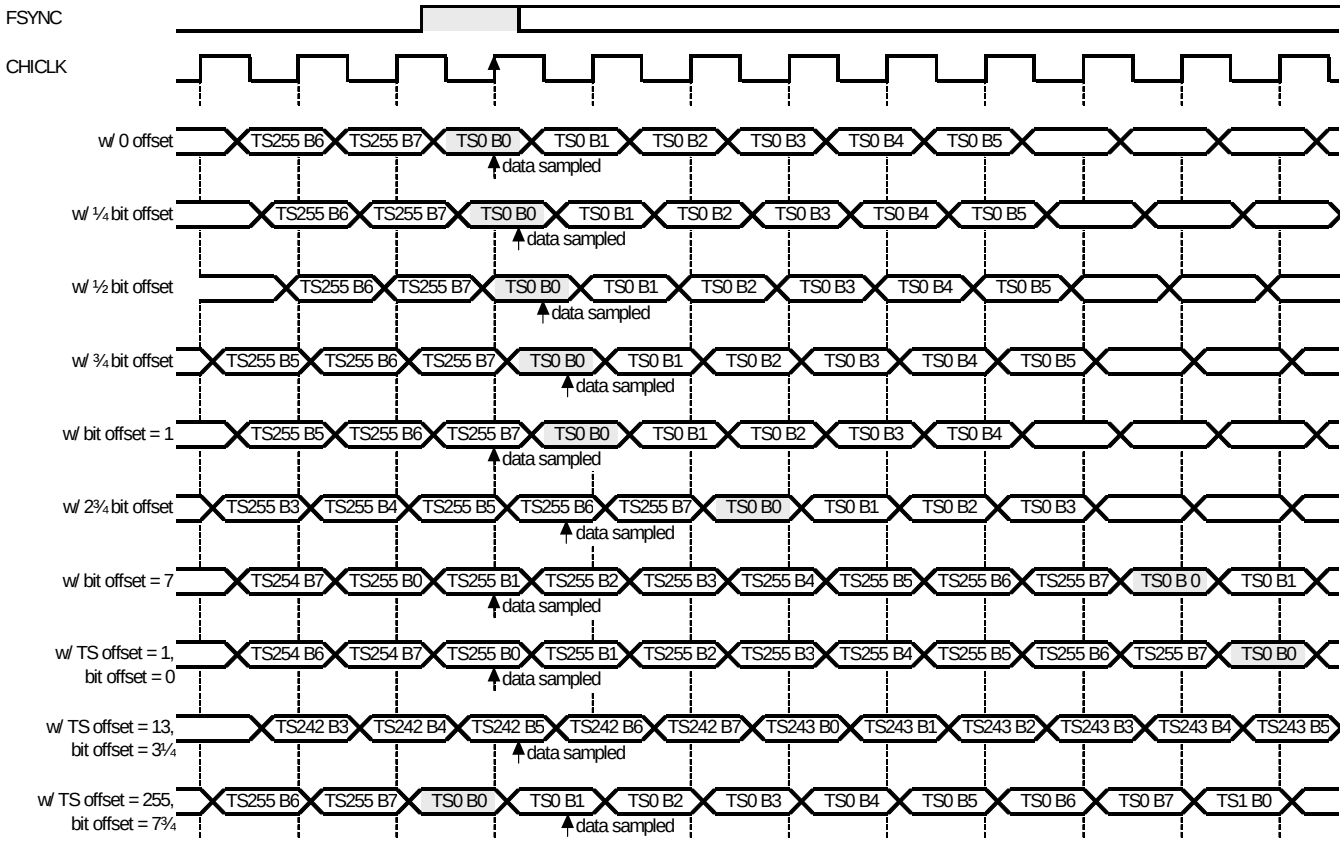
Parameter	Description	Min	Max	Unit
t_{13}	FSYNC Setup Time to Active CHICLK Edge	10	—	ns
t_{14}	FSYNC Hold Time from Active CHICLK Edge	5	—	ns
t_{15}	RXD Setup to Active CHICLK Edge	10	—	ns
t_{16}	RXD Hold Time from Active CHICLK Edge	5	—	ns
t_{17}	TXD High Z to Data Valid	—	15	ns
t_{18}	TXD Propagation Delay from Active CHICLK Edge	2	12	ns
t_{19}	Transmit Data High Impedance*	—	15	ns

* Applies if Driver_Enable_Control = 01; see Figure 17, CHI 3-State Output Control, if Driver_Enable_Control = 11.

All timing specifications are with respect to V_{IHmin} and V_{ILmax} as shown in Figure 5. All timing specifications also apply under the following conditions:

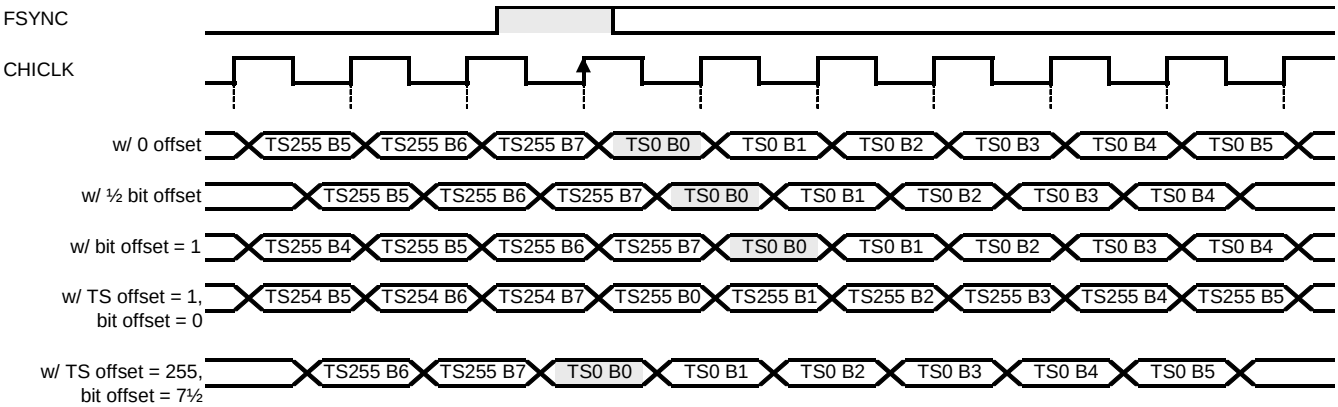
- If FS is active-low.
- If the falling edge of CHICLK is specified as the active edge.
- At all RXD and TXD rates (16.384 Mbits/s, 8.192 Mbits/s, 4.096 Mbits/s, or 2.048 Mbits/s) with a CHICLK frequency of 16.384 MHz or 8.192 MHz.

Timing Diagrams and ac Characteristics (continued)



Note: For this timing diagram, it is assumed that FSYNC has been programmed to be active-high, and to be sampled by the rising edge of the CHICLK.

Figure 7. Typical Receive CHI Timing with 16.384 Mbits/s Data and 16.384 MHz CHICLK

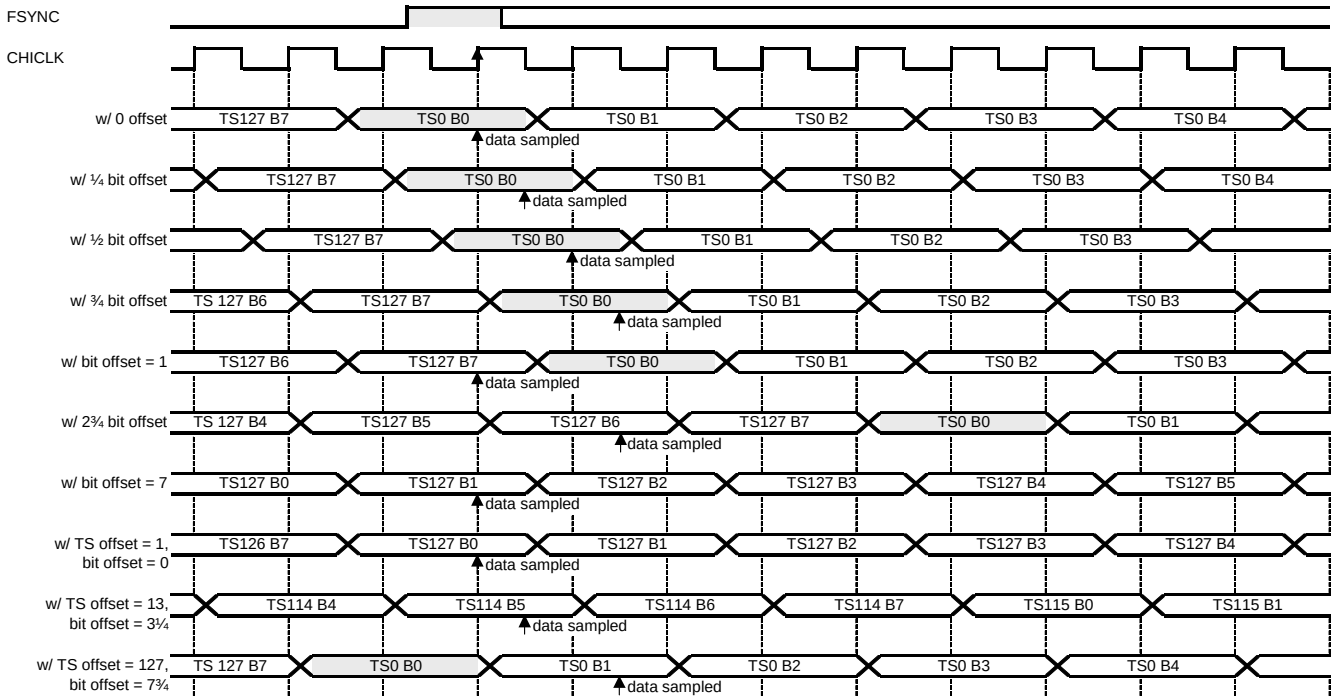


Notes:
1/4 bit offset not valid with 16 Mbits/s data.

For this timing diagram, it is assumed that FSYNC has been programmed to be active-high, and to be sampled by the rising edge of the CHICLK.

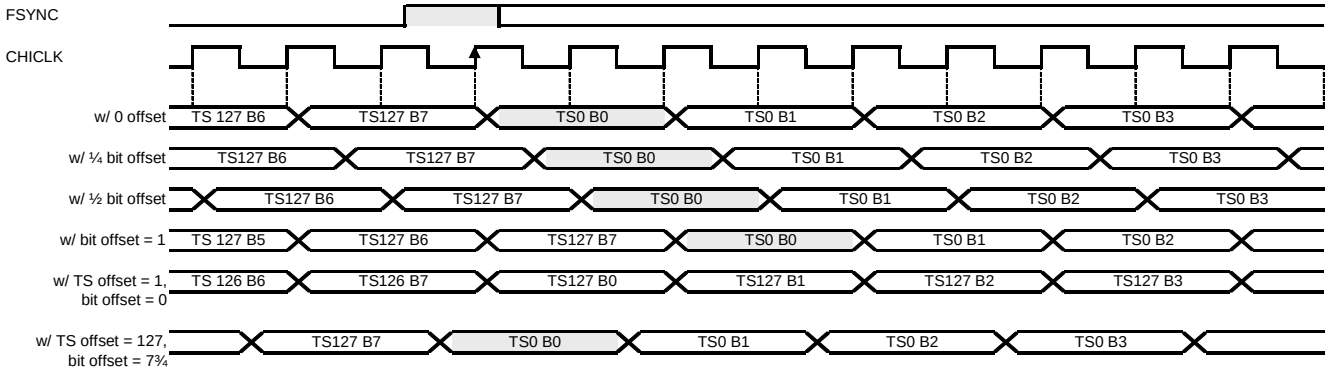
Figure 8. Transmit CHI Timing with 16.384 Mbits/s Data and 16.384 MHz CHICLK

Timing Diagrams and ac Characteristics (continued)



Note: For this timing diagram, it is assumed that FSYNC has been programmed to be active-high, and to be sampled by the rising edge of the CHICLK.

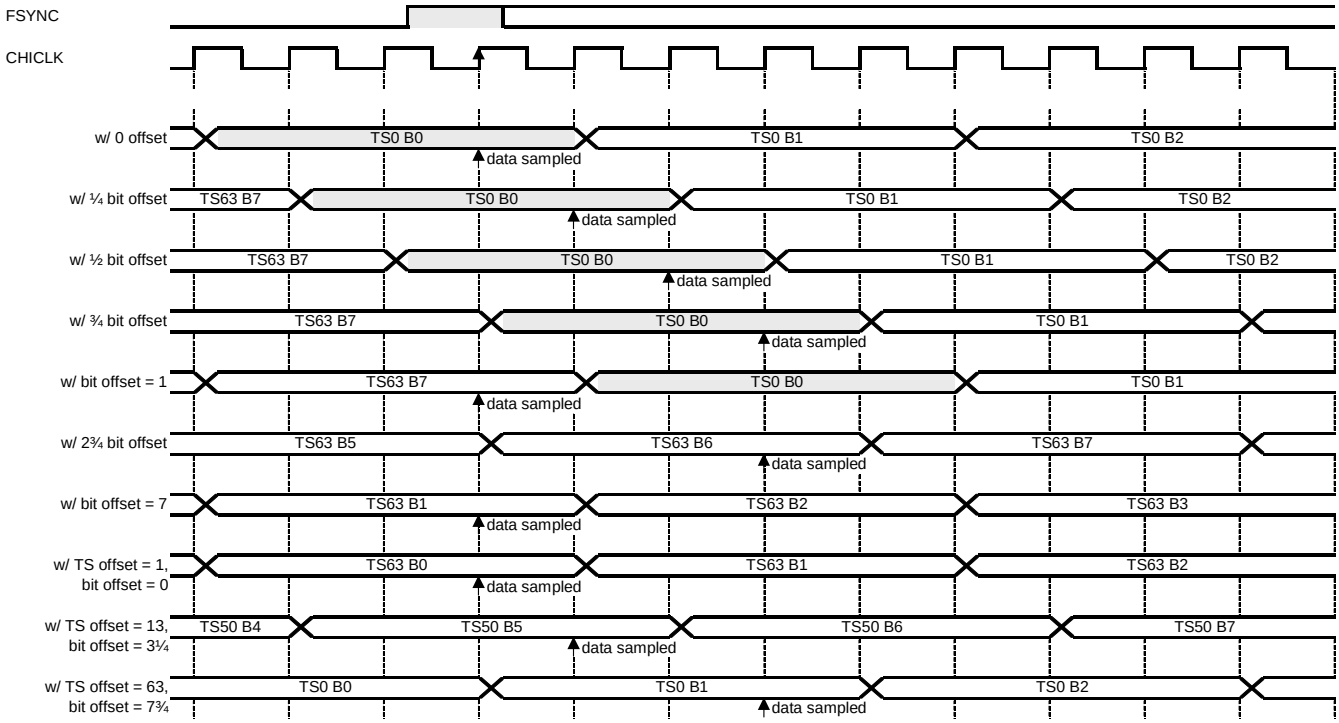
Figure 9. Typical Receive CHI Timing with 8.192 Mbits/s Data and 16.384 MHz CHICLK



Note: For this timing diagram, it is assumed that FSYNC has been programmed to be active-high, and to be sampled by the rising edge of the CHICLK.

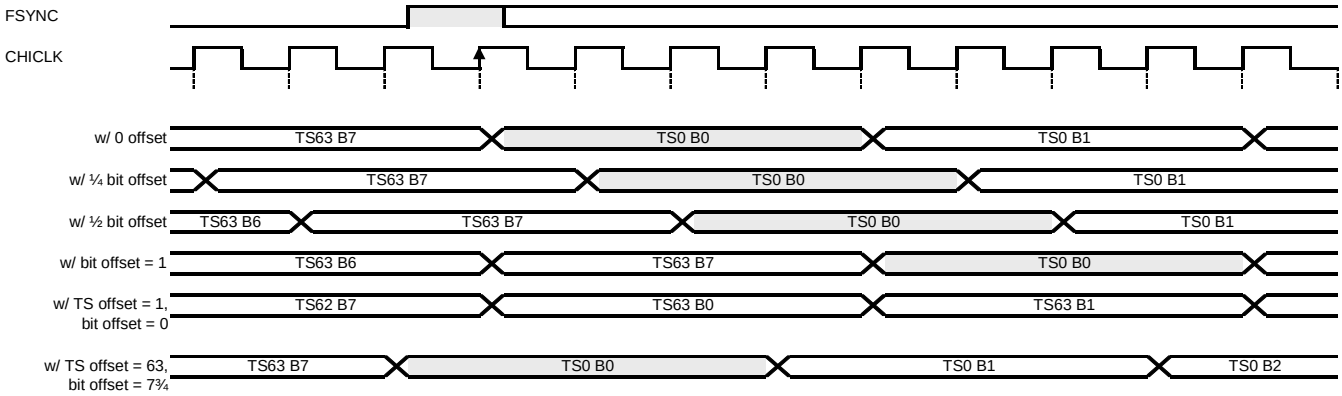
Figure 10. Transmit CHI Timing with 8.192 Mbits/s Data and 16.384 MHz CHICLK

Timing Diagrams and ac Characteristics (continued)



Note: For this timing diagram, it is assumed that FSYNC has been programmed to be active-high, and to be sampled by the rising edge of the CHICLK.

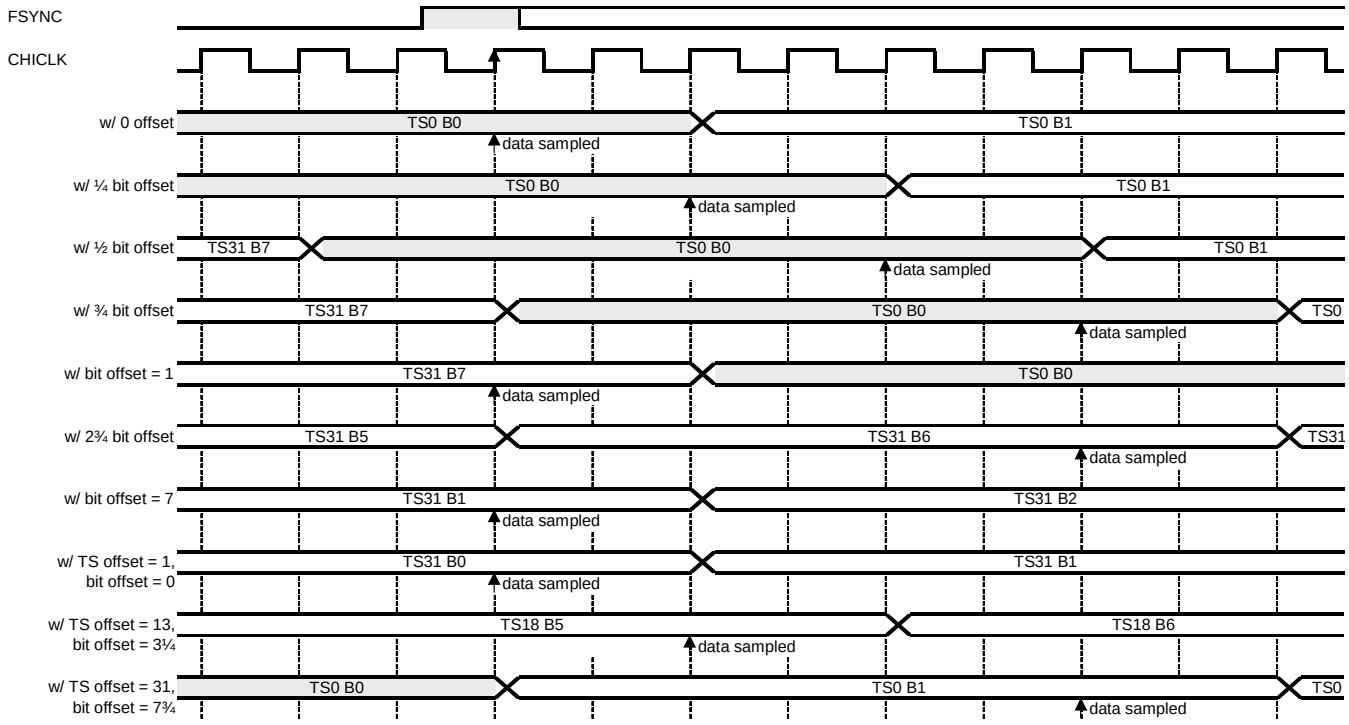
Figure 11. Typical Receive CHI Timing with 4.096 Mbits/s Data and 16.384 MHz CHICLK



Note: For this timing diagram, it is assumed that FSYNC has been programmed to be active-high, and to be sampled by the rising edge of the CHICLK.

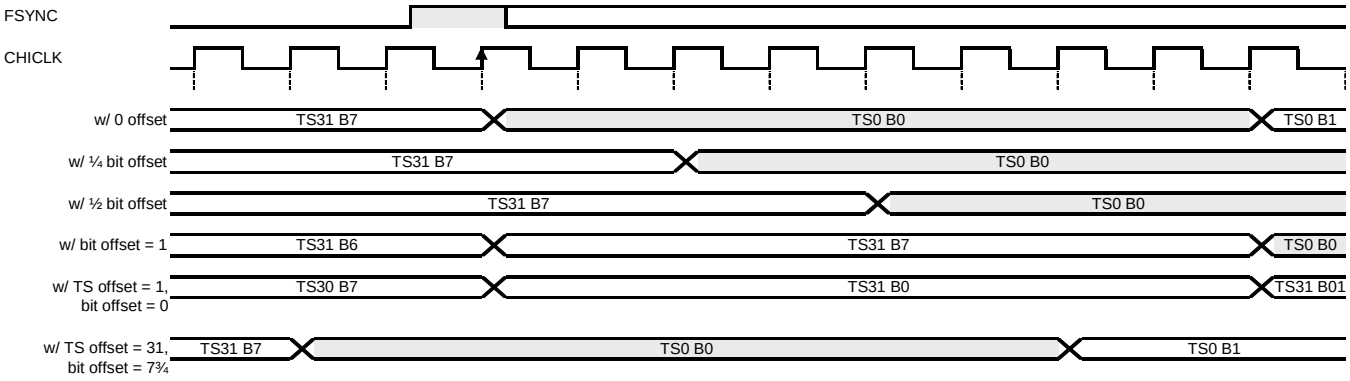
Figure 12. Transmit CHI Timing with 4.096 Mbits/s Data and 16.384 MHz CHICLK

Timing Diagrams and ac Characteristics (continued)



Note: For this timing diagram, it is assumed that FSYNC has been programmed to be active-high, and to be sampled by the rising edge of the CHICLK.

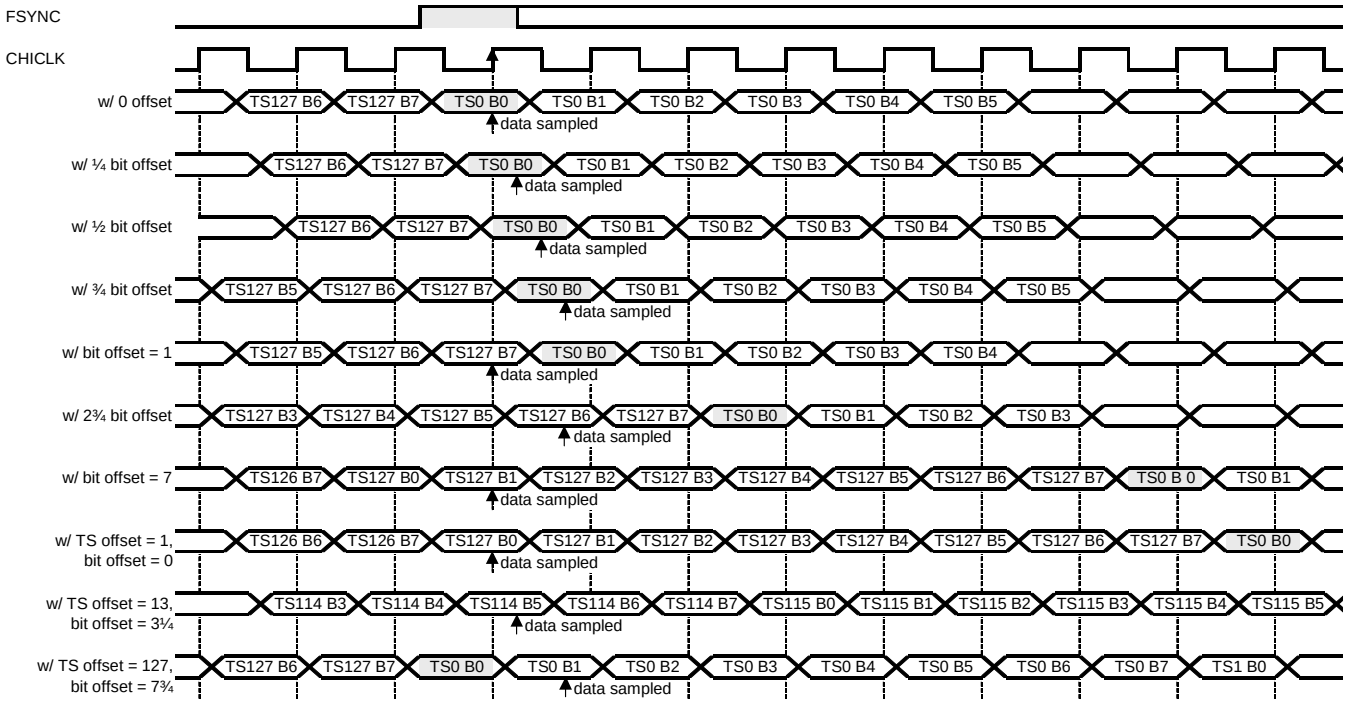
Figure 13. Typical Receive CHI Timing with 2.048 Mbits/s Data and 16.384 MHz CHICLK



Note: For this timing diagram, it is assumed that FSYNC has been programmed to be active-high, and to be sampled by the rising edge of the CHICLK.

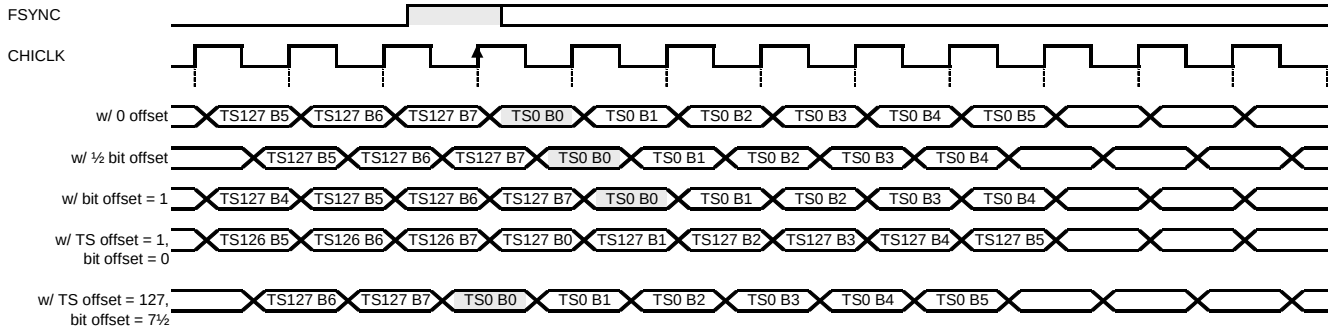
Figure 14. Transmit CHI Timing with 2.048 Mbits/s Data and 16.384 MHz CHICLK

Timing Diagrams and ac Characteristics (continued)



Note: For this timing diagram, it is assumed that FSYNC has been programmed to be active-high, and to be sampled by the rising edge of the CHICLK.

Figure 15. Typical Receive CHI Timing with 8.192 Mbits/s Data and 8.192 MHz CHICLK



Notes:
1/4 bit offset not valid with 8 MHz data and 8 MHz clock.

For this timing diagram, it is assumed that FSYNC has been programmed to be active-high, and to be sampled by the rising edge of the CHICLK.

Figure 16. Transmit CHI Timing with 8.192 Mbits/s Data and 8.192 MHz CHICLK

Timing Diagrams and ac Characteristics (continued)

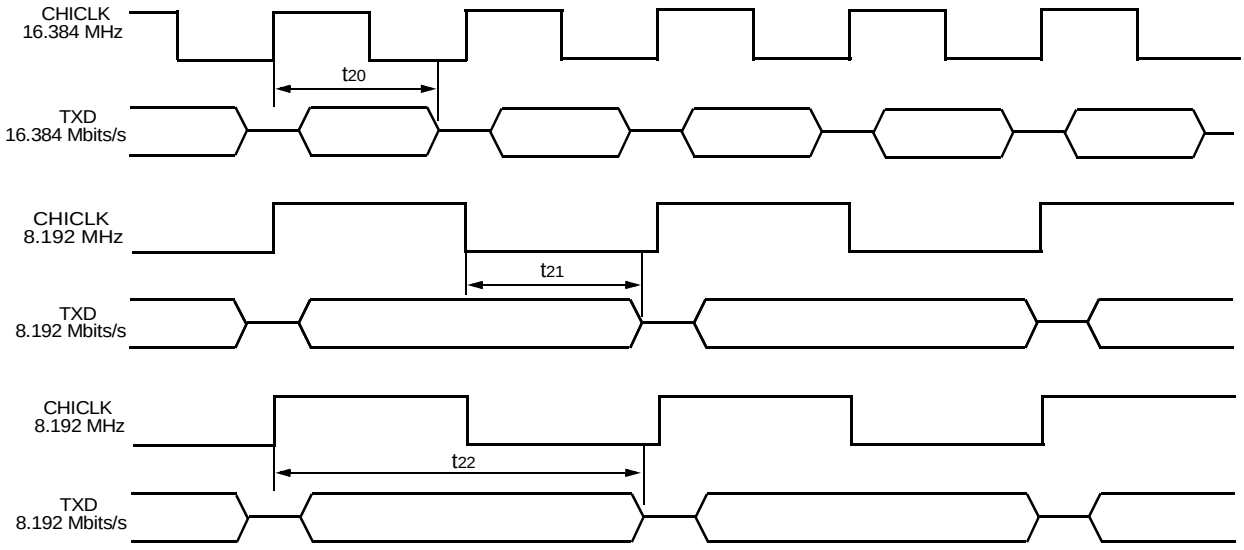


Figure 17. CHI 3-State Output Control

Table 26. CHI 3-State Output Control

Control in the table below refers to bits [6:4] in Transmit_CHI_Global_Configuration register (0x0C84). This only applies if bits 13 and 12 of the corresponding Transmit_CHI_Control register (0x0C00—0x0C7E) are set to 11. See STSI-144 Register Description.

Parameter	Control	Reference Point*	Min†	Max†	Unit
t20	000	After Previous Like Edge in 16 MHz	50	59	ns
	001	After Previous Like Edge in 16 MHz	44	53	ns
	010	After Previous Like Edge in 16 MHz	38	47	ns
	011	After Previous Like Edge in 16 MHz	32	41	ns
t21	000	After Previous Opposite Edge in 8 MHz	50	59	ns
	001	After Previous Opposite Edge in 8 MHz	44	53	ns
	010	After Previous Opposite Edge in 8 MHz	38	47	ns
	011	After Previous Opposite Edge in 8 MHz	32	41	ns
t22	100	After Previous Like Edge (8 MHz mode only)	111	120	ns
	101	After Previous Like Edge (8 MHz mode only)	105	114	ns
	110	After Previous Like Edge (8 MHz mode only)	99	108	ns
	111	After Previous Like Edge (8 MHz mode only)	93	102	ns

* Like edge is the reference edge (rising or falling) as defined by the Transmit_Clock_Edge bit in the Transmit_CHI_Global_Configuration (0x0C84) register. See STSI-144 Register Description document for further details.
† All timing specifications are with respect to the parameters shown in Figure 5.

Timing Diagrams and ac Characteristics (continued)

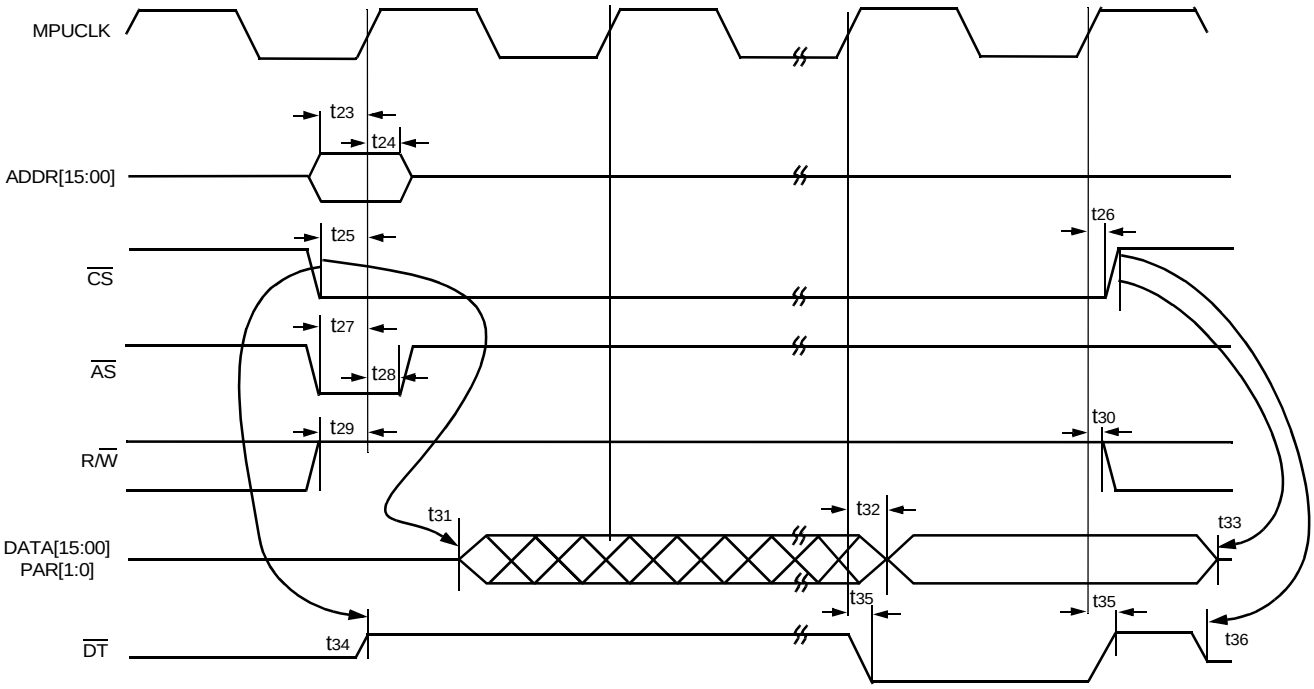


Figure 18. Microprocessor Port Timing—Read Cycle

Table 27. Microprocessor Port Timing—Read Cycle

Parameter	Description	Min*	Max*	Unit
t23	Address Setup	5	—	ns
t24	Address Hold	1	—	ns
t25	Chip Select Setup	5	—	ns
t26	Chip Select Hold	1	—	ns
t27	Address Strobe Setup	5	—	ns
t28	Address Strobe Hold	1	—	ns
t29	R/$\overline{W}$ Setup	5	—	ns
t30	R/$\overline{W}$ Hold	1	—	ns
t31	Data Output Enable	—	15	ns
t32	Data Clock to Valid	1	7	ns
t33	Data High Impedance	—	8	ns
t34	$\overline{DT}$ High Impedance to Valid	1	15	ns
t35	$\overline{DT}$ Clock to Out	1	7	ns
t36	$\overline{DT}$ Valid to High Impedance	1	8	ns

* All timing specifications are with respect to the parameters shown in Figure 5.

Timing Diagrams and ac Characteristics (continued)

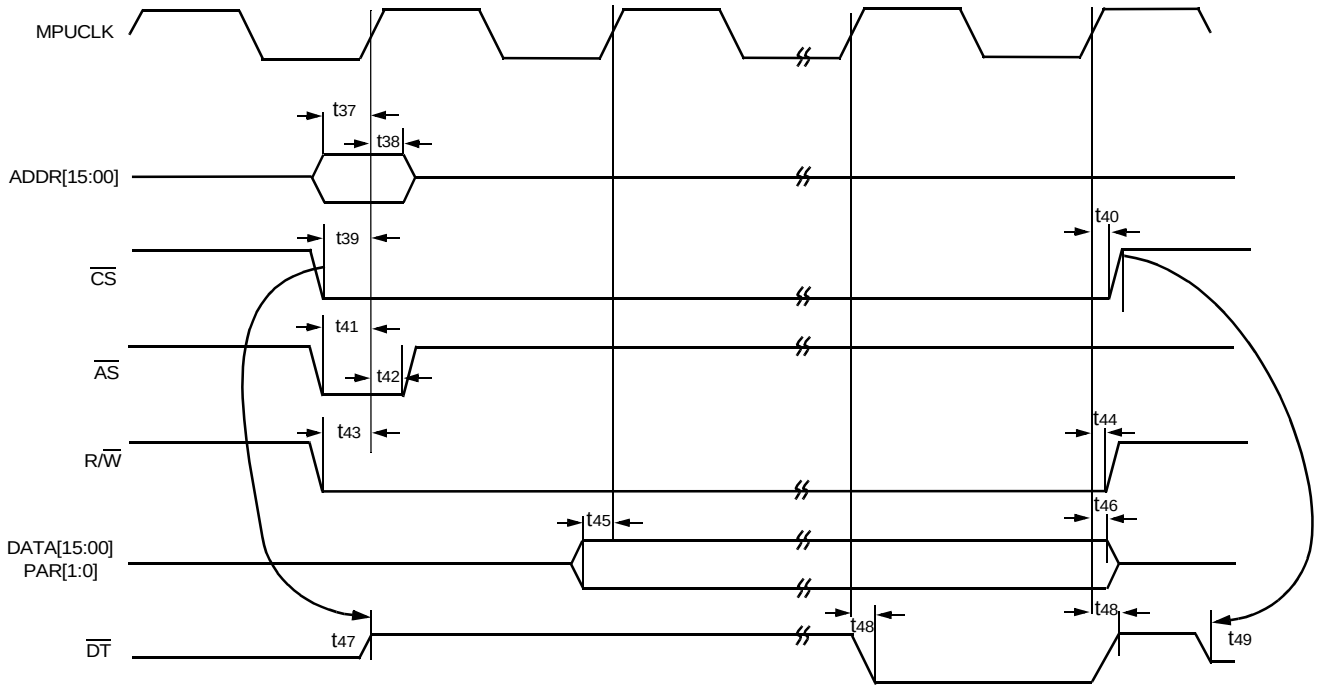


Figure 19. Microprocessor Port Timing—Write Cycle

Table 28. Microprocessor Port Timing—Write Cycle

Parameter	Description	Min*	Max*	Unit
t37	Address Setup	5	—	ns
t38	Address Hold	1	—	ns
t39	Chip Select Setup	5	—	ns
t40	Chip Select Hold	1	—	ns
t41	Address Strobe Setup	5	—	ns
t42	Address Strobe Hold	1	—	ns
t43	R/$\overline{W}$ Setup	5	—	ns
t44	R/$\overline{W}$ Hold	1	—	ns
t45	Data Setup	5	—	ns
t46	Data Hold	1	—	ns
t47	$\overline{DT}$ High Impedance to Valid	1	15	ns
t48	$\overline{DT}$ Clock to Out	1	7	ns
t49	$\overline{DT}$ Valid to High Impedance	1	8	ns

* All timing specifications are with respect to the parameters shown in Figure 5.

Note: Posted writes follow the same timing shown in Figure 19 and Table 28. A posted write may return a $\overline{DT}$ prior to the device completing the write cycle. This allows the microprocessor to continue operation while the STSI-144 completes the write.

Timing Diagrams and ac Characteristics (continued)

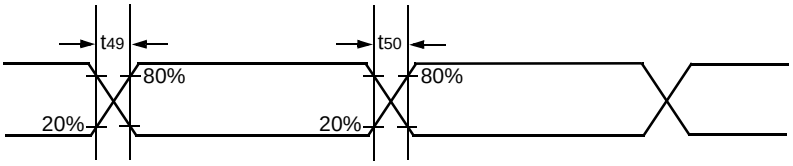


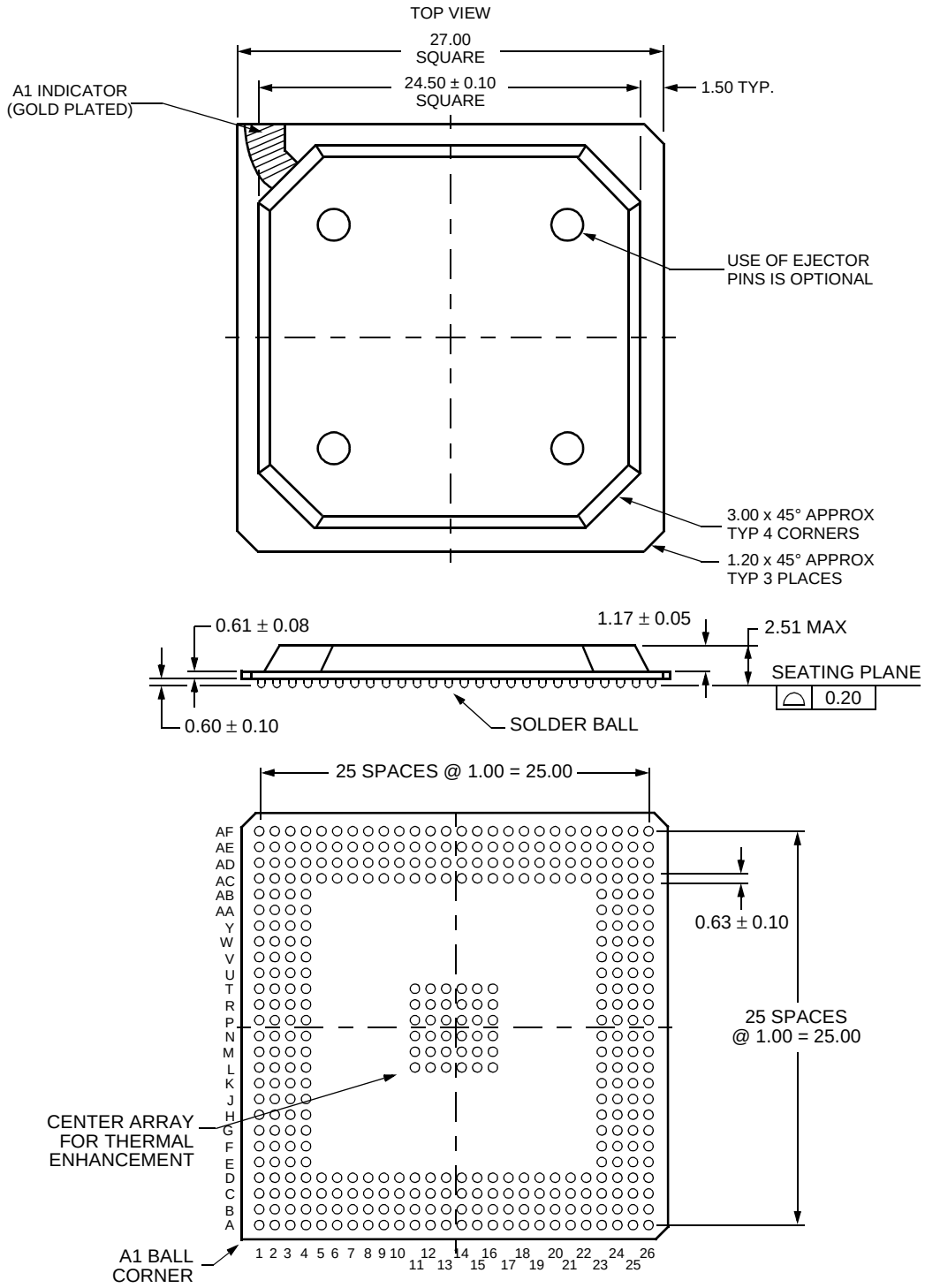
Figure 20. LVDS Output Timing Specifications

Table 29. LVDS ac Characteristics

Parameter	Symbol	Description	Conditions	Min	Typ	Max	Unit
t_{49}	t_R	V_{OD} Rise Time, 20% to 80%	Z_L = 100 Ω ± 1%, C_P = 3.0 pF, C_N = 3.0 pF	100	—	210	ps
t_{50}	t_F	V_{OD} Fall Time, 80% to 20%	Z_L = 100 Ω ± 1%, C_P = 3.0 pF, C_N = 3.0 pF	100	—	210	ps

Outline Diagrams

Dimensions are in millimeters.



Ordering Information

Device	Part Number	Ball Count	Package	Comcode
STSI-144	TTSI144641BL-1	388	PBGAM1T	109101899

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