M54973P

BI-CMOS 8-BIT PARALLEL-INPUT, LATCHED DRIVER

DESCRIPTION

The M54973P is a semiconductor integrated circuit consisting of eight CMOS latches and bipolar output drivers product by a Bi-CMOS process.

FEATURES

- Enable input provides output control
- Low supply current (standby current $I_{CC} \leqq 10\mu A$)
- Input level is compatible with typical CMOS
- Driver features : High withstand voltage ($BV_{CEO} \geqq 30V$)
  Capable of large drive currents ($I_{O\,(max)} = 300mA$)
- Wide operating temperrature range $T_a = -20 \sim +75°C$

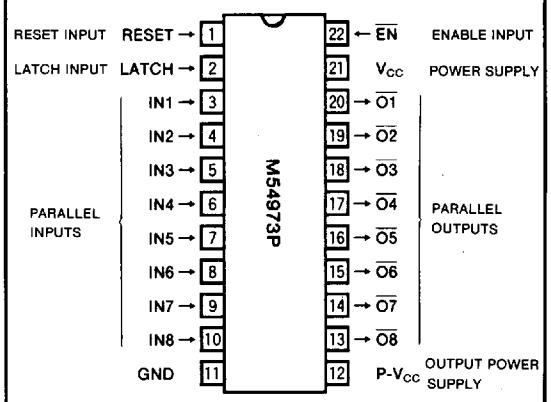
APPLICATION

Dot driver for thermal print heads. Drivers for relays, and solenoids.

FUNCTION

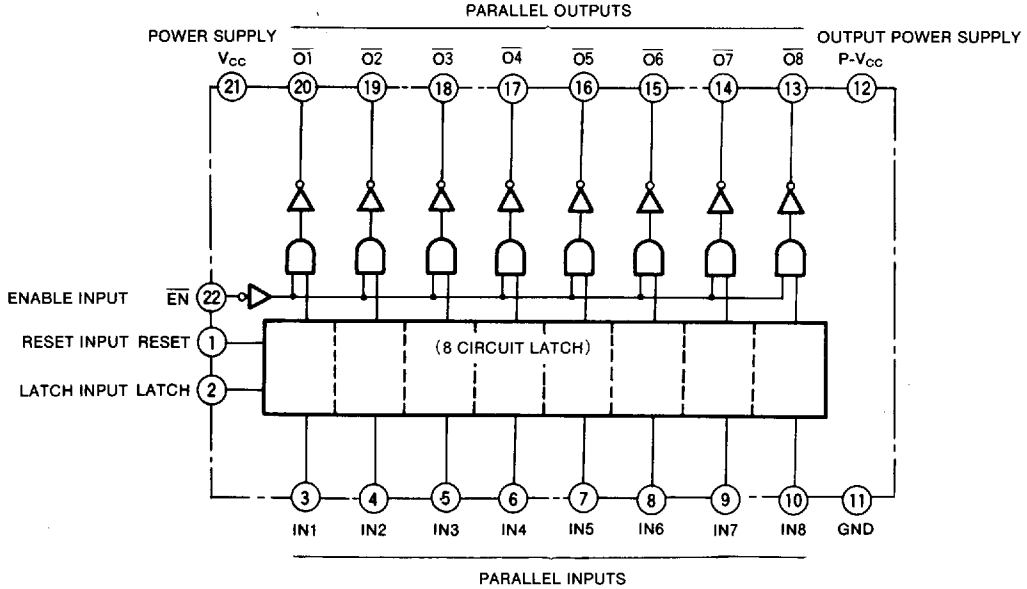
Data are applied to inputs IN1 through IN8. When the LATCH input is set high, the data is latched as shown in the truth table. A high-level signal applied to the RESET input causes the latches to remain open (reset). When the EN input is set low, high data stored in the latches turn on the corresponding outputs and set them low.
When the LATCH and RESET inputs are both low, the latch retains the stored data, irrespective of inputs IN1 through IN8.

PIN CONFIGURATION (TOP VIEW)



Outline 22P4

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

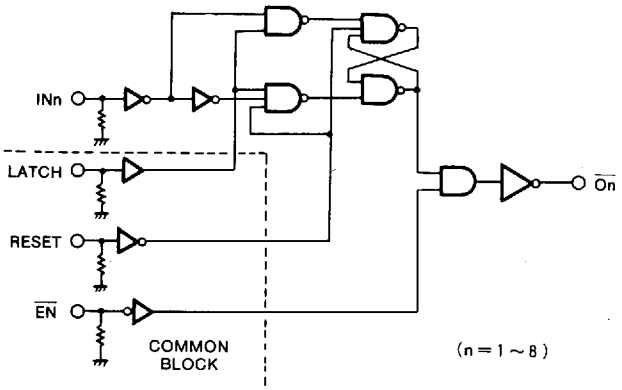
BI-CMOS 8-BIT PARALLEL-INPUT, LATCHED DRIVER

TRUTH TABLE

Inputs				Outputs $\overline{On}$	
INn	LATCH	RESET	$\overline{EN}$	t-1	t
L	H	L	L	X	H
H	H	L	L	X	L
X	X	H	X	X	H
X	X	X	H	X	H
X	L	L	L	L	L
X	L	L	L	H	H

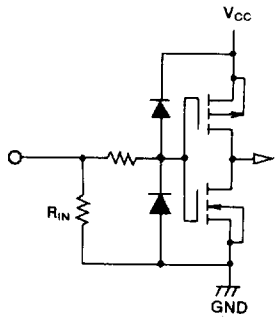
L = low level
H = high level
X = irrelevant
t-1 = previous state
t = current state
Off state when output is high
On state when output is low

LOGIC DIAGRAM (ONE CIRCUIT)

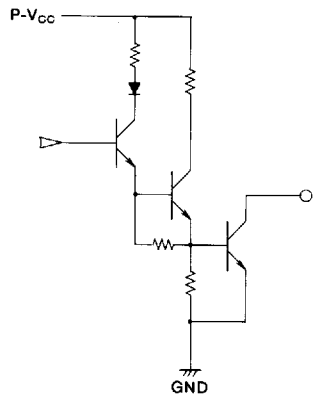


I/O EQUIVALENT CIRCUIT

1 Input circuit (INn, LATCH, RESET, $\overline{EN}$)



2 Output circuit (parallel output On)



BI-CMOS 8-BIT PARALLEL-INPUT, LATCHED DRIVER

ABSOLUTE MAXIMUM RATINGS (T_a=20～+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～+8	V
V_I	Input voltage		−0.5～V_{CC}+0.5	V
V_O	Output voltage	Transistor off	−0.5～+30	V
I_O	Output current	Transistor on	200	mA
P_d	Power dissipation	T_a=25℃	1.42	W
Topr	Operating temperature		−20～+75	℃
Tstg	Storage temperature		−55～+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20～+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	5	6	V
P-V_{CC}	Output spply voltage		4.5	5	7	V
V_O	Applied output voltage	Transistor off			30	V
I_O	Output current per circuit	All outputs on simultaneously Duty cycle 80% max			120	mA

ELECTRICAL CHARACTERISTICS (T_a=+25℃, V_{CC}=5V, P-V_{CC}=5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage	T_a=−20～+75℃	0.7V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.3V_{CC}	V
R_{IN}	Input resistance		50			kΩ
V_{OL1}	Low-level output voltage	I_{OL}=120mA			0.4	V
V_{OL2}		I_{OL}=200mA			0.5	V
I_{OLK}	Output leakage current	V_O=30V			50	μA
I_{CC1}	Supply current	All inputs=0V, all outputs off			10	μA
I_{CC2}		One output circuit on			0.2	mA
I_{CC3}	Output supply current	All inputs open, all outputs off			10	μA
I_{CC4}		One output circuit on			14	mA

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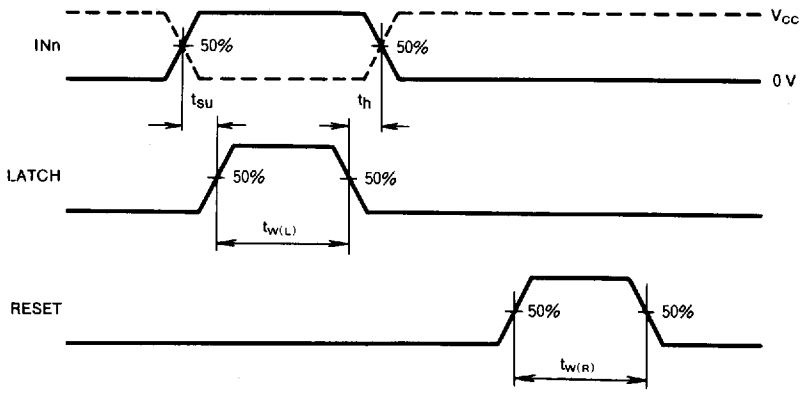
TIMING REQUIREMENTS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(L)}$	Latch pulse width		0.1			μs
$t_{w(R)}$	Reset pulse width		0.1			μs
t_{su}	Data setup time		0			μs
t_h	Data hold time		0.1			μs

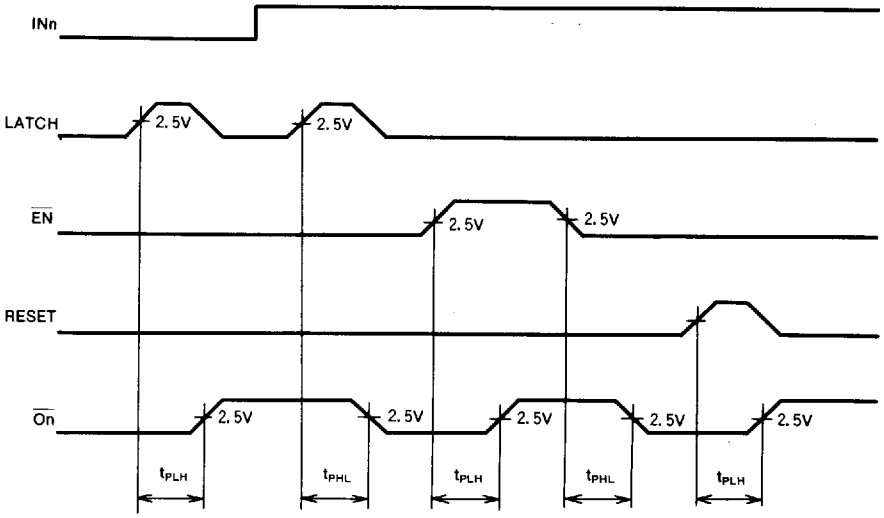
TIMING DIAGRAM



SWITCHING CHARACTERISTICS (T_a=+25℃, V_{CC}=5V)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to high-level output propagation time (Input LATCH to output $\overline{On}$)	V_{IH} = 5 V, V_{IL} = 0 V, R_L = 100Ω, C_L = 15pF (Note 1)		(0.6)	2	μs
t_{PHL}	High-to low-level output propagation time (Input LATCH to output $\overline{On}$)			(0.1)	0.5	μs
t_{PLH}	Low-to high-level output propagation time (Input $\overline{EN}$ to output $\overline{On}$)			(0.6)	2	μs
t_{PHL}	High-to low-level output propagation time (Input $\overline{EN}$ to output $\overline{On}$)			(0.1)	0.5	μs
t_{PLH}	Low-to high-level output propagation time (Input RESET to output $\overline{On}$)			(0.6)	2	μs

TIMING DIAGRAM



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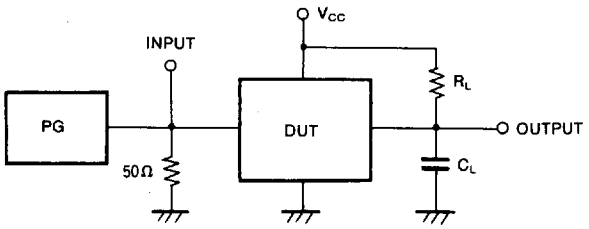
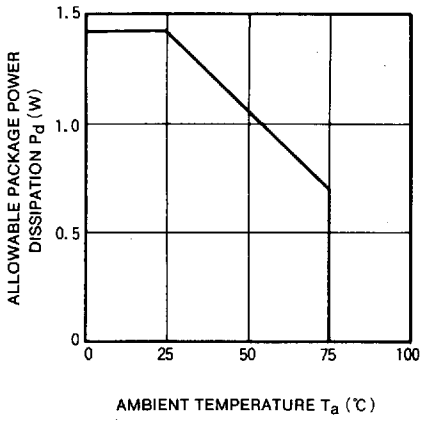
TEST CIRCUIT



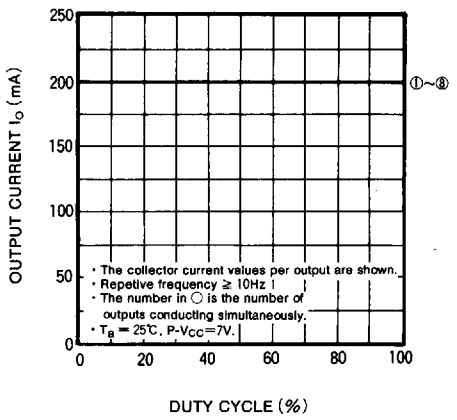
- The input waveform has the characteristics of $t_r \leq 20$ns and $t_f \leq 20$ns
- The capacitance C_L includes stray wiring capacitance and probe input capacitance.

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION



ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE



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