MFR62340A-J

Parallel Fiber Receiver

Data sheet

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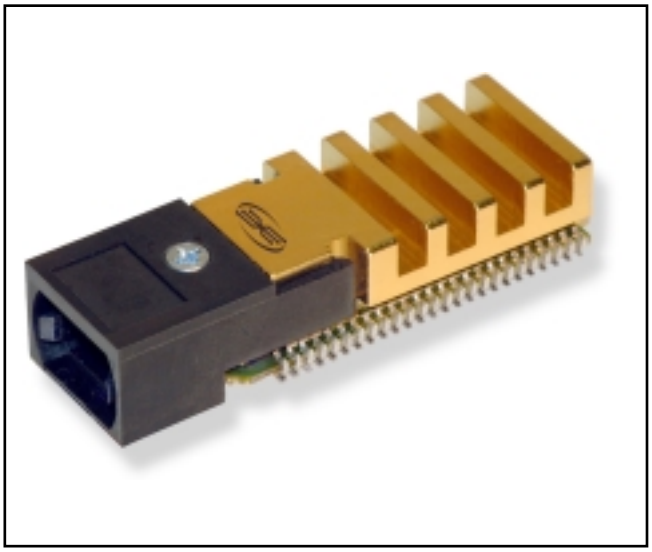

Ordering Information

MFR62340A-J	MPO/MTP Connector

Features

- Data rate 155Mbps to 2.5Gbps per channel
- 12 parallel channels, total 30Gbps capacity
- Differential CML (Current-Mode Logic) interface
- Link length up to 100m (with 400MHz·km fiber)
- Channel BER 10^{-12} when used with MFT62340A-J
- Designed for multimode fiber ribbon
- MPO/MTP™ connector
- Surface-mount package
- Pick-and-placeable; reflow solderable
- Matches the MFT62340A-J Transmitter

Applications

- High-speed interconnects within and between Switches, Routers and Transport equipment
- Proprietary backplanes
- Low cost OC-192 VSR (Very Short Reach) connections
- InfiniBand™ connections
- Interconnects rack-to-rack, shelf-to-shelf, board-to-board, board-to-optical backplane

Description

The MFT62340A-J and MFR62340A-J make a very high speed transmitter and receiver pair for parallel fiber applications. This pair, coupled through a multimode parallel fiber ribbon cable, constitutes a complete parallel fiber link. These links provide high-speed interconnects for use within and between large capacity switches, routers and data transport equipment. The transmitter and receiver have a differential CML interface and MPO/MTP connector.

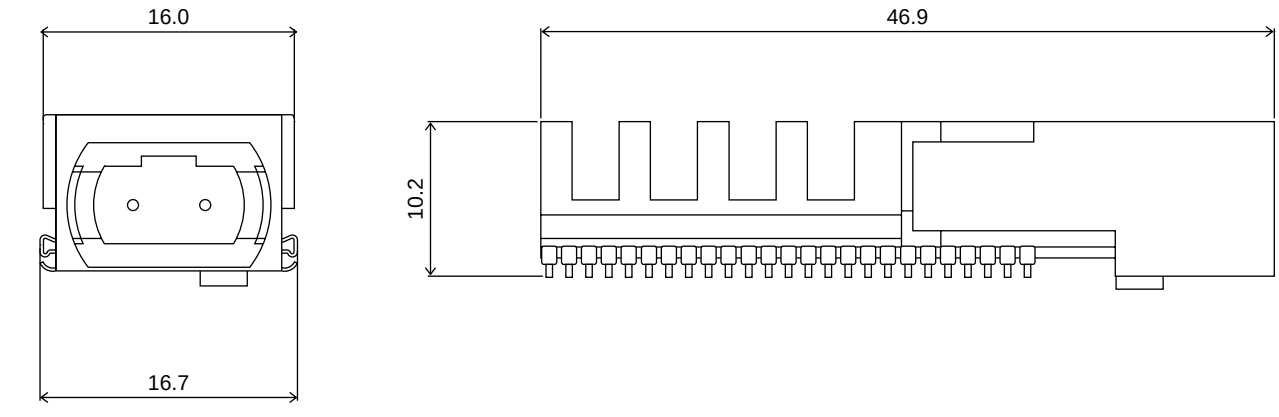

Figure 1 - MFR62340A-JO: MPO/MTP Connector

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Absolute Maximum Ratings (note 1)

	Parameter	Symbol	Min	Max	Unit
1	Supply voltage	V_{CC}	-0.5	4.0	V
2	Voltage on any pin	V_{PIN}	-0.5	V_{CC}+0.3	V
3	Operating and storage moisture	M_{OS}	20	85	%
4	Storage temperature	T_{STG}	-40	+100	°C
5	ESD resistance all I/O (note 2)	V_E	-200	200	V

Recommended Operating Conditions (note 3)

	Parameter	Symbol	Min	Max	Unit
1	Case temperature (note 4, fig. 6)	T_{CASE}	0	80	°C
2	Supply voltage (note 5)	V_{CC}	3.3-5%	3.3+5%	V
3	Data rate per channel	f_D	0.155	2.5	Gbps
4	Optical wavelength	λ	830	860	nm
5	CML differential load impedance (Fig. 4)	Z_O	80	120	Ω
6	Power supply noise (1MHz to 2GHz)	V_{NPS}		100	mV_{p-p}

Note 1: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
Note 2: Human body model.
Note 3: Data patterns are to have maximum run lengths and DC balance shifts no worse than those of a Pseudo Random Bit Sequence of length 2^{23}-1 (PRBS-23).
Note 4: An air flow parallel to the PCB, and parallel with the module's heatsink flanges, is recommended. See figure 6 and figure 7 for information about ambient temperature vs. air flow.
Note 5: The heat sink of the module is at Vcc potential. Take care to avoid shortcircuits with other components.

Characteristics (note 1)

	Parameter		Symbol	Min	Typ	Max	Unit
1	Power consumption (0.155 to 2.5 Gbps)		P_D			2.4	W
2	Power supply current		I_{CC}			760	mA
3	Saturation (average power)		P_{SAT}	-2			dBm
4	Sensitivity (note 2, 3)		P_{S12}			-12	dBm
5	Stressed receiver sensitivity (note 4)		P_{SS}			-9.5	dBm
6	Stressed receiver eye opening (note 5)		P_{SE}	120			ps
7	Jitter	Total (note 6)	TJ			153	ps_{p-p}
8	Contribution	Deterministic (note 7)	DJ			46	ps_{p-p}
9	CML differential output rise/fall time (20-80%, Fig. 5)		t_{RC}, t_{FC}			160	ps
10	CML differential output voltage (Fig. 3,4,5)		V_{OCML}	250	350	450	mV
11	CML differential output reflection coefficient		S_{22}			-5	dB
12	Channel skew (note 8)		t_{SK}			175	ps
13	Return Loss (note 9)		RL	12			dB
14	NMOS output voltage	Low (I_{sink} = 3mA)	V_{LNMOS}			0.4	V
15		High	V_{HNMOS}	2.4			V
16	Receiver Signal Detect (RX_SD) (note 10)	Assert level	P_{AS}			-15.5	dBm
17		De-assert level	P_{DS}	-31			dBm
18		Hysteresis	P_{AS}-P_{DS}	0.5			dBm
19		Assert time (fig. 7)	T_{AS}			10	µs
20		De-assert time (fig. 7)	T_{DS}			10	µs

Note 1: Operating conditions are as per Recommended Operating Conditions. Test pattern PRBS-23 at 2.5Gbps with 50/125µm fiber, unless otherwise specified.

Note 2: Sensitivity for a channel (as defined in IEEE 802.3 (2000 Edition) Gigabit Ethernet specification) is specified at a BER of 10^{-12} using a fast rise/ fall time source with low RIN and Extinction Ratio not less than 6 dB. All channels not under test are receiving signals with an average input power of 6 dB, or higher, above worst case sensitivity.

Note 3: $P_{average}$ = -12dBm and ER = 6dB yields an OMA of 0.076mW.

Note 4: The stressed receiver sensitivity is measured using 0.5 dB Inter-Symbol Interference, ISI, (min), 33 ps Duty Cycle Dependent Deterministic Jitter, DCD DJ (min) and 6 dB ER (ER Penalty = 2.2 dB). All channels not under test are receiving signals with an average input power of 6 dB, or higher, above worst case sensitivity.

Note 5: The stressed receiver eye opening represents the eye at TP4 as defined in IEEE 802.3 Clause 38.5. The stressed receiver eye opening is measured using 0.5 dB ISI (min), 33 ps DCD DJ (min), 6 dB ER (ER Penalty=2.2 dB) and an average input optical power of -9.0 dBm (0.5 dB above Minimum Stressed Receiver Sensitivity as defined in IEEE 802.3 Clause 38.5). All channels not under test are receiving signals with an average input power of 6 dB or higher, above worst case sensitivity.

Note 6: Total Jitter, TJ equals TP3 to TP4 as defined in IEEE 802.3 Gigabit Ethernet Specification Clause 38.5. Total jitter is specified at a BER of 10^{-12} (TJ=DJ+RJx2Q, where Q=7 for BER 10^{-12} and RJ=Random Jitter).

Note 7: Deterministic jitter includes duty cycle distortion.

Note 8: Electrical channel skew is measured with the input signals having equal amplitude and no input optical channel skew.

Note 9: Return loss is the ratio between received optical power and optical power reflected back into the fiber.

Note 10: All channels not under test are receiving signals with an average input power of 6 dB, or higher, above the channel under test.

Cleaning the Optical Interface

A protective connector plug is supplied with each module. This plug should remain in place prior to use, and be re-attached whenever a fiber cable is not inserted. This will keep the optical interface free from dust or other contaminants, which may potentially degrade the optical signal. Before re-attaching the connector plug to the module, visually inspect the plug and remove any contamination. If the optical interface becomes contaminated, it can be cleaned with high-pressure nitrogen. Liquids or physical contact with the optical interface are not advised due to potential damage.

Assembly on Printed Circuit Board

The module can be soldered by hand or by a reflow process.

- For hand soldering, a soldering iron with its tip connected to ground should be used. Solder extractors, including replacement parts, should be of the non-static generating type.
- For reflow soldering, the recommendations advised by Zarlink in the technical note “MFTN6005A Manufacturing Guidelines” should be followed. This document provides guidelines about choice of solder, reflow temperature and time profile etc.

Use of solder with no-clean flux, i.e. solder that does not require washing after assembly, is recommended. Washing the module with any kind of liquid is not advised due to potential damage.

Electrostatic Discharge (ESD)

The module is classified as Class 1 according to MIL-STD-883, test method 3015. When handling the modules, precautions for ESD sensitive devices should be taken. These precautions include use of ESD protected work areas with wrist straps, controlled work benches, floors etc. The recommendations advised by Zarlink in the technical note "MFTN6005A Manufacturing Guidelines" should be followed.

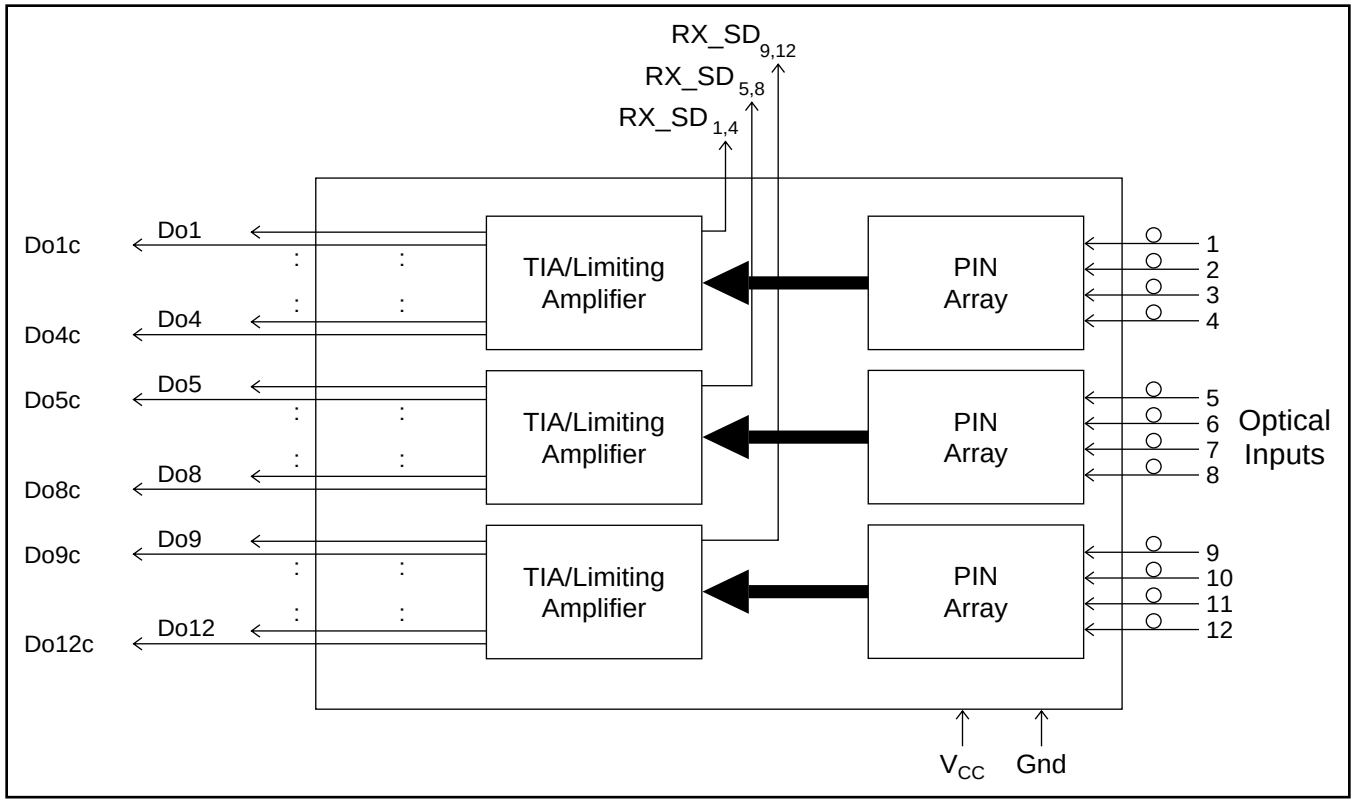


Figure 2 - Block Diagram

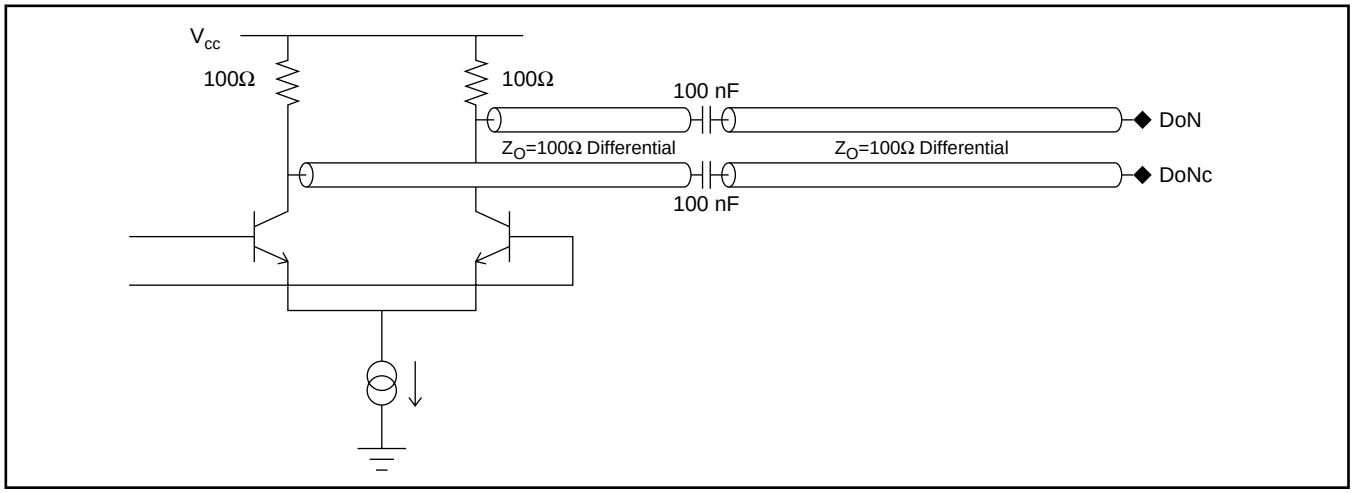


Figure 3 - Data Output Equivalent Circuit

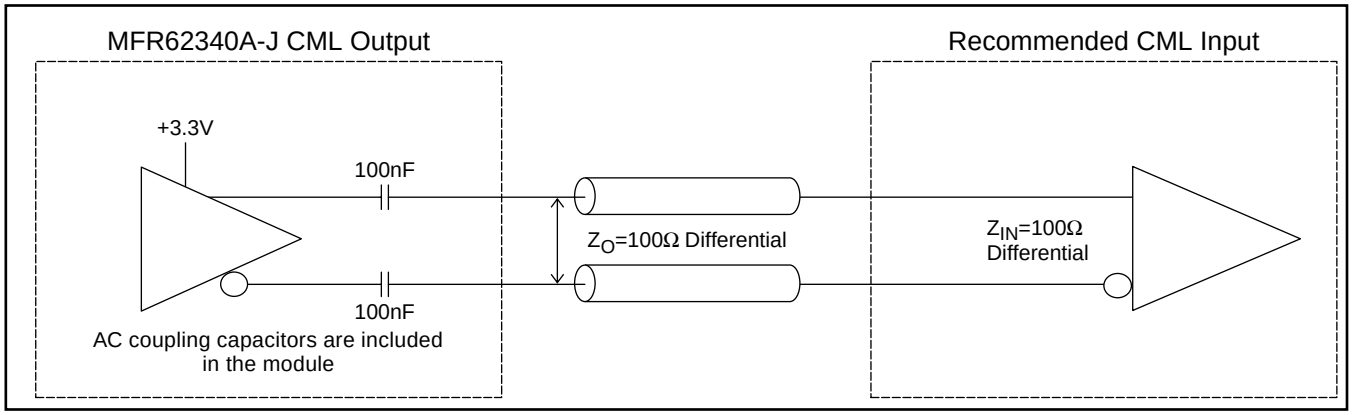


Figure 4 - Differential CML Interface

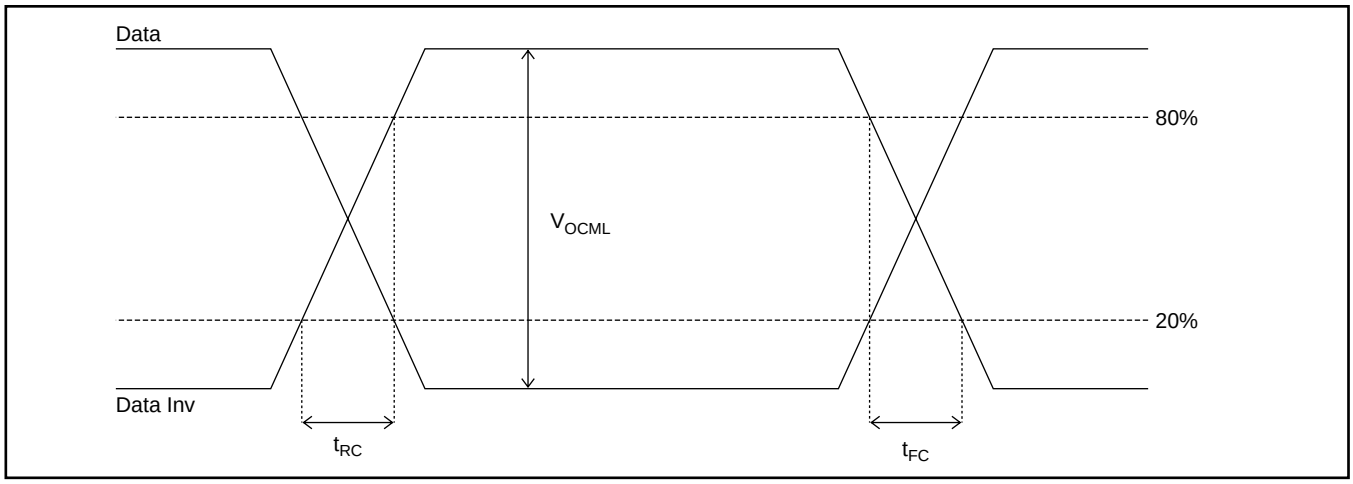


Figure 5 - CML Differential Signals

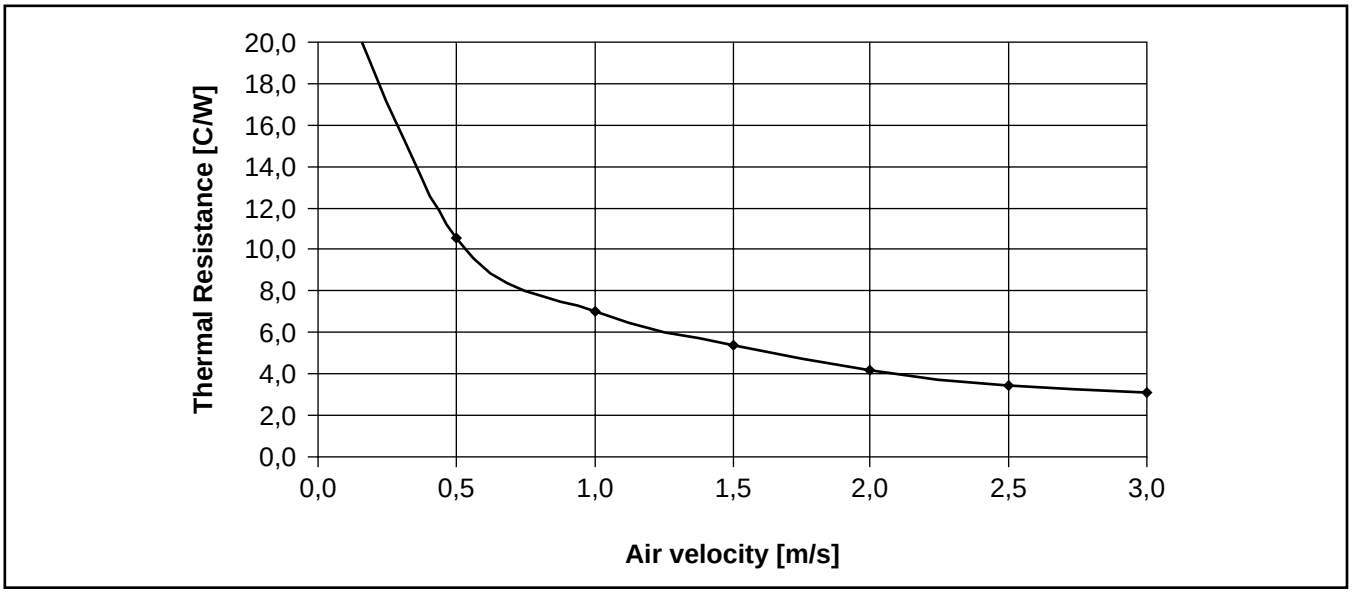


Figure 6 - Typical thermal resistance vs. flowing ambient air velocity

Note 1: These data correspond to a single module placed on a thermally insulating board and air velocity measured approximately 1cm above the board and 0.5cm in front of the module. The airflow is parallel to the flanges of the heat sink (100 LFM (linear feet per minute) =0.51m/s)

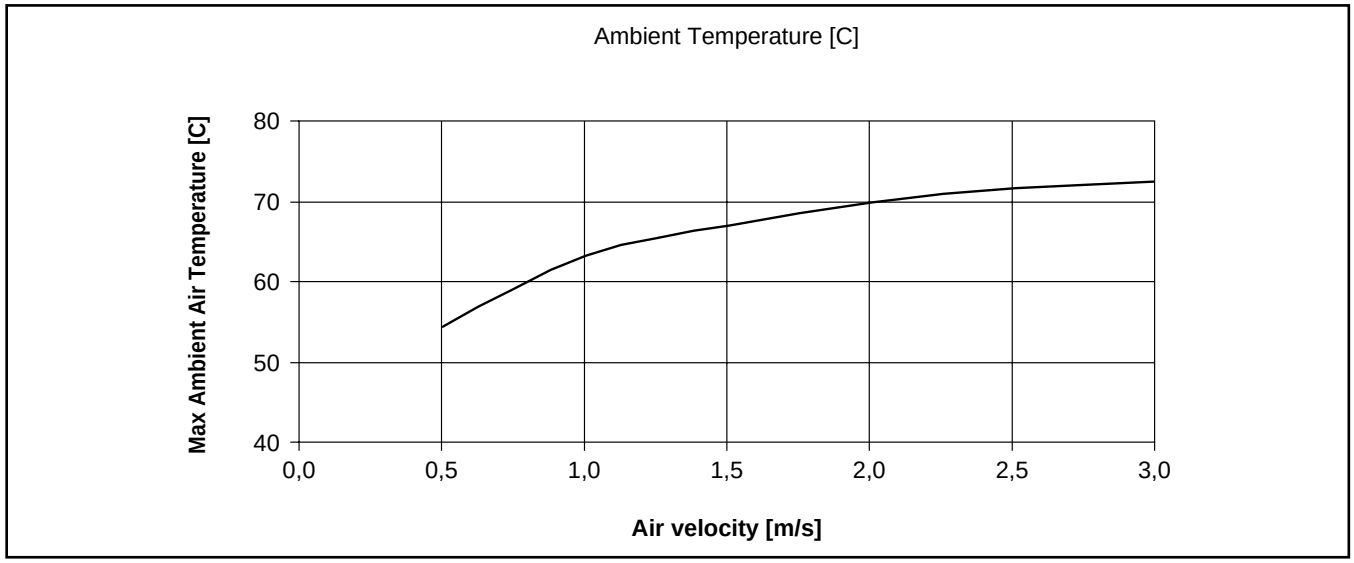


Figure 7 - Typical required air temperature to keep the module temperature below 80˚C. The line correspond to a heat dissipation of 2.4 Watt (worst case).

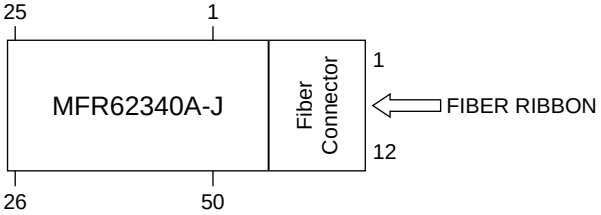


Figure 8 - Pin Assignment (Top View)

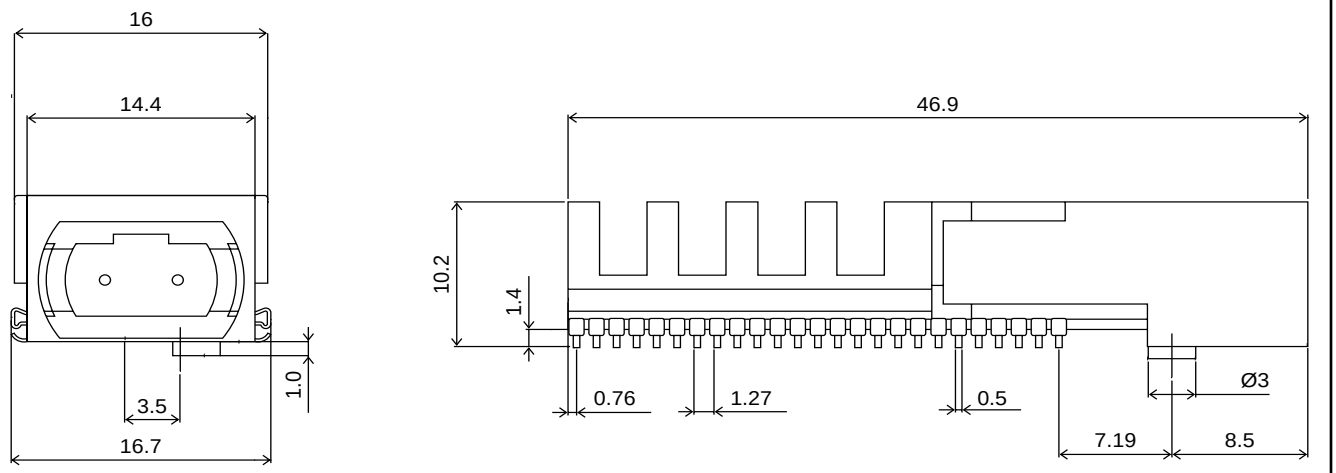
Pin Description

No	Name	Logic	Description
1	Gnd		Ground
2	V_{CC}		Positive power supply
3	V_{CC}		Positive power supply
4	$RX\_SD_{1,4}$	NMOS	Receiver Signal Detect channels 1 and 4 (channels 2 and 3 are not monitored). High = Signal detected. Low = No signal detected. Open drain with internal pull-up resistor 40kΩ (note 1).
5	$RX\_SD_{5,8}$	NMOS	Receiver Signal Detect channels 5 and 8 (Channels 6 and 7 are not monitored). High = Signal detected. Low = No signal detected. Open drain with internal pull-up resistor 40kΩ (note 1).
6	$RX\_SD_{9,12}$	NMOS	Receiver Signal Detect channels 9 and 12 (channels 10 and 11 are not monitored). High = Signal detected. Low = No signal detected. Open drain with internal pull-up resistor 40kΩ (note 1).
7	Gnd		Ground
8	Do1	CML	Data output No 1.
9	Do1c	CML	Data output No 1, inv
10	Gnd		Ground
11	Do2	CML	Data output No 2.
12	Do2c	CML	Data output No 2, inv.
13	Gnd		Ground
14	Do3	CML	Data output No 3.
15	Do3c	CML	Data output No 3, inv.
16	Gnd		Ground
17	Do4	CML	Data output No 4.
18	Do4c	CML	Data output No 4, inv.
19	Gnd		Ground
20	Do5	CML	Data output No 5.
21	Do5c	CML	Data output No 5, inv.
22	Gnd		Ground
23	Do6	CML	Data output No 6.
24	Do6c	CML	Data output No 6, inv.
25	Gnd		Ground

No	Name	Logic	Description
26	Gnd		Ground
27	Do7	CML	Data output No 7.
28	Do7c	CML	Data output No 7, inv.
29	Gnd		Ground
30	Do8	CML	Data output No 8.
31	Do8c	CML	Data output No 8, inv.
32	Gnd		Ground
33	Do9	CML	Data output No 9.
34	Do9c	CML	Data output No 9, inv.
35	Gnd		Ground
36	Do10	CML	Data output No 10.
37	Do10c	CML	Data output No 10, inv.
38	Gnd		Ground
39	Do11	CML	Data output No 11.
40	Do11c	CML	Data output No 11, inv.
41	Gnd		Ground
42	Do12	CML	Data output No 12.
43	Do12c	CML	Data output No 12, inv.
44	Gnd		Ground
45			Not Connected
46			Not Connected
47			Not Connected
48	V_{CC}		Positive power supply
49	V_{CC}		Positive power supply
50	Gnd		Ground

Note 1: All RX_SD pins may be tied together (wired OR) to create one Receiver Signal Detect (RX_SD) output.

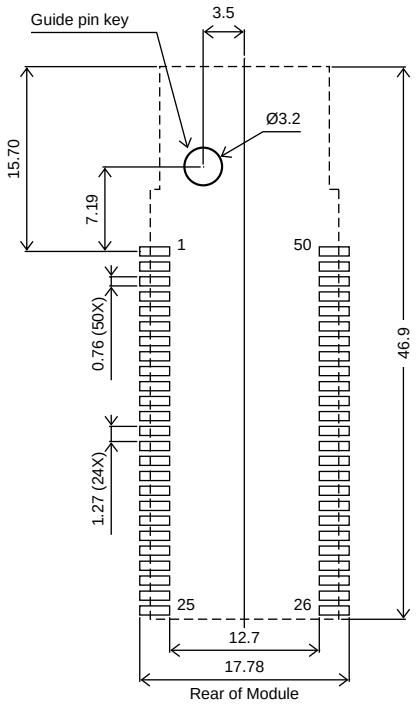
Mechanical Drawing



Dimensions in mm

Figure 9 - MFR62340A-JO: MPO/MTP Connector

PCB Footprint



Dashed lines indicate module outline
Solid lines indicate board layout
Dimensions in mm

Figure 10 - MFR62340A-JO: MPO/MTP Connector (Top View)

Electrical Connections

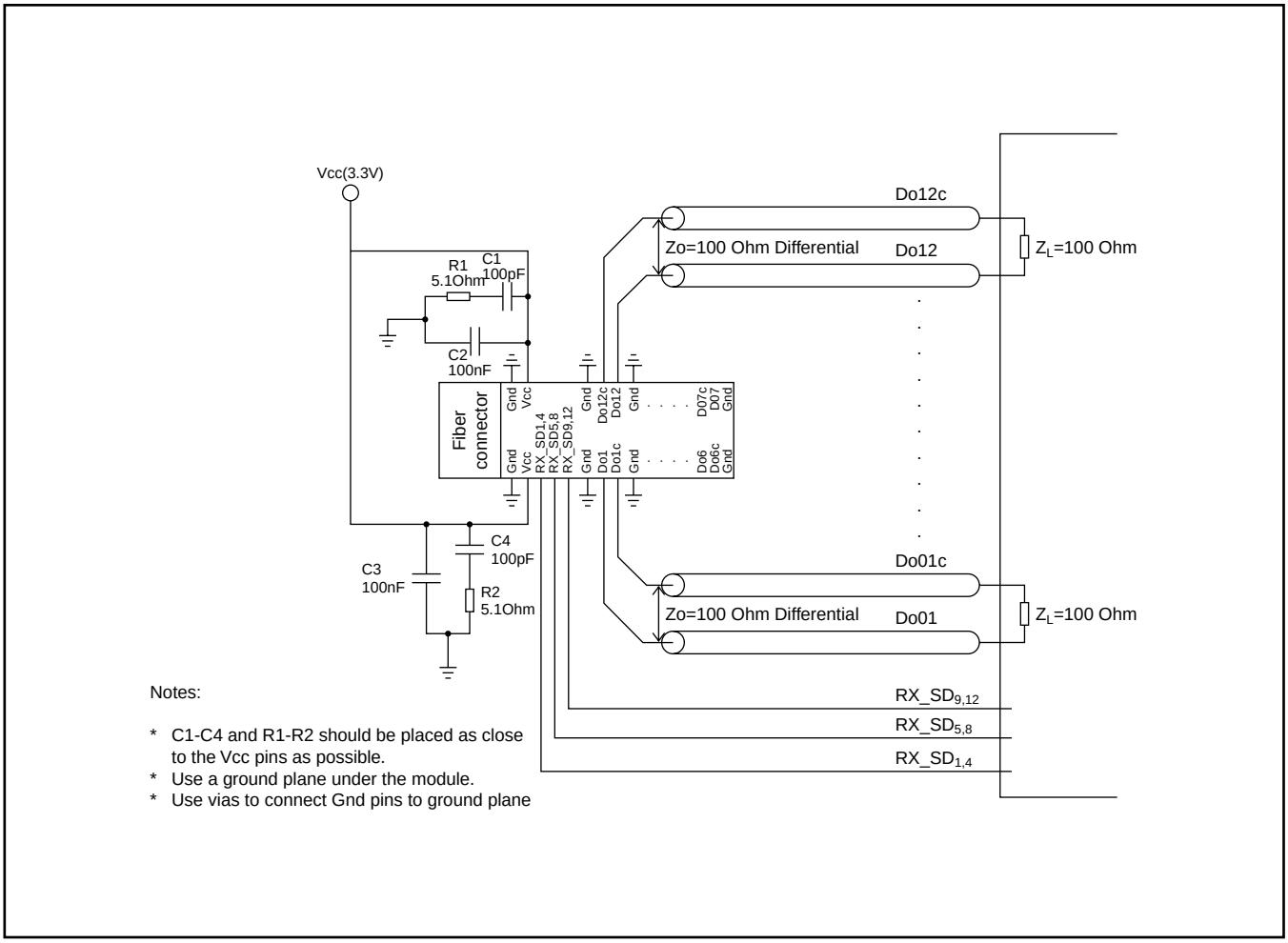


Figure 15 - Recommended Electrical Connections

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