

2Gb gDDR3 SDRAM C-die

96FBGA with Lead-Free & Halogen-Free
(RoHS compliant)

datasheet

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	- Added current spec. up to 1866Mbps			
1.1	- Added Thermal Characteristics spec on page 38	Sep. 2010	-	S.H.Kim
	- Corrected MRS table and added note on page 72.			

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1. Ordering Information

[Table 1] Samsung 2Gb gDDR3 C-die ordering information table

Organization	gDDR3-1333(9-9-9)	gDDR3-1600(11-11-11) ⁴	gDDR3-1866(13-13-13) ³	gDDR3-2133(14-14-14) ²	Package
128Mx16	K4W2G1646C-HC15	K4W2G1646C-HC12	K4W2G1646C-HC11	K4W2G1646C-HC1A	96 FBGA

NOTE :

1. Speed bin is in order of CL-tRCD-tRP.
2. Backward Compatible to gDDR3-1866(13-13-13), gDDR3-1600(11-11-11), gDDR3-1333(9-9-9)
3. Backward Compatible to gDDR3-1600(11-11-11), gDDR3-1333(9-9-9)
4. Backward Compatible to gDDR3-1333(9-9-9)

2. Key Features

[Table 2] 2Gb gDDR3 C-die Speed bins

Speed	gDDR3-800	gDDR3-1066	gDDR3-1333	gDDR3-1600	gDDR3-1866	gDDR3-2133	Unit
	6-6-6	7-7-7	9-9-9	11-11-11	13-13-13	14-14-14	
tCK(min)	2.5	1.875	1.5	1.25	1.07	0.935	ns
CAS Latency	6	7	9	11	13	14	nCK
tRCD(min)	15	13.125	13.5	13.75	13.91	13.09	ns
tRP(min)	15	13.125	13.5	13.75	13.91	13.09	ns
tRAS(min)	37.5	37.5	36	35	34	33	ns
tRC(min)	52.5	50.625	49.5	48.75	47.91	46.09	ns

- JEDEC standard 1.5V ± 0.075V Power Supply
- V_{DDQ} = 1.5V ± 0.075V
- 400 MHz f_{CK} for 800Mb/sec/pin, 533MHz f_{CK} for 1066Mb/sec/pin, 667MHz f_{CK} for 1333Mb/sec/pin, 800MHz f_{CK} for 1600Mb/sec/pin, 900MHz f_{CK} for 1866Mb/sec/pin, 1000MHz f_{CK} for 2133Mb/sec/pin
- 8 Banks
- Programmable CAS Latency(posted CAS): 5,6,7,8,9,10,11,13,14
- Programmable Additive Latency: 0, CL-2 or CL-1 clock
- Programmable CAS Write Latency (CWL) = 5 (gDDR3-800), 6 (gDDR3-1066), 7 (gDDR3-1333), 8 (gDDR3-1600), 9(gDDR3-1866) and 10(gDDR3-2133)
- 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address "000" only), 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data-Strobe
- Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm ± 1%)
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower than T_{CASE} 85°C, 3.9us at 85°C < T_{CASE} ≤ 95 °C
- Asynchronous Reset
- Package : 96 balls FBGA - x16
- All of Lead-Free products are compliant for RoHS
- All of products are Halogen-free

The 2Gb gDDR3 SDRAM C-die is organized as a 16Mbit x 16 I/Os x 8 banks device. This synchronous device achieves high speed double-data-rate transfer rates of up to 2133Mb/sec/pin (gDDR3-2133) for general applications.

The chip is designed to comply with the following key gDDR3 SDRAM features such as posted CAS, Programmable CWL, Internal (Self) Calibration, On Die Termination using ODT pin and Asynchronous Reset .

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the crosspoint of differential clocks (CK rising and $\overline{CK}$ falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and $\overline{DQS}$) in a source synchronous fashion. The address bus is used to convey row, column, and bank address information in a $\overline{RAS}/CAS$ multiplexing style. The gDDR3 device operates with a single 1.5V ± 0.075V power supply and 1.5V ± 0.075V V_{DDQ}.

The 2Gb gDDR3 C-die device is available in 96balls FBGA(x16).

- NOTE :**
1. This data sheet is an abstract of full gDDR3 specification and does not cover the common features which are described in "gDDR3 SDRAM Device Operation & Timing Diagram".
 2. The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

3. Package pinout/Mechanical Dimension & Addressing

3.1 x16 Package Pinout (Top view) : 96ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	V _{DDQ}	DQU5	DQU7				DQU4	V _{DDQ}	V _{SS}	A
B	V _{SSQ}	V _{DD}	V _{SS}				$\overline{\text{DQSU}}$	DQU6	V _{SSQ}	B
C	V _{DDQ}	DQU3	DQU1				DQSU	DQU2	V _{DDQ}	C
D	V _{SSQ}	V _{DDQ}	DMU				DQU0	V _{SSQ}	V _{DD}	D
E	V _{SS}	V _{SSQ}	DQL0				DML	V _{SSQ}	V _{DDQ}	E
F	V _{DDQ}	DQL2	DQSL				DQL1	DQL3	V _{SSQ}	F
G	V _{SSQ}	DQL6	$\overline{\text{DQSL}}$				V _{DD}	V _{SS}	V _{SSQ}	G
H	V _{REFDQ}	V _{DDQ}	DQL4				DQL7	DQL5	V _{DDQ}	H
J	NC	V _{SS}	$\overline{\text{RAS}}$				CK	V _{SS}	NC	J
K	ODT	V _{DD}	$\overline{\text{CAS}}$				$\overline{\text{CK}}$	V _{DD}	CKE	K
L	NC	$\overline{\text{CS}}$	WE				A10/AP	ZQ	NC	L
M	V _{SS}	BA0	BA2				NC	V _{REFCA}	V _{SS}	M
N	V _{DD}	A3	A0				A12/ $\overline{\text{BC}}$	BA1	V _{DD}	N
P	V _{SS}	A5	A2				A1	A4	V _{SS}	P
R	V _{DD}	A7	A9				A11	A6	V _{DD}	R
T	V _{SS}	RESET	A13				NC	A8	V _{SS}	T

Ball Locations (x16)

- Populated ball
- + Ball not populated

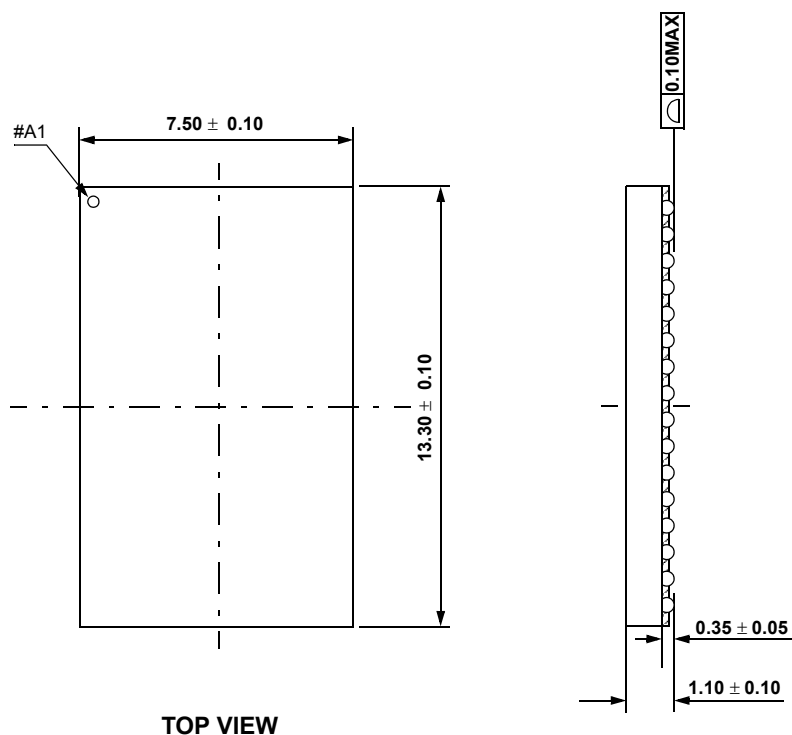
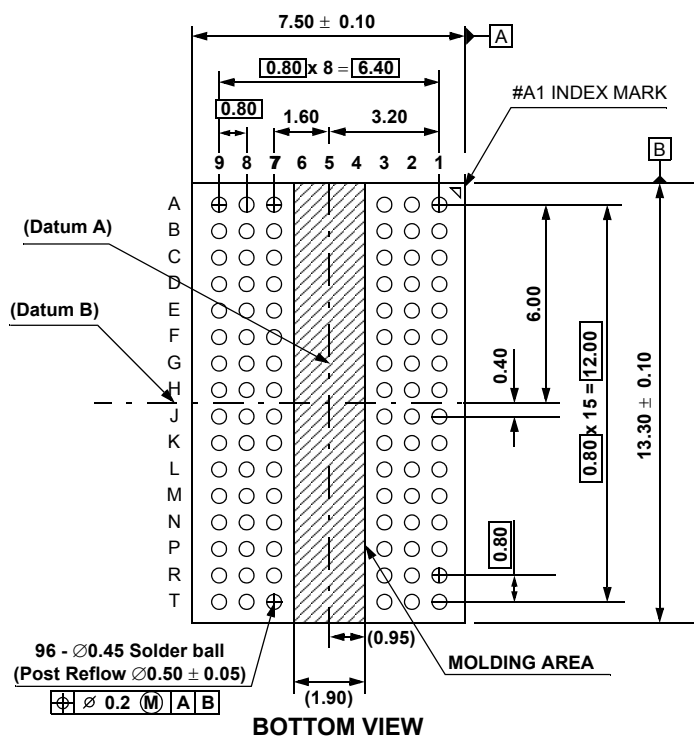
Top view

(See the balls through the package)

	1	2	3	4	5	6	7	8	9
A	●	●	●	+	+	+	●	●	●
B	●	●	●	+	+	+	●	●	●
C	●	●	●	+	+	+	●	●	●
D	●	●	●	+	+	+	●	●	●
E	●	●	●	+	+	+	●	●	●
F	●	●	●	+	+	+	●	●	●
G	●	●	●	+	+	+	●	●	●
H	●	●	●	+	+	+	●	●	●
J	●	●	●	+	+	+	●	●	●
K	●	●	●	+	+	+	●	●	●
L	●	●	●	+	+	+	●	●	●
M	●	●	●	+	+	+	●	●	●
N	●	●	●	+	+	+	●	●	●
P	●	●	●	+	+	+	●	●	●
R	●	●	●	+	+	+	●	●	●
T	●	●	●	+	+	+	●	●	●

3.2 FBGA Package Dimension (x16)

Units : Millimeters



4. Input/Output Functional Description

[Table 3] Input/Output function description

Symbol	Type	Function
CK, $\overline{\text{CK}}$	Input	Clock: CK and $\overline{\text{CK}}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{\text{CK}}$. Output (read) data is referenced to the crossings of CK and $\overline{\text{CK}}$.
CKE	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (Row Active in any bank). CKE is asynchronous for self refresh exit. After V_{REFCA} has become stable during the power on and initialization sequence, it must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{\text{CK}}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
$\overline{\text{CS}}$	Input	Chip Select: All commands are masked when $\overline{\text{CS}}$ is registered HIGH. $\overline{\text{CS}}$ provides for external Rank selection on systems with multiple Ranks. $\overline{\text{CS}}$ is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{\text{DQS}}$ and DM/TDQS, $\overline{\text{DM/TDQS}}$ (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. The ODT pin will be ignored if the Mode Register (MR1) is programmed to disable ODT.
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Input	Command Inputs: $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ (along with $\overline{\text{CS}}$) define the command being entered.
DM (DMU), (DML)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/ $\overline{\text{TDQS}}$ is enabled by Mode Register A11 setting in MR1.
BA0 - BA2	Input	Bank Address Inputs: BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.
A0 - A13	Input	Address Inputs: Provided the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/ $\overline{\text{BC}}$ have additional functions, see below) The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Autoprecharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH:Autoprecharge; LOW: No Autoprecharge) A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). if only one bank is to be precharged, the bank is selected by bank addresses.
A12 / $\overline{\text{BC}}$	Input	Burst Chop: A12 is sampled during Read and Write commands to determine if burst chop(on-the-fly) will be performed. (HIGH : no burst chop, LOW : burst chopped). See command truth table for details
$\overline{\text{RESET}}$	Input	Active Low Asynchronous Reset: Reset is active when $\overline{\text{RESET}}$ is LOW, and inactive when $\overline{\text{RESET}}$ is HIGH. $\overline{\text{RESET}}$ must be HIGH during normal operation. $\overline{\text{RESET}}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD} , i.e. 1.20V for DC high and 0.30V for DC low.
DQ	Input/Output	Data Input/ Output: Bi-directional data bus.
DQS, ($\overline{\text{DQS}}$)	Input/Output	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL: corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS, DQSL and DQSU are paired with differential signals $\overline{\text{DQS}}$, $\overline{\text{DQSL}}$ and $\overline{\text{DQSU}}$, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
TDQS, ($\overline{\text{TDQS}}$)	Output	Termination Data Strobe: TDQS/ $\overline{\text{TDQS}}$ is applicable for X8 DRAMs only. When enabled via Mode Register A11=1 in MR1, DRAM will enable the same termination resistance function on TDQS/ $\overline{\text{TDQS}}$ that is applied to DQS/ $\overline{\text{DQS}}$. When disabled via mode register A11=0 in MR1, DM/TDQS will provide the data mask function and TDQS is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11=0 in MR1.
NC		No Connect: No internal electrical connection is present.
V_{DDQ}	Supply	DQ Power Supply: 1.5V +/- 0.075V
V_{SSQ}	Supply	DQ Ground
V_{DD}	Supply	Power Supply: 1.5V +/- 0.075V
V_{SS}	Supply	Ground
V_{REFDQ}	Supply	Reference voltage for DQ
V_{REFCA}	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

NOTE : Input only pins (BA0-BA2, A0-A13, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{CS}}$, CKE, ODT and $\overline{\text{RESET}}$) do not supply termination.

5. gDDR3 SDRAM Addressing

1Gb

Configuration	256Mb x 4	128Mb x 8	64Mb x 16
# of Bank	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A ₁₀ /AP	A ₁₀ /AP	A ₁₀ /AP
Row Address	A ₀ - A ₁₃	A ₀ - A ₁₃	A ₀ - A ₁₂
Column Address	A ₀ - A ₉ , A ₁₁	A ₀ - A ₉	A ₀ - A ₉
BC switch on the fly	A ₁₂ / $\overline{BC}$	A ₁₂ / $\overline{BC}$	A ₁₂ / $\overline{BC}$
Page size ^{*1}	1 KB	1 KB	2 KB

2Gb

Configuration	512Mb x 4	256Mb x 8	128Mb x 16
# of Bank	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A ₁₀ /AP	A ₁₀ /AP	A ₁₀ /AP
Row Address	A ₀ - A ₁₄	A ₀ - A ₁₄	A ₀ - A ₁₃
Column Address	A ₀ - A ₉ , A ₁₁	A ₀ - A ₉	A ₀ - A ₉
BC switch on the fly	A ₁₂ / $\overline{BC}$	A ₁₂ / $\overline{BC}$	A ₁₂ / $\overline{BC}$
Page size ^{*1}	1 KB	1 KB	2 KB

4Gb

Configuration	1Gb x 4	512Mb x 8	256Mb x 16
# of Bank	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A ₁₀ /AP	A ₁₀ /AP	A ₁₀ /AP
Row Address	A ₀ - A ₁₅	A ₀ - A ₁₅	A ₀ - A ₁₄
Column Address	A ₀ - A ₉ , A ₁₁	A ₀ - A ₉	A ₀ - A ₉
BC switch on the fly	A ₁₂ / $\overline{BC}$	A ₁₂ / $\overline{BC}$	A ₁₂ / $\overline{BC}$
Page size ^{*1}	1 KB	1 KB	2 KB

8Gb

Configuration	2Gb x 4	1Gb x 8	512Mb x 16
# of Bank	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A ₁₀ /AP	A ₁₀ /AP	A ₁₀ /AP
Row Address	A ₀ - A ₁₅	A ₀ - A ₁₅	A ₀ - A ₁₅
Column Address	A ₀ - A ₉ , A ₁₁ , A ₁₃	A ₀ - A ₉ , A ₁₁	A ₀ - A ₉
BC switch on the fly	A ₁₂ / $\overline{BC}$	A ₁₂ / $\overline{BC}$	A ₁₂ / $\overline{BC}$
Page size ^{*1}	2 KB	2 KB	2 KB

NOTE 1 : Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered.

Page size is per bank, calculated as follows: $\text{page size} = 2^{\text{COLBITS}} \times \text{ORG} \div 8$
 where, COLBITS = the number of column address bits, ORG = the number of I/O (DQ) bits

6. Absolute Maximum Ratings

6.1 Absolute Maximum DC Ratings

[Table 4] Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-0.4 V ~ 1.975 V	V	1,3
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.4 V ~ 1.975 V	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.4 V ~ 1.975 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2

NOTE :

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC standard.
- V_{DD} and V_{DDQ} must be within 300mV of each other at all times; and V_{REF} must be not greater than $0.6 \times V_{DDQ}$. When V_{DD} and V_{DDQ} are less than 500mV; V_{REF} may be equal to or less than 300mV.

6.2 DRAM Component Operating Temperature Range

[Table 5] Temperature Range

Symbol	Parameter	rating	Unit	NOTE
T_{OPER}	Operating Temperature Range	0 to 95	°C	1, 2, 3

NOTE :

- Operating Temperature T_{OPER} is the case surface temperature on the center/top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85°C under all operating conditions
- Some applications require operation of the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
 - Refresh commands must be doubled in frequency, therefore reducing the refresh interval $tREFI$ to 3.9us.
 - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0_b and MR2 A7 = 1_b), in this case I_{DD6} current can be increased around 10~20% than normal Temperature range.

7. AC & DC Operating Conditions

7.1 Recommended DC operating Conditions (SSTL_1.5)

[Table 6] Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	NOTE
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1,2
V_{DDQ}	Supply Voltage for Output	1.425	1.5	1.575	V	1,2

NOTE :

- Under all conditions V_{DDQ} must be less than or equal to V_{DD} .
- V_{DDQ} tracks with V_{DD} . AC parameters are measured with V_{DD} and V_{DDQ} tied together.

8. AC & DC Input Measurement Levels

8.1 AC & DC Logic input levels for single-ended signals

[Table 7] Single-ended AC & DC input levels for Command and Address

Symbol	Parameter	gDDR3-800/1066/1333/1600		gDDR3-1866/2133		Unit	NOTE
		Min.	Max.	Min.	Max.		
$V_{IH,CA}(DC100)$	DC input logic high	$V_{REF} + 100$	V_{DD}	$V_{REF} + 100$	V_{DD}	mV	1,5
$V_{IL,CA}(DC100)$	DC input logic low	V_{SS}	$V_{REF} - 100$	V_{SS}	$V_{REF} - 100$	mV	1,6
$V_{IH,CA}(AC175)$	AC input logic high	$V_{REF} + 175$	Note 2	-	-	mV	1,2,7
$V_{IL,CA}(AC175)$	AC input logic low	Note 2	$V_{REF} - 175$	-	-	mV	1,2,8
$V_{IH,CA}(AC150)$	AC input logic high	$V_{REF} + 150$	Note 2	-	-	mV	1,2,7
$V_{IL,CA}(AC150)$	AC input logic low	Note 2	$V_{REF} - 150$	-	-	mV	1,2,8
$V_{IH,CA}(AC135)$	AC input logic high	-	-	$V_{REF} + 135$	Note 2	mV	1,2,7
$V_{IL,CA}(AC135)$	AC input logic low	-	-	Note 2	$V_{REF} - 135$	mV	1,2,8
$V_{IH,CA}(AC125)$	AC input logic high	-	-	$V_{REF} + 125$	Note 2	mV	1,2,7
$V_{IL,CA}(AC125)$	AC input logic low	-	-	Note 2	$V_{REF} - 125$	mV	1,2,8
$V_{REFCA}(DC)$	Reference Voltage for ADD, CMD inputs	$0.49 \cdot V_{DD}$	$0.51 \cdot V_{DD}$	$0.49 \cdot V_{DD}$	$0.51 \cdot V_{DD}$	V	3,4

NOTE :

- For input only pins except $\overline{RESET}$, $V_{REF} = V_{REFCA}(DC)$
- See 'Overshoot/Undershoot Specification' on page 19.
- The AC peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REF}(DC)$ by more than $\pm 1\% V_{DD}$ (for reference : approx. $\pm 15mV$)
- For reference : approx. $V_{DD}/2 \pm 15mV$
- $V_{IH}(dc)$ is used as a simplified symbol for $V_{IH,CA}(DC100)$
- $V_{IL}(dc)$ is used as a simplified symbol for $V_{IL,CA}(DC100)$
- $V_{IH}(ac)$ is used as a simplified symbol for $V_{IH,CA}(AC175)$, $V_{IH,CA}(AC150)$, $V_{IH,CA}(AC135)$ and $V_{IH,CA}(AC125)$; $V_{IH,CA}(AC175)$ value is used when $V_{REF} + 175mV$ is referenced, $V_{IH,CA}(AC150)$ value is used when $V_{REF} + 150mV$ is referenced, $V_{IH,CA}(AC135)$ value is used when $V_{REF} + 135mV$ is referenced and $V_{IH,CA}(AC125)$ value is used when $V_{REF} + 125mV$ is referenced.
- $V_{IL}(ac)$ is used as a simplified symbol for $V_{IL,CA}(AC175)$ and $V_{IL,CA}(AC150)$; $V_{IL,CA}(AC175)$ value is used when $V_{REF} - 175mV$ is referenced, $V_{IL,CA}(AC150)$ value is used when $V_{REF} - 150mV$ is referenced, $V_{IL,CA}(AC135)$ value is used when $V_{REF} - 135mV$ is referenced and $V_{IL,CA}(AC125)$ value is used when $V_{REF} - 125mV$ is referenced.

[Table 8] Single-ended AC & DC input levels for DQ and DM

Symbol	Parameter	gDDR3-800/1066		gDDR3-1333/1600		gDDR3-1866/2133		Unit	NOTE
		Min.	Max.	Min.	Max.	Min.	Max.		
$V_{IH,DQ}(DC100)$	DC input logic high	$V_{REF} + 100$	V_{DD}	$V_{REF} + 100$	V_{DD}	$V_{REF} + 100$	V_{DD}	mV	1,5
$V_{IL,DQ}(DC100)$	DC input logic low	V_{SS}	$V_{REF} - 100$	V_{SS}	$V_{REF} - 100$	V_{SS}	$V_{REF} - 100$	mV	1,6
$V_{IH,DQ}(AC175)$	AC input logic high	$V_{REF} + 175$	NOTE 2	-	-	-	-	mV	1,2,7
$V_{IL,DQ}(AC175)$	AC input logic low	NOTE 2	$V_{REF} - 175$	-	-	-	-	mV	1,2,8
$V_{IH,DQ}(AC150)$	AC input logic high	$V_{REF} + 150$	NOTE 2	$V_{REF} + 150$	NOTE 2	-	-	mV	1,2,7
$V_{IL,DQ}(AC150)$	AC input logic low	NOTE 2	$V_{REF} - 150$	NOTE 2	$V_{REF} - 150$	-	-	mV	1,2,8
$V_{IH,DQ}(AC135)$	AC input logic high	-	-	-	-	$V_{REF} + 135$	NOTE 2	mV	1,2,7
$V_{IL,DQ}(AC135)$	AC input logic low	-	-	-	-	NOTE 2	$V_{REF} - 135$	mV	1,2,8
$V_{REFDQ}(DC)$	Reference Voltage for DQ, DM inputs	$0.49 \cdot V_{DD}$	$0.51 \cdot V_{DD}$	$0.49 \cdot V_{DD}$	$0.51 \cdot V_{DD}$	$0.49 \cdot V_{DD}$	$0.51 \cdot V_{DD}$	V	3,4

NOTE :

- For input only pins except $\overline{RESET}$, $V_{REF} = V_{REFDQ}(DC)$
- See 'Overshoot/Undershoot Specification' on page 19.
- The AC peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REF}(DC)$ by more than $\pm 1\% V_{DD}$ (for reference : approx. $\pm 15mV$)
- For reference : approx. $V_{DD}/2 \pm 15mV$
- $V_{IH}(dc)$ is used as a simplified symbol for $V_{IH,DQ}(DC100)$
- $V_{IL}(dc)$ is used as a simplified symbol for $V_{IL,DQ}(DC100)$
- $V_{IH}(ac)$ is used as a simplified symbol for $V_{IH,DQ}(AC175)$, $V_{IH,DQ}(AC150)$ and $V_{IH,DQ}(AC135)$; $V_{IH,DQ}(AC175)$ value is used when $V_{REF} + 175mV$ is referenced, $V_{IH,DQ}(AC150)$ value is used when $V_{REF} + 150mV$ is referenced.
- $V_{IL}(ac)$ is used as a simplified symbol for $V_{IL,DQ}(AC175)$, $V_{IL,DQ}(AC150)$; $V_{IL,DQ}(AC175)$ value is used when $V_{REF} - 175mV$ is referenced, $V_{IL,DQ}(AC150)$ value is used when $V_{REF} - 150mV$ is referenced.

8.2 V_{REF} Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages V_{REFCA} and V_{REFDQ} are illustrate in Figure 1. It shows a valid reference voltage $V_{REF}(t)$ as a function of time. (V_{REF} stands for V_{REFCA} and V_{REFDQ} likewise).

$V_{REF}(DC)$ is the linear average of $V_{REF}(t)$ over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table 7 on page 12. Furthermore $V_{REF}(t)$ may temporarily deviate from $V_{REF}(DC)$ by no more than $\pm 1\% V_{DD}$.

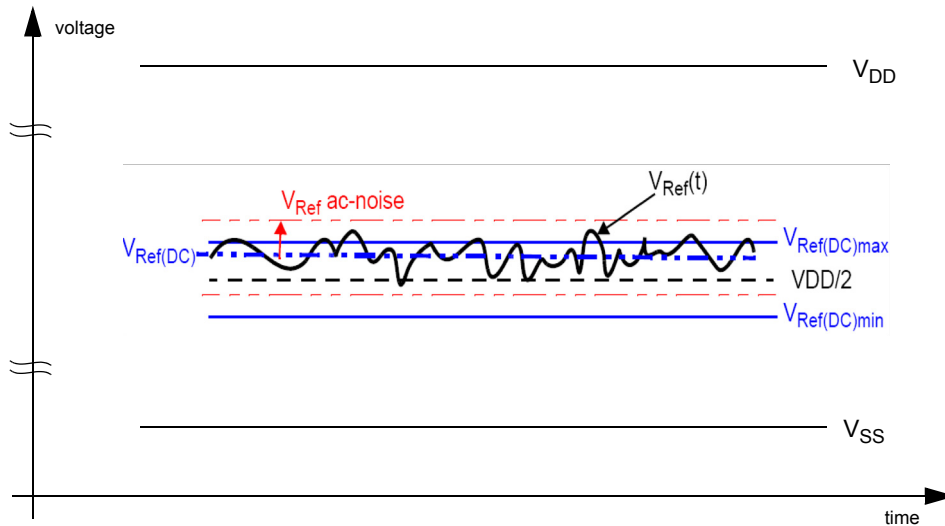


Figure 1. Illustration of $V_{REF}(DC)$ tolerance and V_{REF} ac-noise limits

The voltage levels for setup and hold time measurements $V_{IH}(AC)$, $V_{IH}(DC)$, $V_{IL}(AC)$ and $V_{IL}(DC)$ are dependent on V_{REF} .

" V_{REF} " shall be understood as $V_{REF}(DC)$, as defined in Figure 1 .

This clarifies, that dc-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{REF}(DC)$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} ac-noise. Timing and voltage effects due to ac-noise on V_{REF} up to the specified limit ($\pm 1\%$ of V_{DD}) are included in DRAM timings and their associated deratings.

8.3 AC & DC Logic Input Levels for Differential Signals

8.3.1 Differential signals definition

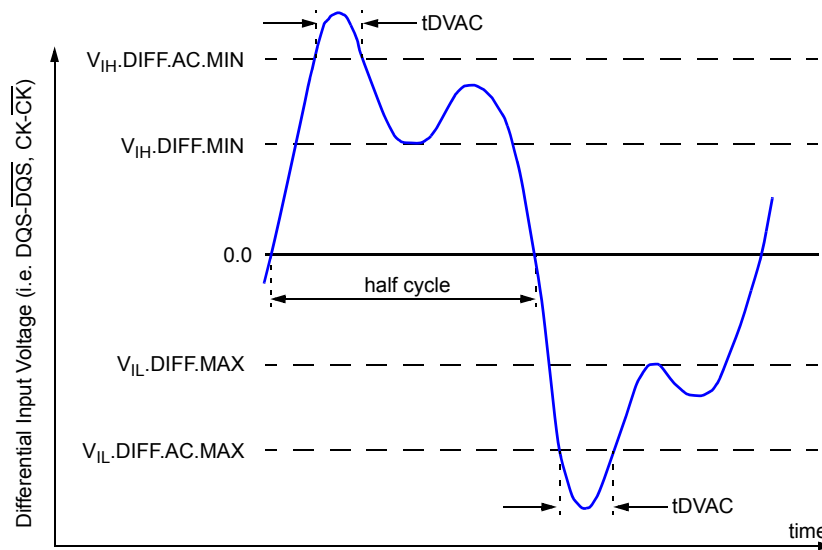


Figure 2. Definition of differential ac-swing and "time above ac level" tDVAC

8.3.2 Differential swing requirement for clock (CK - $\overline{\text{CK}}$) and strobe (DQS - $\overline{\text{DQS}}$)

[Table 9] Differential AC & DC Input Levels

Symbol	Parameter	gDDR3-800/1066/1333/1600/1866/2133		unit	NOTE
		min	max		
V_{IHdiff}	differential input high	+0.2	NOTE 3	V	1
V_{ILdiff}	differential input low	NOTE 3	-0.2	V	1
$V_{IHdiff}(AC)$	differential input high ac	$2 \times (V_{IH}(AC) - V_{REF})$	NOTE 3	V	2
$V_{ILdiff}(AC)$	differential input low ac	NOTE 3	$2 \times (V_{IL}(AC) - V_{REF})$	V	2

NOTE :

- Used to define a differential signal slew-rate.
- for CK - $\overline{\text{CK}}$ use $V_{IH}/V_{IL}(AC)$ of ADD/CMD and V_{REFCA} ; for DQS - $\overline{\text{DQS}}$, DQSL - $\overline{\text{DQSL}}$, DQSU - $\overline{\text{DQSU}}$ use $V_{IH}/V_{IL}(AC)$ of DQs and V_{REFDQ} ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
- These values are not defined, however they single-ended signals CK, $\overline{\text{CK}}$, DQS, $\overline{\text{DQS}}$, DQSL, $\overline{\text{DQSL}}$, DQSU, $\overline{\text{DQSU}}$ need to be within the respective limits ($V_{IH}(DC)$ max, $V_{IL}(DC)$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "overshoot and Undershoot Specification"

[Table 10] Allowed time before ringback (tDVAC) for CK - $\overline{\text{CK}}$ and DQS - $\overline{\text{DQS}}$

Slew Rate [V/ns]	tDVAC [ps] @ $ V_{IH/Ldiff}(AC) = 350mV$		tDVAC [ps] @ $ V_{IH/Ldiff}(AC) = 300mV$		tDVAC [ps] @ $ V_{IH/Ldiff}(AC) = 270mV$		tDVAC [ps] @ $ V_{IH/Ldiff}(AC) = 250mV$	
	min	max	min	max	min	max	min	max
> 4.0	75	-	175	-	TBD	-	TBD	-
4.0	57	-	170	-	TBD	-	TBD	-
3.0	50	-	167	-	TBD	-	TBD	-
2.0	38	-	163	-	TBD	-	TBD	-
1.8	34	-	162	-	TBD	-	TBD	-
1.6	29	-	161	-	TBD	-	TBD	-
1.4	22	-	159	-	TBD	-	TBD	-
1.2	13	-	155	-	TBD	-	TBD	-
1.0	0	-	150	-	TBD	-	TBD	-
< 1.0	0	-	150	-	TBD	-	TBD	-

8.3.3 Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, DQSL, DQSU, $\overline{\text{CK}}$, $\overline{\text{DQS}}$, $\overline{\text{DQSL}}$, or $\overline{\text{DQSU}}$) has also to comply with certain requirements for single-ended signals.

CK and $\overline{\text{CK}}$ have to approximately reach $V_{\text{SEHmin}} / V_{\text{SELmax}}$ [approximately equal to the ac-levels $\{V_{\text{IH}}(\text{AC}) / V_{\text{IL}}(\text{AC})\}$ for ADD/CMD signals] in every half-cycle.

DQS, DQSL, DQSU, $\overline{\text{DQS}}$, $\overline{\text{DQSL}}$ have to reach $V_{\text{SEHmin}} / V_{\text{SELmax}}$ [approximately the ac-levels $\{V_{\text{IH}}(\text{AC}) / V_{\text{IL}}(\text{AC})\}$ for DQ signals] in every half-cycle proceeding and following a valid transition.

Note that the applicable ac-levels for ADD/CMD and DQ's might be different per speed-bin etc. E.g. if $V_{\text{IH150}}(\text{AC})/V_{\text{IL150}}(\text{AC})$ is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK and $\overline{\text{CK}}$.

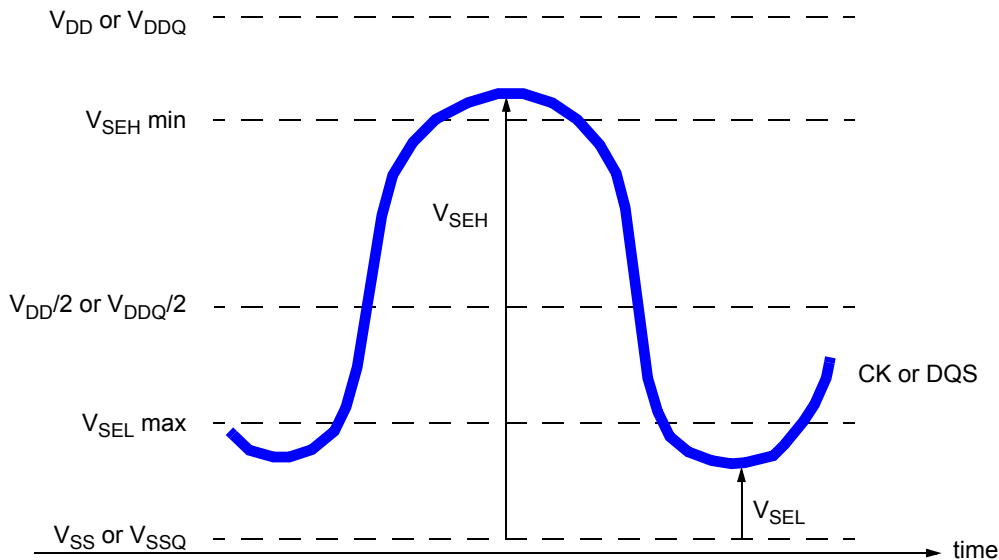


Figure 3. Single-ended requirement for differential signals

Note that while ADD/CMD and DQ signal requirements are with respect to V_{REF} , the single-ended components of differential signals have a requirement with respect to $V_{\text{DD}}/2$; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach V_{SELmax} , V_{SEHmin} has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

[Table 11] Single-ended levels for CK, DQS, DQSL, DQSU, $\overline{\text{CK}}$, $\overline{\text{DQS}}$, $\overline{\text{DQSL}}$, or $\overline{\text{DQSU}}$

Symbol	Parameter	gDDR3-800/1066/1333/1600/1866/2133		Unit	NOTE
		Min	Max		
V_{SEH}	Single-ended high-level for strobes	$(V_{\text{DD}}/2)+0.175$	NOTE3	V	1, 2
	Single-ended high-level for CK, $\overline{\text{CK}}$	$(V_{\text{DD}}/2)+0.175$	NOTE3	V	1, 2
V_{SEL}	Single-ended low-level for strobes	NOTE3	$(V_{\text{DD}}/2)-0.175$	V	1, 2
	Single-ended low-level for CK, $\overline{\text{CK}}$	NOTE3	$(V_{\text{DD}}/2)-0.175$	V	1, 2

NOTE :

- For CK, $\overline{\text{CK}}$ use $V_{\text{IH}}/V_{\text{IL}}(\text{AC})$ of ADD/CMD; for strobes (DQS, $\overline{\text{DQS}}$, DQSL, $\overline{\text{DQSL}}$, DQSU, $\overline{\text{DQSU}}$) use $V_{\text{IH}}/V_{\text{IL}}(\text{AC})$ of DQs.
- $V_{\text{IH}}(\text{AC})/V_{\text{IL}}(\text{AC})$ for DQs is based on V_{REFDQ} ; $V_{\text{IH}}(\text{AC})/V_{\text{IL}}(\text{AC})$ for ADD/CMD is based on V_{REFCA} ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here
- These values are not defined, however the single-ended signals CK, $\overline{\text{CK}}$, DQS, $\overline{\text{DQS}}$, DQSL, $\overline{\text{DQSL}}$, DQSU, $\overline{\text{DQSU}}$ need to be within the respective limits ($V_{\text{IH}}(\text{DC})$ max, $V_{\text{IL}}(\text{DC})$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specification"

8.4 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, $\overline{\text{CK}}$ and DQS, $\overline{\text{DQS}}$) must meet the requirements in below table. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signal to the mid level between of V_{DD} and V_{SS} .

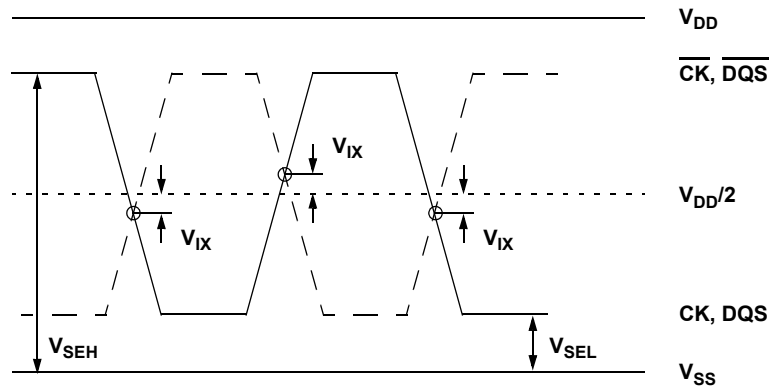


Figure 4. VIX Definition

[Table 12] Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	gDDR3-800/1066/1333/1600/1866/2133		Unit	NOTE
		Min	Max		
V_{IX}	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK, $\overline{\text{CK}}$	-150	150	mV	2
		-175	175	mV	1
V_{IX}	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for DQS, $\overline{\text{DQS}}$	-150	150	mV	2

NOTE :

- Extended range for V_{IX} is only allowed for clock and if single-ended clock input signals CK and $\overline{\text{CK}}$ are monotonic, have a single-ended swing V_{SEL} / V_{SEH} of at least $V_{DD}/2 \pm 250$ mV, and the differential slew rate of CK- $\overline{\text{CK}}$ is larger than 3 V/ ns. Refer to Table 11 on page 15 for V_{SEL} and V_{SEH} standard values.
- The relation between V_{IX} Min/Max and V_{SEL}/V_{SEH} should satisfy following.
 $(V_{DD}/2) + V_{IX}(\text{Min}) - V_{SEL} \geq 25\text{mV}$
 $V_{SEH} - ((V_{DD}/2) + V_{IX}(\text{Max})) \geq 25\text{mV}$

8.5 Slew rate definition for Differential Input Signals

See 14.3 "Address/Command Setup, Hold and Derating :" on page 48 for single-ended slew rate definitions for address and command signals.
 See 14.4 "Data Setup, Hold and Slew Rate Derating :" on page 54 for single-ended slew rate definitions for data signals.

8.6 Slew rate definitions for Differential Input Signals

Input slew rate for differential signals (CK, $\overline{\text{CK}}$ and DQS, $\overline{\text{DQS}}$) are defined and measured as shown in Table 13 and Figure 5.

[Table 13] Differential input slew rate definition

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK- $\overline{\text{CK}}$ and DQS- $\overline{\text{DQS}}$)	$V_{IL\text{diffmax}}$	$V_{IH\text{diffmin}}$	$\frac{V_{IH\text{diffmin}} - V_{IL\text{diffmax}}}{\text{Delta TRdiff}}$
Differential input slew rate for falling edge (CK- $\overline{\text{CK}}$ and DQS- $\overline{\text{DQS}}$)	$V_{IH\text{diffmin}}$	$V_{IL\text{diffmax}}$	$\frac{V_{IH\text{diffmin}} - V_{IL\text{diffmax}}}{\text{Delta TFdiff}}$

NOTE :

The differential signal (i.e. CK - $\overline{\text{CK}}$ and DQS - $\overline{\text{DQS}}$) must be linear between these thresholds.

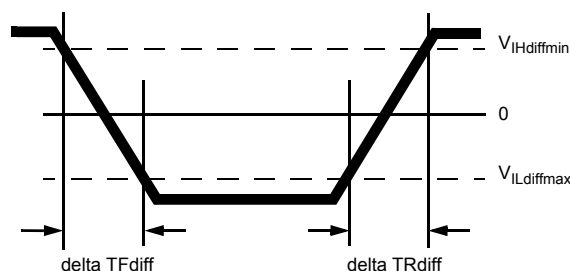


Figure 5. Differential Input Slew Rate definition for DQS, $\overline{\text{DQS}}$, and CK, $\overline{\text{CK}}$

9. AC & DC Output Measurement Levels

9.1 Single-ended AC & DC Output Levels

[Table 14] Single-ended AC & DC output levels

Symbol	Parameter	gDDR3-800/1066/1333/1600/1866/2133	Units	NOTE
$V_{OH}(DC)$	DC output high measurement level (for IV curve linearity)	$0.8 \times V_{DDQ}$	V	
$V_{OM}(DC)$	DC output mid measurement level (for IV curve linearity)	$0.5 \times V_{DDQ}$	V	
$V_{OL}(DC)$	DC output low measurement level (for IV curve linearity)	$0.2 \times V_{DDQ}$	V	
$V_{OH}(AC)$	AC output high measurement level (for output SR)	$V_{TT} + 0.1 \times V_{DDQ}$	V	1
$V_{OL}(AC)$	AC output low measurement level (for output SR)	$V_{TT} - 0.1 \times V_{DDQ}$	V	1

NOTE : 1. The swing of $\pm 0.1 \times V_{DDQ}$ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to $V_{TT} = V_{DDQ}/2$.

9.2 Differential AC & DC Output Levels

[Table 15] Differential AC & DC output levels

Symbol	Parameter	gDDR3-800/1066/1333/1600/1866/2133	Units	NOTE
$V_{OHdiff}(AC)$	AC differential output high measurement level (for output SR)	$+0.2 \times V_{DDQ}$	V	1
$V_{OLdiff}(AC)$	AC differential output low measurement level (for output SR)	$-0.2 \times V_{DDQ}$	V	1

NOTE : 1. The swing of $\pm 0.2 \times V_{DDQ}$ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to $V_{TT} = V_{DDQ}/2$ at each of the differential outputs.

9.3 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL}(AC)$ and $V_{OH}(AC)$ for single ended signals as shown in Table 16 and Figure 6.

[Table 16] Single-ended output slew rate definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	$V_{OL}(AC)$	$V_{OH}(AC)$	$\frac{V_{OH}(AC) - V_{OL}(AC)}{\Delta TRse}$
Single ended output slew rate for falling edge	$V_{OH}(AC)$	$V_{OL}(AC)$	$\frac{V_{OH}(AC) - V_{OL}(AC)}{\Delta TFse}$

NOTE : Output slew rate is verified by design and characterization, and may not be subject to production test.

[Table 17] Single-ended output slew rate

Parameter	Symbol	gDDR3-800		gDDR3-1066		gDDR3-1333		gDDR3-1600		gDDR3-1866		gDDR3-2133		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	2.5	5	2.5	5	2.5	5	2.5	5	2.5	5 ¹⁾	2.5	5 ¹⁾	V/ns

Description : SR : Slew Rate

Q : Query Output (like in DQ, which stands for Data-in, Query-Output)

se : Single-ended Signals

For Ron = RZQ/7 setting

NOTE : 1) In two cases, a maximum slew rate of 6V/ns applies for a single DQ signal within a byte lane.

- Case_1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e they stay at either high or low).
- Case_2 is defined for a single DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 5 V/ns applies.

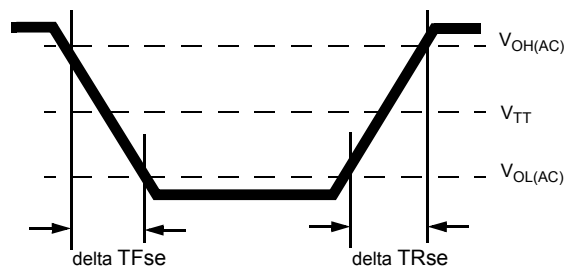


Figure 6. Single-ended Output Slew Rate Definition

9.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OLdiff}(AC)$ and $V_{OHdiff}(AC)$ for differential signals as shown in Table 18 and Figure 7.

[Table 18] Differential output slew rate definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OLdiff}(AC)$	$V_{OHdiff}(AC)$	$\frac{V_{OHdiff}(AC) - V_{OLdiff}(AC)}{\Delta TR_{diff}}$
Differential output slew rate for falling edge	$V_{OHdiff}(AC)$	$V_{OLdiff}(AC)$	$\frac{V_{OHdiff}(AC) - V_{OLdiff}(AC)}{\Delta TF_{diff}}$

NOTE : Output slew rate is verified by design and characterization, and may not be subject to production test.

[Table 19] Differential output slew rate

Parameter	Symbol	gDDR3-800		gDDR3-1066		gDDR3-1333		gDDR3-1600		gDDR3-1866		gDDR3-2133		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQdiff	5	10	5	10	5	10	5	10	5	12	5	12	V/ns

Description : SR : Slew Rate

Q : Query Output (like in DQ, which stands for Data-in, Query-Output)

diff : Differential Signals

For Ron = RZQ/7 setting

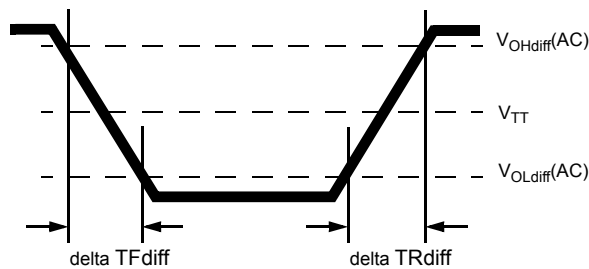


Figure 7. Differential Output Slew Rate Definition

9.5 Reference Load for AC Timing and Output Slew Rate

Figure 8 represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

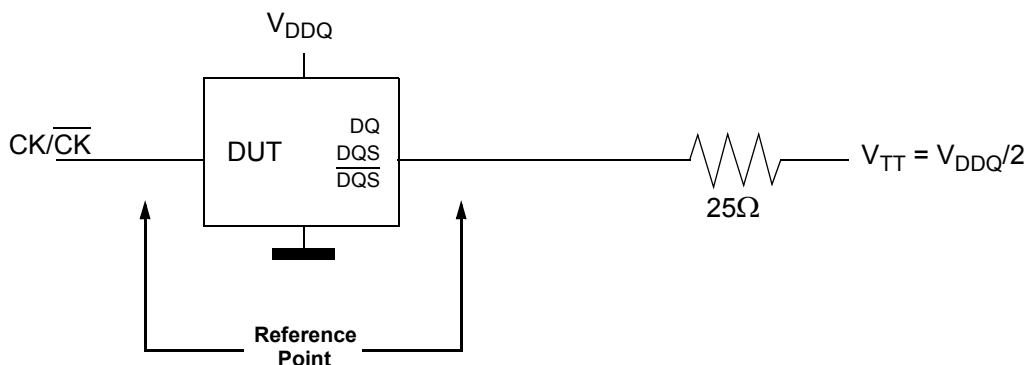


Figure 8. Reference Load for AC Timing and Output Slew Rate

9.6 Overshoot/Undershoot Specification

9.6.1 Address and Control Overshoot and Undershoot specifications

[Table 20] AC overshoot/undershoot specification for Address and Control pins (A0-A12, BA0-BA2, $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, CKE, ODT)

Parameter	Specification						Unit
	gDDR3-800	gDDR3-1066	gDDR3-1333	gDDR3-1600	gDDR3-1866	gDDR3-2133	
Maximum peak amplitude allowed for overshoot area (See Figure 9)	0.4	0.4	0.4	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area (See Figure 9)	0.4	0.4	0.4	0.4	0.4	0.4	V
Maximum overshoot area above V_{DD} (See Figure 9)	0.67	0.5	0.4	0.33	0.28	0.25	V-ns
Maximum undershoot area below V_{SS} (See Figure 9)	0.67	0.5	0.4	0.33	0.28	0.25	V-ns

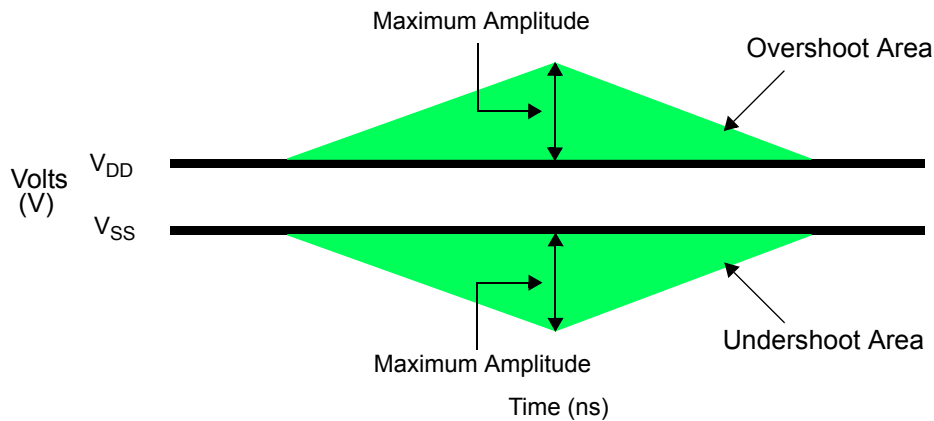


Figure 9. Address and Control Overshoot and Undershoot Definition

9.6.2 Clock, Data, Strobe and Mask Overshoot and Undershoot Specifications

[Table 21] AC overshoot/undershoot specification for Clock, Data, Strobe and Mask (DQ, DQS, $\overline{\text{DQS}}$, DM, CK, $\overline{\text{CK}}$)

Parameter	Specification						Unit
	gDDR3-800	gDDR3-1066	gDDR3-1333	gDDR3-1600	gDDR3-1866	gDDR3-2133	
Maximum peak amplitude allowed for overshoot area (See Figure 10)	0.4	0.4	0.4	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area (See Figure 10)	0.4	0.4	0.4	0.4	0.4	0.4	V
Maximum overshoot area above V_{DDQ} (See Figure 10)	0.25	0.19	0.15	0.13	0.11	0.10	V-ns
Maximum undershoot area below V_{SSQ} (See Figure 10)	0.25	0.19	0.15	0.13	0.11	0.10	V-ns

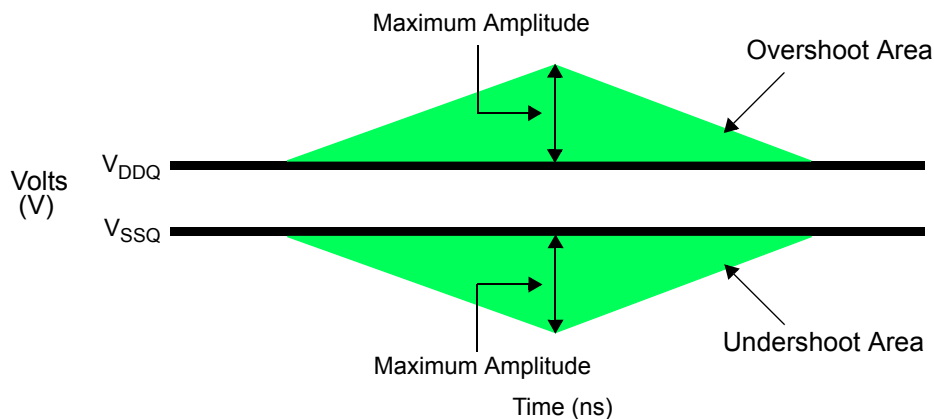


Figure 10. Clock, Data, Strobe and Mask Overshoot and Undershoot Definition

9.7 34ohm Output Driver DC Electrical Characteristics

A functional representation of the output buffer is shown below. Output driver impedance R_{ON} is defined by the value of external reference resistor R_{ZQ} as follows:

$$R_{ON34} = R_{ZQ}/7 \text{ (Nominal 34.3ohms } \pm 10\% \text{ with nominal } R_{ZQ}=240\text{ohm)}$$

The individual Pull-up and Pull-down resistors (R_{ONpu} and R_{ONpd}) are defined as follows

$$R_{ONpu} = \frac{V_{DDQ} - V_{OUT}}{|I_{out}|} \quad \text{under the condition that } R_{ONpd} \text{ is turned off}$$

$$R_{ONpd} = \frac{V_{OUT}}{|I_{out}|} \quad \text{under the condition that } R_{ONpu} \text{ is turned off}$$

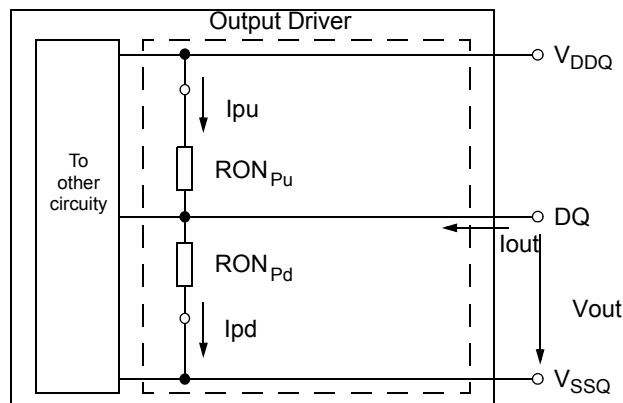


Figure 11. Output Driver : Definition of Voltages and Currents

[Table 22] Output Driver DC Electrical Characteristics, assuming $R_{ZQ}=240\text{ohms}$;
entire operating temperature range ; after proper ZQ calibration

RONnom	Resistor	Vout	Min	Nom	Max	Units	NOTE
34Ohms	RON34pd	$V_{OLdc} = 0.2 \times V_{DDQ}$	0.6	1.0	1.1	RZQ/7	1,2,3
		$V_{OMdc} = 0.5 \times V_{DDQ}$	0.9	1.0	1.1		1,2,3
		$V_{OHdc} = 0.8 \times V_{DDQ}$	0.9	1.0	1.4		1,2,3
	RON34pu	$V_{OLdc} = 0.2 \times V_{DDQ}$	0.9	1.0	1.4		1,2,3
		$V_{OMdc} = 0.5 \times V_{DDQ}$	0.9	1.0	1.1		1,2,3
		$V_{OHdc} = 0.8 \times V_{DDQ}$	0.6	1.0	1.1		1,2,3
40Ohms	RON40pd	$V_{OLdc} = 0.2 \times V_{DDQ}$	0.6	1.0	1.1	RZQ/6	1,2,3
		$V_{OMdc} = 0.5 \times V_{DDQ}$	0.9	1.0	1.1		1,2,3
		$V_{OHdc} = 0.8 \times V_{DDQ}$	0.9	1.0	1.4		1,2,3
	RON40pu	$V_{OLdc} = 0.2 \times V_{DDQ}$	0.9	1.0	1.4		1,2,3
		$V_{OMdc} = 0.5 \times V_{DDQ}$	0.9	1.0	1.1		1,2,3
		$V_{OHdc} = 0.8 \times V_{DDQ}$	0.6	1.0	1.1		1,2,3
Mismatch between Pull-up and Pull-down, MMpupd		$V_{OMdc} = 0.5 \times V_{DDQ}$	-10		10	%	1,2,4

NOTE :

- The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity
- The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and that $V_{SSQ} = V_{SS}$
- Pull-down and pull-up output driver impedance are recommended to be calibrated at $0.5 \times V_{DDQ}$. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at $0.2 \times V_{DDQ}$ and $0.8 \times V_{DDQ}$
- Measurement definition for mismatch between pull-up and pull-down, MM_{pupd} : Measure R_{ONpu} and R_{ONpd} . both at $0.5 \times V_{DDQ}$:

$$MM_{pupd} = \frac{R_{ONpu} - R_{ONpd}}{R_{ONnom}} \times 100$$

9.7.1 Output Drive Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table 23 and Table 24.

$\Delta T = T - T(@\text{calibration})$; $\Delta V = V_{DDQ} - V_{DDQ}(@\text{calibration})$; $V_{DD} = V_{DDQ}$

* dR_{ONdT} and dR_{ONdV} are not subject to production test but are verified by design and characterization

[Table 23] Output Driver Sensitivity Definition

	Min	Max	Units
$RONPU@V_{OHDC}$	$0.6 - dR_{ONdTH} * \Delta T - dR_{ONdVH} * \Delta V $	$1.1 + dR_{ONdTH} * \Delta T + dR_{ONdVH} * \Delta V $	RZQ/7
$RON@V_{OMDC}$	$0.9 - dR_{ONdTM} * \Delta T - dR_{ONdVM} * \Delta V $	$1.1 + dR_{ONdTM} * \Delta T + dR_{ONdVM} * \Delta V $	RZQ/7
$RONPD@VOLDC$	$0.6 - dR_{ONdTL} * \Delta T - dR_{ONdVL} * \Delta V $	$1.1 + dR_{ONdTL} * \Delta T + dR_{ONdVL} * \Delta V $	RZQ/7

[Table 24] Output Driver Voltage and Temperature Sensitivity

Speed Bin	gDDR3-800/1066/1333/1600		gDDR3-1866/2133		Units
	Min	Max	Min	Max	
dR_{ONdTM}	0	1.5	0	1.5	%/°C
dR_{ONdVM}	0	0.15	0	0.13	%/mV
dR_{ONdTL}	0	1.5	0	1.5	%/°C
dR_{ONdVL}	0	0.15	0	0.13	%/mV
dR_{ONdTH}	0	1.5	0	1.5	%/°C
dR_{ONdVH}	0	0.15	0	0.13	%/mV

9.8 On-Die Termination (ODT) Levels and I-V Characteristics

On-Die Termination effective resistance RTT is defined by bits A9, A6 and A2 of MR1 register.

ODT is applied to the DQ, DM, DQS/DQS and TDQS, TDQS (x8 devices only) pins.

A functional representation of the on-die termination is shown below. The individual pull-up and pull-down resistors (RTT_{pu} and RTT_{pd}) are defined as follows :

$$RTT_{pu} = \frac{V_{DDQ} - V_{OUT}}{|I_{out}|} \quad \text{under the condition that } RTT_{pd} \text{ is turned off}$$

$$RTT_{pd} = \frac{V_{OUT}}{|I_{out}|} \quad \text{under the condition that } RTT_{pu} \text{ is turned off}$$

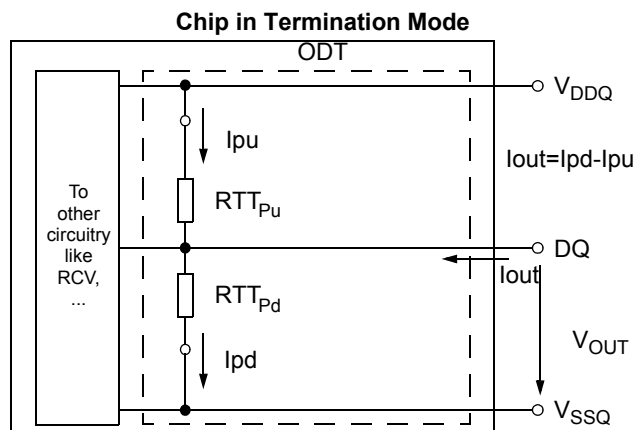


Figure 12. On-Die Termination : Definition of Voltages and Currents

9.8.1 ODT DC Electrical Characteristics

Table 25 provides an overview of the ODT DC electrical characteristics. The values for $RTT_{60pd120}$, $RTT_{60pu120}$, $RTT_{120pd240}$, $RTT_{120pu240}$, RTT_{40pd80} , RTT_{40pu80} , RTT_{30pd60} , RTT_{30pu60} , RTT_{20pd40} , RTT_{20pu40} are not specification requirements, but can be used as design guide lines:

[Table 25] ODT DC Electrical Characteristics, assuming $RZQ=240\Omega \pm 1\%$ entire operating temperature range; after proper ZQ calibration

MR1 (A9,A6,A2)	RTT	RESISTOR	Vout	Min	Nom	Max	Unit	NOTE
(0,1,0)	120 ohm	RTT _{120pd240}	V _{OL} (DC) 0.2XV _{DDQ}	0.6	1.0	1.1	R _{ZQ}	1,2,3,4
			0.5XV _{DDQ}	0.9	1.0	1.1	R _{ZQ}	1,2,3,4
			V _{OH} (DC) 0.8XV _{DDQ}	0.9	1.0	1.4	R _{ZQ}	1,2,3,4
		RTT _{120pu240}	V _{OL} (DC) 0.2XV _{DDQ}	0.9	1.0	1.4	R _{ZQ}	1,2,3,4
			0.5XV _{DDQ}	0.9	1.0	1.1	R _{ZQ}	1,2,3,4
			V _{OH} (DC) 0.8XV _{DDQ}	0.6	1.0	1.1	R _{ZQ}	1,2,3,4
		RTT ₁₂₀	V _{IL} (AC) to V _{IH} (AC)	0.9	1.0	1.6	R _{ZQ} /2	1,2,5
(0,0,1)	60 ohm	RTT _{60pd240}	V _{OL} (DC) 0.2XV _{DDQ}	0.6	1.0	1.1	R _{ZQ} /2	1,2,3,4
			0.5XV _{DDQ}	0.9	1.0	1.1	R _{ZQ} /2	1,2,3,4
			V _{OH} (DC) 0.8XV _{DDQ}	0.9	1.0	1.4	R _{ZQ} /2	1,2,3,4
		RTT _{60pu240}	V _{OL} (DC) 0.2XV _{DDQ}	0.9	1.0	1.4	R _{ZQ} /2	1,2,3,4
			0.5XV _{DDQ}	0.9	1.0	1.1	R _{ZQ} /2	1,2,3,4
			V _{OH} (DC) 0.8XV _{DDQ}	0.6	1.0	1.1	R _{ZQ} /2	1,2,3,4
		RTT ₆₀	V _{IL} (AC) to V _{IH} (AC)	0.9	1.0	1.6	R _{ZQ} /4	1,2,5
(0,1,1)	40 ohm	RTT _{40pd240}	V _{OL} (DC) 0.2XV _{DDQ}	0.6	1.0	1.1	R _{ZQ} /3	1,2,3,4
			0.5XV _{DDQ}	0.9	1.0	1.1	R _{ZQ} /3	1,2,3,4
			V _{OH} (DC) 0.8XV _{DDQ}	0.9	1.0	1.4	R _{ZQ} /3	1,2,3,4
		RTT _{40pu240}	V _{OL} (DC) 0.2XV _{DDQ}	0.9	1.0	1.4	R _{ZQ} /3	1,2,3,4
			0.5XV _{DDQ}	0.9	1.0	1.1	R _{ZQ} /3	1,2,3,4
			V _{OH} (DC) 0.8XV _{DDQ}	0.6	1.0	1.1	R _{ZQ} /3	1,2,3,4
		RTT ₄₀	V _{IL} (AC) to V _{IH} (AC)	0.9	1.0	1.6	R _{ZQ} /6	1,2,5
(1,0,1)	30 ohm	RTT _{60pd240}	V _{OL} (DC) 0.2XV _{DDQ}	0.6	1.0	1.1	R _{ZQ} /4	1,2,3,4
			0.5XV _{DDQ}	0.9	1.0	1.1	R _{ZQ} /4	1,2,3,4
			V _{OH} (DC) 0.8XV _{DDQ}	0.9	1.0	1.4	R _{ZQ} /4	1,2,3,4
		RTT _{60pu240}	V _{OL} (DC) 0.2XV _{DDQ}	0.9	1.0	1.4	R _{ZQ} /4	1,2,3,4
			0.5XV _{DDQ}	0.9	1.0	1.1	R _{ZQ} /4	1,2,3,4
			V _{OH} (DC) 0.8XV _{DDQ}	0.6	1.0	1.1	R _{ZQ} /4	1,2,3,4
		RTT ₆₀	V _{IL} (AC) to V _{IH} (AC)	0.9	1.0	1.6	R _{ZQ} /8	1,2,5
(1,0,0)	20 ohm	RTT _{60pd240}	V _{OL} (DC) 0.2XV _{DDQ}	0.6	1.0	1.1	R _{ZQ} /6	1,2,3,4
			0.5XV _{DDQ}	0.9	1.0	1.1	R _{ZQ} /6	1,2,3,4
			V _{OH} (DC) 0.8XV _{DDQ}	0.9	1.0	1.4	R _{ZQ} /6	1,2,3,4
		RTT _{60pu240}	V _{OL} (DC) 0.2XV _{DDQ}	0.9	1.0	1.4	R _{ZQ} /6	1,2,3,4
			0.5XV _{DDQ}	0.9	1.0	1.1	R _{ZQ} /6	1,2,3,4
			V _{OH} (DC) 0.8XV _{DDQ}	0.6	1.0	1.1	R _{ZQ} /6	1,2,3,4
		RTT ₆₀	V _{IL} (AC) to V _{IH} (AC)	0.9	1.0	1.6	R _{ZQ} /12	1,2,5
Deviation of V _M w.r.t V _{DDQ} /2, ΔVM				-5		5	%	1,2,5,6

NOTE :

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity
2. The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and that $V_{SSQ} = V_{SS}$
3. Pull-down and pull-up ODT resistors are recommended to be calibrated at $0.5XV_{DDQ}$. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at $0.2XV_{DDQ}$ and $0.8XV_{DDQ}$.
4. Not a specification requirement, but a design guide line
5. Measurement definition for R_{TT} :
Apply $V_{IH}(AC)$ to pin under test and measure current $I(V_{IH}(AC))$, then apply $V_{IL}(AC)$ to pin under test and measure current $I(V_{IL}(AC))$ respectively

$$R_{TT} = \frac{V_{IH}(AC) - V_{IL}(AC)}{I(V_{IH}(AC)) - I(V_{IL}(AC))}$$

6. Measurement definition for V_M and ΔV_M : Measure voltage (V_M) at test pin (midpoint) with no load

$$\Delta V_M = \left(\frac{2 \times V_M}{V_{DDQ}} - 1 \right) \times 100$$

9.8.2 ODT Temperature and Voltage sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to table below

$\Delta T = T - T(@\text{calibration})$; $\Delta V = V_{DDQ} - V_{DDQ}(@\text{calibration})$; $V_{DD} = V_{DDQ}$

[Table 26] ODT Sensitivity Definition

	Min	Max	Units
R_{TT}	$0.9 - dR_{TTdT} * \Delta T - dR_{TTdV} * \Delta V $	$1.6 + dR_{TTdT} * \Delta T + dR_{TTdV} * \Delta V $	RZQ/2,4,6,8,12

[Table 27] ODT Voltage and Temperature Sensitivity

	Min	Max	Units
dR_{TTdT}	0	1.5	%/°C
dR_{TTdV}	0	0.15	%/mV

NOTE : These parameters may not be subject to production test. They are verified by design and characterization.

9.9 ODT Timing Definitions

9.9.1 Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings is defined in Figure 13.

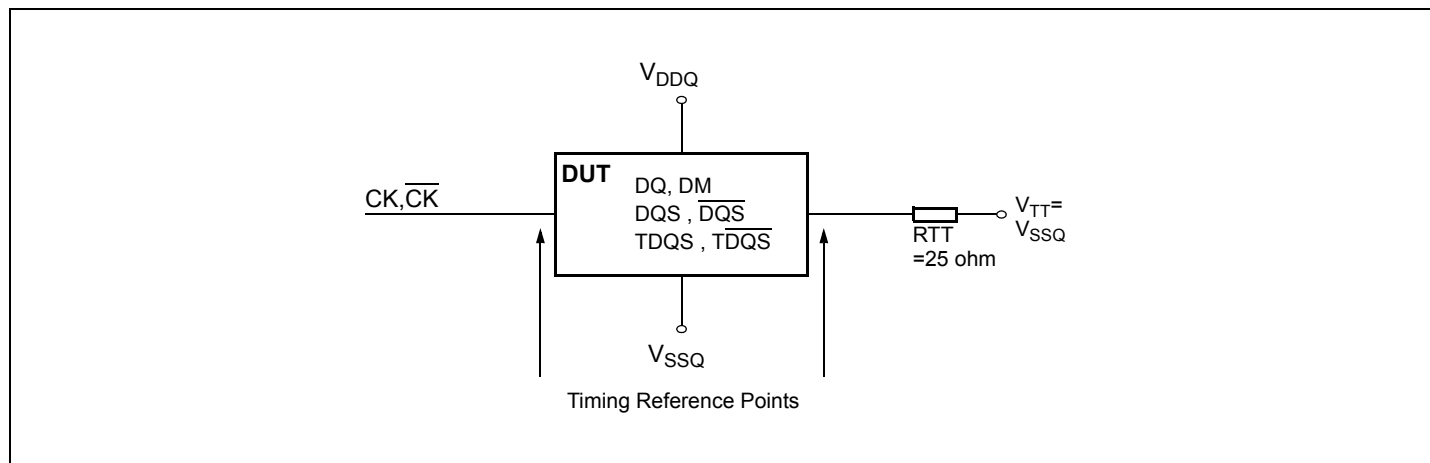


Figure 13. ODT Timing Reference Load

9.9.2 ODT Timing Definitions

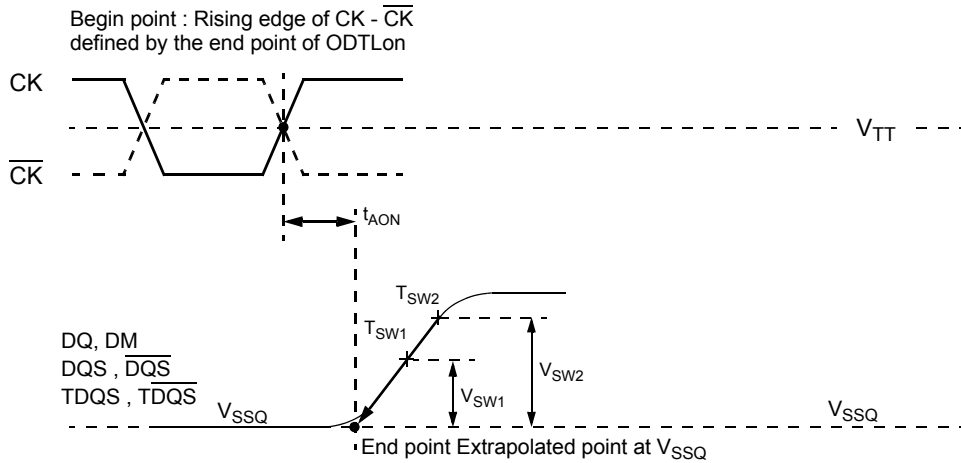
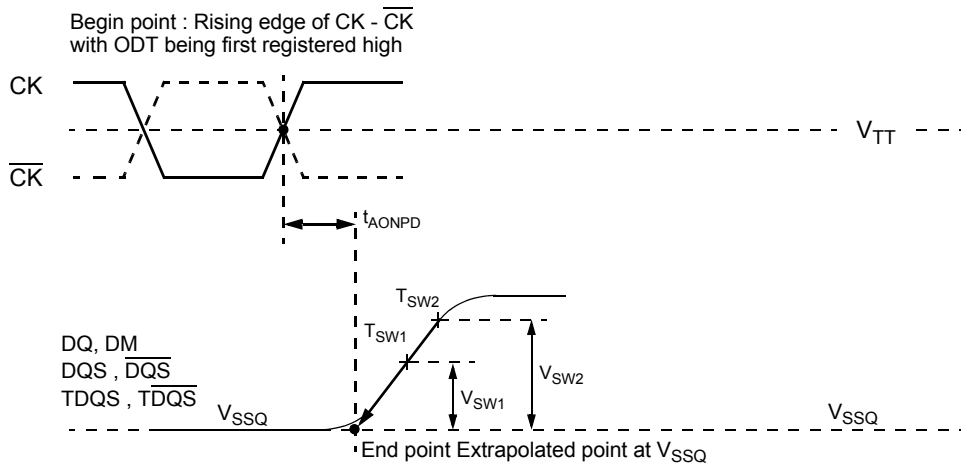
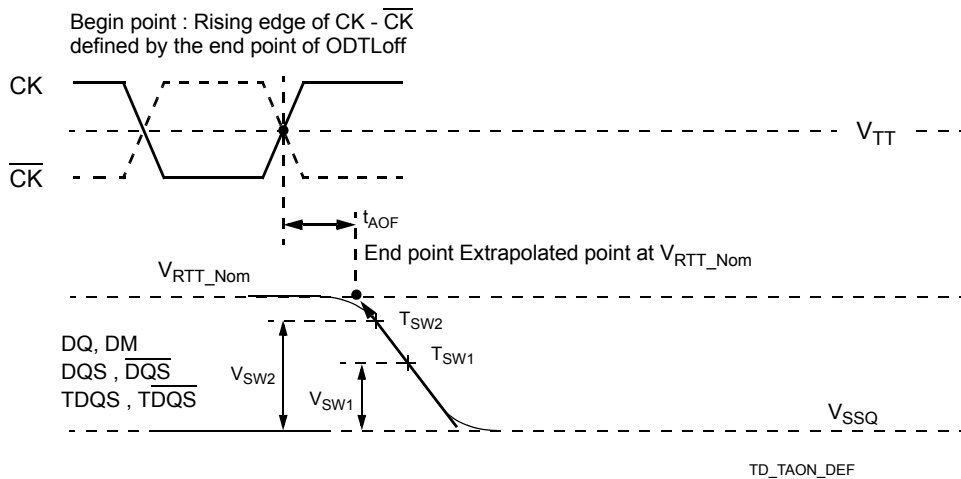
Definitions for tAON, tAONPD, tAOF, tAOFPD and tADC are provided in Table 28 and subsequent figures. Measurement reference settings are provided in Table 29.

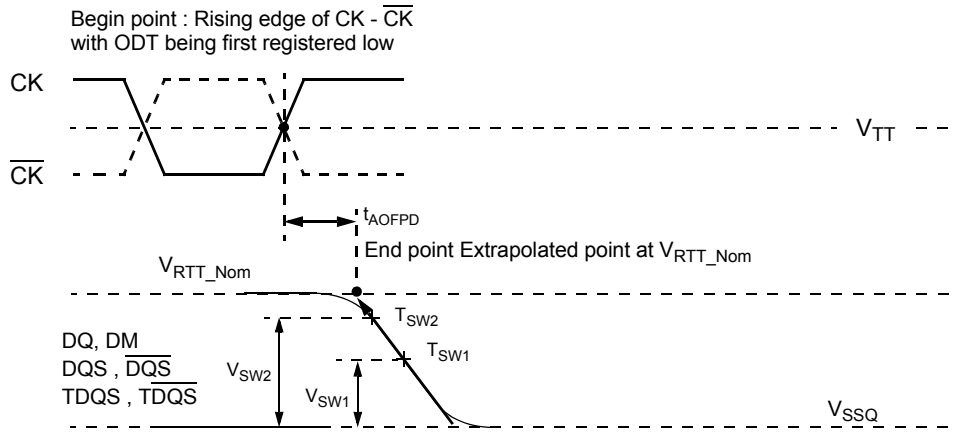
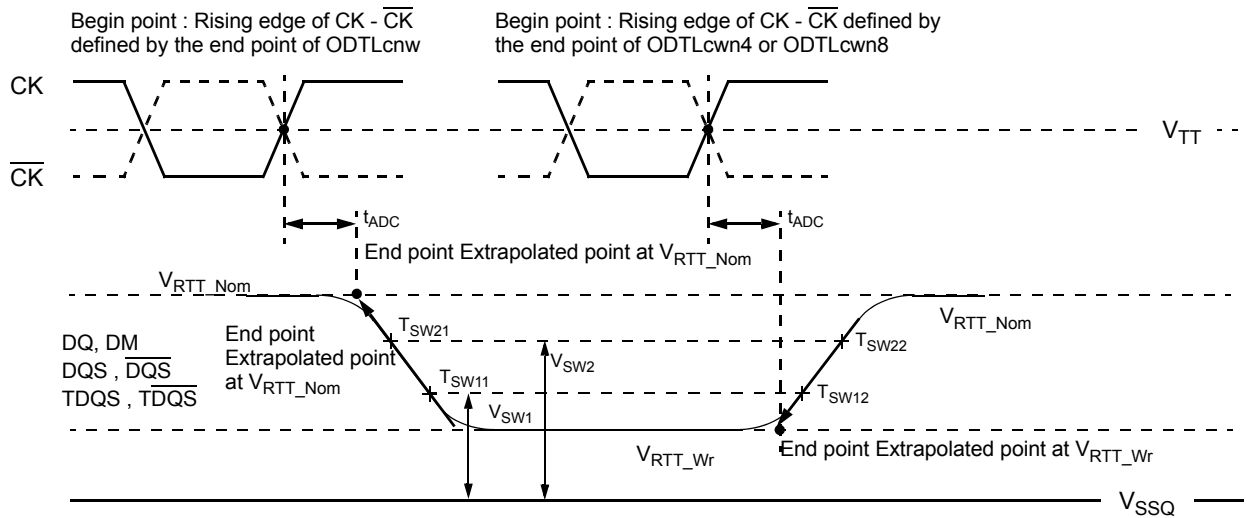
[Table 28] ODT Timing Definitions

Symbol	Begin Point Definition	End Point Definition	Figure
tAON	Rising edge of CK - $\overline{\text{CK}}$ defined by the end point of ODTLon	Extrapolated point at V_{SSQ}	Figure 14
tAONPD	Rising edge of CK - $\overline{\text{CK}}$ with ODT being first registered high	Extrapolated point at V_{SSQ}	Figure 15
tAOF	Rising edge of CK - $\overline{\text{CK}}$ defined by the end point of ODTLoff	End point: Extrapolated point at $V_{\text{RTT_Nom}}$	Figure 16
tAOFPD	Rising edge of CK - $\overline{\text{CK}}$ with ODT being first registered low	End point: Extrapolated point at $V_{\text{RTT_Nom}}$	Figure 17
tADC	Rising edge of CK - $\overline{\text{CK}}$ defined by the end point of ODTLcwn, ODTLcwn4 of ODTLcwn8	End point: Extrapolated point at $V_{\text{RTT_Wr}}$ and $V_{\text{RTT_Nom}}$ respectively	Figure 18

[Table 29] Reference Settings for ODT Timing Measurements

Measured Parameter	RTT_Nom Setting	RTT_Wr Setting	V _{sw1} [V]	V _{sw2} [V]	NOTE
tAON	$R_{\text{ZQ}}/4$	NA	0.05	0.10	
	$R_{\text{ZQ}}/12$	NA	0.10	0.20	
tAONPD	$R_{\text{ZQ}}/4$	NA	0.05	0.10	
	$R_{\text{ZQ}}/12$	NA	0.10	0.20	
tAOF	$R_{\text{ZQ}}/4$	NA	0.05	0.10	
	$R_{\text{ZQ}}/12$	NA	0.10	0.20	
tAOFPD	$R_{\text{ZQ}}/4$	NA	0.05	0.10	
	$R_{\text{ZQ}}/12$	NA	0.10	0.20	
tADC	$R_{\text{ZQ}}/12$	$R_{\text{ZQ}}/2$	0.20	0.30	

Figure 14. Definition of t_{AON} Figure 15. Definition of t_{AONPD} Figure 16. Definition of t_{AOF}

Figure 17. Definition of t_{AOFPD} Figure 18. Definition of t_{ADC}

10. IDD Current Measure Method

10.1 IDD Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined. Figure 19 shows the setup and test load for IDD and IDDQ measurements.

- **IDD currents** (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET, IDD6TC and IDD7) are measured as time-averaged currents with all V_{DD} balls of the gDDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.

- **IDDQ currents** (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all V_{DDQ} balls of the gDDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

Attention : IDDQ values cannot be directly used to calculate IO power of the gDDR3 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 20. In DRAM module application, IDDQ cannot be measured separately since V_{DD} and V_{DDQ} are using one merged-power layer in Module PCB.

For IDD and IDDQ measurements, the following definitions apply :

- "0" and "LOW" is defined as $V_{IN} \leq V_{ILAC}(\max)$.

- "1" and "HIGH" is defined as $V_{IN} \geq V_{IHAC}(\min)$.

- "FLOATING" is defined as inputs are $V_{REF} = V_{DD} / 2$.

- "Timing used for IDD and IDDQ Measured - Loop Patterns" are provided in Table 30

- "Basic IDD and IDDQ Measurement Conditions" are described in Table 31

- Detailed IDD and IDDQ Measurement-Loop Patterns are described in Table 32 on page 31 through Table 39.

- IDD Measurements are done after properly initializing the gDDR3 SDRAM. This includes but is not limited to setting

RON = RZQ/7 (34 Ohm in MR1);

Qoff = 0B (Output Buffer enabled in MR1);

RTT_Nom = RZQ/6 (40 Ohm in MR1);

RTT_Wr = RZQ/2 (120 Ohm in MR2);

TDQS Feature disabled in MR1

- **Attention :** The IDD and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.

- Define $\underline{D} = \{\underline{CS}, \underline{RAS}, \underline{CAS}, \underline{WE}\} := \{\text{HIGH}, \text{LOW}, \text{LOW}, \text{LOW}\}$

- Define $\underline{D} = \{\underline{CS}, \underline{RAS}, \underline{CAS}, \underline{WE}\} := \{\text{HIGH}, \text{HIGH}, \text{HIGH}, \text{HIGH}\}$

- RESET Stable time is : During a Cold Boot RESET (Initialization), current reading is valid once power is stable and RESET has been LOW for 1ms;
During Warm Boot RESET(while operating), current reading is valid after RESET has been LOW for 200ns + tRFC

[Table 30] Timing used for IDD and IDDQ Measured - Loop Patterns

Parameter	Bin	gDDR3-800	gDDR3-1066	gDDR3-1333	gDDR3-1600	gDDR3-1866	gDDR3-2133	Unit
		6-6-6	7-7-7	9-9-9	11-11-11	13-13-13	14-14-14	
tCKmin(IDD)		2.5	1.875	1.5	1.25	1.07	0.935	ns
CL(IDD)		6	7	9	11	13	14	nCK
tRCDmin(IDD)		6	7	9	11	13	14	nCK
tRCmin(IDD)		21	27	33	39	45	50	nCK
tRASmin(IDD)		15	20	24	28	32	36	nCK
tRPmin(IDD)		6	7	9	11	13	14	nCK
tFAW(IDD)	x16	20	27	30	32	33	38	nCK
tRRD(IDD)	x16	4	6	5	6	6	7	nCK
tRFC(IDD) - 512Mb		36	48	60	72	85	97	nCK
tRFC(IDD) - 1Gb		44	59	74	88	103	118	nCK
tRFC(IDD) - 2Gb		64	86	107	128	150	172	nCK
tRFC(IDD) - 4Gb		120	160	200	240	281	321	nCK
tRFC(IDD) - 8Gb		140	187	234	280	328	375	nCK

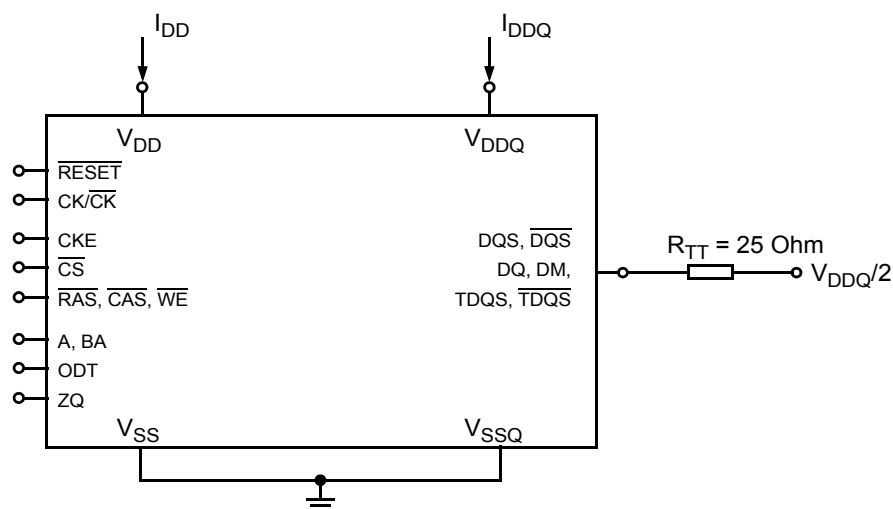


Figure 19. Measurement Setup and Test Load for IDD and IDDQ Measurements

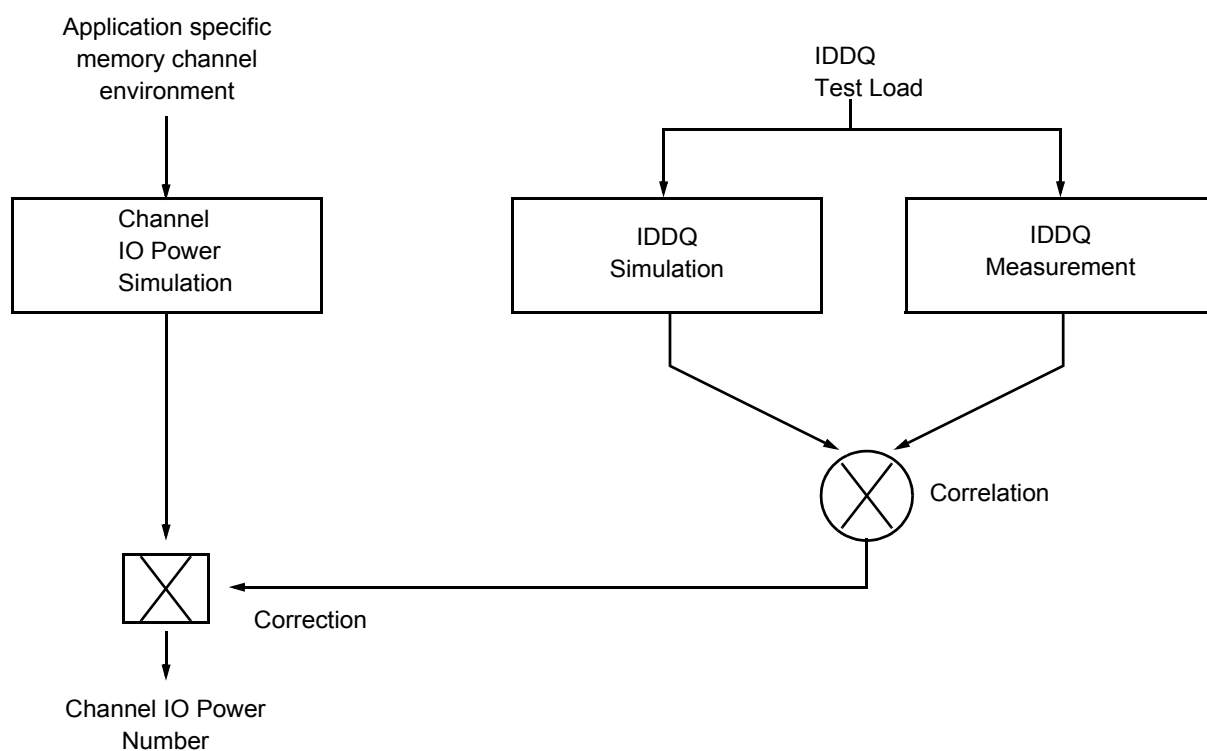


Figure 20. Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement.

[Table 31] Basic IDD and IDDQ Measurement Conditions

Symbol	Description
IDD0	Operating One Bank Active-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; CS: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling according to Table 32 on page 31 ; Data IO: FLOATING; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 32); Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pattern Details: see Table 32
IDD1	Operating One Bank Active-Read-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; CS: High between ACT, RD and PRE; Command, Address, Bank Address Inputs, Data IO: partially toggling according to Table 33 on page 32 ; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 33); Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pattern Details: see Table 33
IDD2N	Precharge Standby Current CKE: High; External clock: On; tCK, CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 34 on page 32 ; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pattern Details: see Table 34
IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 35 on page 33 ; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: toggling according to Table 35 ; Pattern Details: see Table 35
IDDQ2NT	Precharge Standby ODT IDDQ Current Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
IDD2P0	Precharge Power-Down Current Slow Exit CKE: Low; External clock: On; tCK, CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pre-charge Power Down Mode: Slow Exit ³⁾
IDD2P1	Precharge Power-Down Current Fast Exit CKE: Low; External clock: On; tCK, CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pre-charge Power Down Mode: Fast Exit ³⁾
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0
IDD3N	Active Standby Current CKE: High; External clock: On; tCK, CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 34 on page 32 ; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pattern Details: see Table 34
IDD3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0
IDD4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; CS: High between RD; Command, Address, Bank Address Inputs: partially toggling according to Table 36 on page 33 ; Data IO: seamless read data burst with different data between one burst and the next one according to Table 36 ; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 7 on page 12); Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pattern Details: see Table 36
IDDQ4R	Operating Burst Read IDDQ Current Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDD4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; CS: High between WR; Command, Address, Bank Address Inputs: partially toggling according to Table 37 on page 34 ; Data IO: seamless write data burst with different data between one burst and the next one according to Table 37; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see Table 37); Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at HIGH; Pattern Details: see Table 37
IDD5B	Burst Refresh Current CKE: High; External clock: On; tCK, CL, nRFC: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; CS: High between REF; Command, Address, Bank Address Inputs: partially toggling according to Table 38 on page 34 ; Data IO: FLOATING; DM: stable at 0; Bank Activity: REF command every nRFC (see Table 38); Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pattern Details: see Table 38
IDD6	Self Refresh Current: Normal Temperature Range TCASE: 0 - 85°C; Auto Self-Refresh (ASR): Disabled ⁴⁾ ; Self-Refresh Temperature Range (SRT): Normal ⁵⁾ ; CKE: Low; External clock: Off; CK and CK: LOW; CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; CS, Command, Address, Bank Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: FLOATING

[Table 31] Basic IDD and IDDQ Measurement Conditions

Symbol	Description
IDD7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: CL-1; CS: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling according to Table 39 on page 35 ; Data IO: read data bursts with different data between one burst and the next one according to Table 39 ; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 39 ; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pattern Details: see Table 39
IDD8	RESET Low Current RESET : Low; External clock : off; CK and CK : LOW; CKE : FLOATING ; CS, Command, Address, Bank Address, Data IO : FLOATING ; ODT Signal : FLOATING

NOTE :

- 1) Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B
- 2) Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B
- 3) Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12=1B for Fast Exit
- 4) Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature
- 5) Self-Refresh Temperature Range (SRT): set MR2 A7=0B for normal or 1B for extended temperature range
- 6) Read Burst type : Nibble Sequential, set MR0 A[3]=0B

[Table 32] IDD0 Measurement - Loop Pattern¹⁾

CK/CK	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²⁾
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{\text{D}}, \overline{\text{D}}$	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC + 0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC + 1, 2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC + 3, 4	$\overline{\text{D}}, \overline{\text{D}}$	1	1	1	1	0	0	00	0	0	F	0	-
			...	repeat pattern 1...4 until 1*nRC + nRAS - 1, truncate if necessary												
			1*nRC + nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	
			...	repeat 1...4 until 2*nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

NOTE :

1. DM must be driven LOW all the time. DQS, $\overline{\text{DQS}}$ are MID-LEVEL.
 2. DQ signals are MID-LEVEL.

[Table 33] IDD1 Measurement - Loop Pattern¹⁾

CK/CK	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²⁾
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRCD - 1, truncate if necessary												
			nRCD	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC + 1, 2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC + 3, 4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			...	repeat pattern nRC + 1,..., 4 until nRC + nRCD - 1, truncate if necessary												
			1*nRC + nRCD	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			...	repeat pattern nRC + 1,..., 4 until nRC + nRAS - 1, truncate if necessary												
			1*nRC + nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	repeat pattern nRC + 1,..., 4 until 2 * nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

NOTE :

- DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise MID-LEVEL.
- Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

[Table 34] IDD2 and IDD3N Measurement - Loop Pattern¹⁾

CK/CK	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²⁾
toggling	Static High	0	0	D	1	0	0	0	0	0	00	0	0	0	0	-
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2	$\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			3	$\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
		1	4-7	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	8-11	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	12-15	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	16-19	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	20-23	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	24-27	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	28-31	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

NOTE :

- DM must be driven Low all the time. DQS, $\overline{DQS}$ are MID-LEVEL.
- DQ signals are MID-LEVEL.

[Table 35] IDD2NT and IDDQ2NT Measurement - Loop Pattern¹⁾

CK/CK	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²⁾
toggling	Static High	0	0	D	1	0	0	0	0	0	00	0	0	0	0	-
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2	$\overline{\text{D}}$	1	1	1	1	0	0	00	0	0	F	0	-
			3	$\overline{\text{D}}$	1	1	1	1	0	0	00	0	0	F	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 1												
		2	8-11	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 2												
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 3												
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 4												
		5	20-23	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 5												
		6	24-27	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 6												
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 7												

NOTE :

1. DM must be driven Low all the time. DQS, $\overline{\text{DQS}}$ are MID-LEVEL.

2. DQ signals are MID-LEVEL.

[Table 36] IDD4R and IDDQ4R Measurement - Loop Pattern¹⁾

CK/CK	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²⁾
toggling	Static High	0	0	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2,3	$\overline{\text{D}}, \overline{\text{D}}$	1	1	1	1	0	0	00	0	0	0	0	-
			4	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	00	0	0	F	0	-
			6,7	$\overline{\text{D}}, \overline{\text{D}}$	1	1	1	1	0	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

NOTE :

1. DM must be driven LOW all the time. DQS, $\overline{\text{DQS}}$ are used according to WR Commands, otherwise MID-LEVEL.

2. Burst Sequence driven on each DQ signal by Write Command. Outside burst operation, DQ signals are MID-LEVEL.

[Table 37] IDD4W Measurement - Loop Pattern¹⁾

CK/CK	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²⁾
toggling	Static High	0	0	WR	0	1	0	0	1	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	00	0	0	0	0	-
			2,3	$\overline{\text{D}}, \overline{\text{D}}$	1	1	1	1	1	0	00	0	0	0	0	-
			4	WR	0	1	0	0	1	0	00	0	0	F	0	00110011
		5	5	D	1	0	0	0	1	0	00	0	0	F	0	-
			6,7	$\overline{\text{D}}, \overline{\text{D}}$	1	1	1	1	1	0	00	0	0	F	0	-
			8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

NOTE :

1. DM must be driven LOW all the time. DQS, $\overline{\text{DQS}}$ are used according to WR Commands, otherwise MID-LEVEL.
 2. Burst Sequence driven on each DQ signal by Write Command. Outside burst operation, DQ signals are MID-LEVEL.

[Table 38] IDD5B Measurement - Loop Pattern¹⁾

CK/CK	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²⁾
toggling	Static High	1	0	REF	0	0	0	1	0	0	00	0	0	0	0	-
			1,2	D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{\text{D}}, \overline{\text{D}}$	1	1	1	1	0	0	00	0	0	F	0	-
			5...8	repeat cycles 1...4, but BA[2:0] = 1												
			9...12	repeat cycles 1...4, but BA[2:0] = 2												
			13...16	repeat cycles 1...4, but BA[2:0] = 3												
			17...20	repeat cycles 1...4, but BA[2:0] = 4												
			21...24	repeat cycles 1...4, but BA[2:0] = 5												
			25...28	repeat cycles 1...4, but BA[2:0] = 6												
			29...32	repeat cycles 1...4, but BA[2:0] = 7												
		2	33...nRFC - 1	repeat Sub-Loop 1, until nRFC - 1. Truncate, if necessary.												

NOTE :

1. DM must be driven LOW all the time. DQS, $\overline{\text{DQS}}$ are MID-LEVEL.
 2. DQ signals are MID-LEVEL.

[Table 39] IDD7 Measurement - Loop Pattern¹⁾

CK/CK	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²⁾
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1	RDA	0	1	0	1	0	0	00	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	00	0	0	0	0	-
			...	repeat above D Command until nRRD - 1												
		1	nRRD	ACT	0	0	1	1	0	1	00	0	0	F	0	-
			nRRD + 1	RDA	0	1	0	1	0	1	00	1	0	F	0	00110011
			nRRD + 2	D	1	0	0	0	0	1	00	0	0	F	0	-
			...	repeat above D Command until 2*nRRD-1												
		2	2 * nRRD	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	3 * nRRD	repeat Sub-Loop 1, but BA[2:0] = 3												
		4	4 * nRRD	D	1	0	0	0	0	3	00	0	0	F	0	-
				Assert and repeat above D Command until nFAW - 1, if necessary												
		5	nFAW	repeat Sub-Loop 0, but BA[2:0] = 4												
		6	nFAW+nRRD	repeat Sub-Loop 1, but BA[2:0] = 5												
		7	nFAW+2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 6												
		8	nFAW+3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 7												
		9	nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	F	0	-
				Assert and repeat above D Command until 2*nFAW - 1, if necessary												
		10	2*nFAW+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			2*nFAW+1	RDA	0	1	0	1	0	0	00	1	0	F	0	00110011
			2*nFAW+2	D	1	0	0	0	0	0	00	0	0	F	0	-
				Repeat above D Command until 2*nFAW + nRRD - 1												
		11	2*nFAW+nRRD	ACT	0	0	1	1	0	1	00	0	0	0	0	-
			2*nFAW+nRRD+1	RDA	0	1	0	1	0	1	00	1	0	0	0	00000000
			2*nFAW+nRRD+2	D	1	0	0	0	0	1	00	0	0	0	0	-
				Repeat above D Command until 2*nFAW + 2*nRRD - 1												
		12	2*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 2												
		13	2*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 3												
		14	2*nFAW+4*nRRD	D	1	0	0	0	0	3	00	0	0	0	0	-
				Assert and repeat above D Command until 3*nFAW - 1, if necessary												
		15	3*nFAW	repeat Sub-Loop 10, but BA[2:0] = 4												
		16	3*nFAW+nRRD	repeat Sub-Loop 11, but BA[2:0] = 5												
		17	3*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 6												
		18	3*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 7												
		19	3*nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	0	0	-
				Assert and repeat above D Command until 4*nFAW - 1, if necessary												

NOTE :

- DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise MID-LEVEL.
- Burst Sequence driven on each DQ signal by Read Command. Outside burst operation. DQ signals are MID-LEVEL.

11. 2Gb gDDR3 SDRAM C-die IDD Specification Table

[Table 40] IDD Specification for 2Gb gDDR3 C-die

Symbol	128Mx16 (K4W2G1646C)				Unit	NOTE
	gDDR3-1333	gDDR3-1600	gDDR3-1866	gDDR3-2133		
	9-9-9	11-11-11	13-13-13	14-14-14		
IDD0	65	70	75	TBD	mA	
IDD1	90	95	100	TBD	mA	
IDD2P0(slow exit)	12	12	12	TBD	mA	
IDD2P1(fast exit)	25	25	25	TBD	mA	
IDD2N	30	30	30	TBD	mA	
IDD2NT	35	40	40	TBD	mA	
IDDQ2NT	95	95	95	TBD	mA	
IDD2Q	30	30	30	TBD	mA	
IDD3P	25	30	30	TBD	mA	
IDD3N	55	55	60	TBD	mA	
IDD4R	160	190	215	TBD	mA	
IDDQ4R	100	105	115	TBD	mA	
IDD4W	165	185	205	TBD	mA	
IDD5B	150	153	155	TBD	mA	
IDD6	12	12	12	TBD	mA	
IDD7	245	270	285	TBD	mA	
IDD8	12	12	12	TBD	mA	

12. Thermal Characteristics Table

(1333Mbps/1600Mbps/1866Mbps/2133Mbps at $V_{DD}=1.5V \pm 0.075V$, $V_{DDQ}=1.5V \pm 0.075V$)

Parameter	Description	Value	Units	NOTE
Theta_JA	Thermal resistance junction to ambient	27.53	°C/W	Thermal measurement : 1,2,3,5
Max_Tj	Maximum operating junction temperature	31.9	°C	1.333Gbps@Max 1.575V(Pd=0.25W)
		33.2		1.6Gbps@Max 1.575V(Pd=0.30W)
		34.3		1.866Gbps@Max 1.575V(Pd=0.34W)
Max_Tc	Maximum operating case temperature	30.5	°C	1.333Gbps@Max 1.575V
		31.6		1.6Gbps@Max 1.575V
		32.4		1.866Gbps@Max 1.575V
Theta_Jc	Thermal resistance junction to case	5.55	°C/W	Thermal measurement : 1, 6
Theta_JB	Thermal resistance junction to board	12.76	°C/W	Thermal simulation : 1, 2, 6

NOTE :

1. Measurement procedures for each parameter must follow standard procedures defined in the current JEDEC JESD-51 standard.
2. Theta_JA and Theta_JB must be measured with the high effective thermal conductivity test board defined in JESD51-7
3. Airflow information must be documented for Theta JA.
4. Max_Tj and Max_Tc are documented for normal operation in this table. These are not intended to reflect reliability limits.
5. Theta_JA should only be used for comparing the thermal performance of single packages and not for system related junction.
6. Theta_JB and Theta_JC are derived through a package thermal simulation and measurement.

13. Input/Output Capacitance

[Table 41] Input/Output Capacitance

Parameter	Symbol	gDDR3-800		gDDR3-1066		gDDR3-1333		gDDR3-1600		gDDR3-1866		gDDR3-2133		Units	NOTE
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Input/output capacitance (DQ, DM, DQS, $\overline{\text{DQS}}$, TDQS, $\overline{\text{TDQS}}$)	CIO	1.5	3.0	1.5	2.7	1.5	2.5	1.5	2.3	1.4	2.2	1.4	2.1	pF	1,2,3
Input capacitance (CK and $\overline{\text{CK}}$)	CCK	0.8	1.6	0.8	1.6	0.8	1.4	0.8	1.4	0.8	1.3	0.8	1.3	pF	2,3
Input capacitance delta (CK and $\overline{\text{CK}}$)	CDCK	0	0.15	0	0.15	0	0.15	0	0.15	0	0.15	0	0.15	pF	2,3,4
Input capacitance (All other input-only pins)	CI	0.75	1.5	0.75	1.5	0.75	1.3	0.75	1.3	0.75	1.2	0.75	1.2	pF	2,3,5
Input capacitance delta (DQS and $\overline{\text{DQS}}$)	CDDQS	0	0.2	0	0.2	0	0.15	0	0.15	0	0.15	0	0.15	pF	2,3,6
Input capacitance delta (All control input-only pins)	CDI_CTRL	-0.5	0.3	-0.5	0.3	-0.4	0.2	-0.4	0.2	-0.4	0.2	-0.4	0.2	pF	2,3,7,8
Input capacitance delta (all ADD and CMD input-only pins)	CDI_ADD_CMD	-0.5	0.5	-0.5	0.5	-0.4	0.4	-0.4	0.4	-0.4	0.4	-0.4	0.4	pF	2,3,9,10
Input/output capacitance delta (DQ, DM, DQS, $\overline{\text{DQS}}$, TDQS, $\overline{\text{TDQS}}$)	CDIO	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2,3,11
Input/output capacitance of ZQ pin	CZQ	-	3	-	3	-	3	-	3	-	3	-	3	pF	2, 3, 12

NOTE :

- Although the DM, TDQS and $\overline{\text{TDQS}}$ pins have different functions, the loading matches DQ and DQS
- This parameter is not subject to production test. It is verified by design and characterization.
The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with V_{DD} , V_{DDQ} , V_{SS} , V_{SSQ} applied and all other pins floating (except the pin under test, CKE, $\overline{\text{RESET}}$ and ODT as necessary). $V_{DD}=V_{DDQ}=1.5V$, $V_{BIAS}=V_{DD}/2$ and on-die termination off.
- This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
- Absolute value of $CCK-\overline{CCK}$
- Absolute value of $CIO(DQS)-CIO(\overline{DQS})$
- CI applies to ODT, $\overline{CS}$, CKE, A0-A15, BA0-BA2, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$.
- CDI_CTRL applies to ODT, $\overline{CS}$ and CKE
- $CDI_CTRL=C I(CTRL)-0.5*(C I(CLK)+C I(\overline{CLK}))$
- CDI_ADD_CMD applies to A0-A15, BA0-BA2, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$
- $CDI_ADD_CMD=C I(ADD_CMD)-0.5*(C I(CLK)+C I(\overline{CLK}))$
- $CDIO=C I O(DQ,DM)-0.5*(C I O(DQS)+C I O(\overline{DQS}))$
- Maximum external load capacitance on ZQ pin: 5pF

14. Electrical Characteristics and AC timing for gDDR3-800 to gDDR3-2133

14.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the gDDR3 SDRAM device.

14.1.1 Definition for tCK(avg)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$\left(\sum_{j=1}^N tCK_j \right) / N \quad N=200$$

14.1.2 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject to production test.

14.1.3 Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses:

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses:

$$\left(\sum_{j=1}^N tCH_j \right) / N \times tCK(avg) \quad N=200 \quad \left(\sum_{j=1}^N tCL_j \right) / N \times tCK(avg) \quad N=200$$

14.1.4 Definition for note for tJIT(per), tJIT(per, Ick)

tJIT(per) is defined as the largest deviation of any single tCK from tCK(avg). tJIT(per) = min/max of {tCK_i-tCK(avg) where i=1 to 200}

tJIT(per) defines the single period jitter when the DLL is already locked.

tJIT(per, lck) uses the same definition for single period jitter, during the DLL locking period only.

tJIT(per) and tJIT(per, lck) are not subject to production test.

14.1.5 Definition for tJIT(cc), tJIT(cc, Ick)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles: tJIT(cc) = Max of {tCK_{i+1}-tCK_i}

tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.

tJIT(cc, lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.

tJIT(cc) and tJIT(cc, lck) are not subject to production test.

14.1.6 Definition for tERR(nper)

tERR is defined as the cumulative error across n multiple consecutive cycles from tCK(avg). tERR is not subject to production test.

14.2 Refresh Parameters by Device Density

[Table 42] Refresh parameters by device density

Parameter	Symbol	1Gb	2Gb	4Gb	8Gb	Units	NOTE
All Bank Refresh to active/refresh cmd time	tRFC	110	160	300	350	ns	
Average periodic refresh interval	tREFI	0 °C ≤ T _{CASE} ≤ 85°C	7.8	7.8	7.8	μs	
		85 °C < T _{CASE} ≤ 95°C	3.9	3.9	3.9	μs	1

NOTE :

1. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if gDDR3 SDRAM devices support the following options or requirements referred to in this material.

14.3 Speed Bins and CL, tRCD, tRP, tRC and tRAS for corresponding Bin

gDDR3 SDRAM Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin.

[Table 43] gDDR3-800 Speed Bins

Speed			gDDR3-800		Units	NOTE
CL-nRCD-nRP			6 - 6 - 6			
Parameter		Symbol	min	max		
Internal read command to first data		tAA	15	20	ns	
ACT to internal read or write delay time		tRCD	15	-	ns	
PRE command period		tRP	15	-	ns	
ACT to ACT or REF command period		tRC	52.5	-	ns	
ACT to PRE command period		tRAS	37.5	9*tREFI	ns	
CL = 5	CWL = 5	tCK(AVG)	3.0	3.3	ns	1,2,3,4,11,12
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3
Supported CL Settings			5,6		nCK	
Supported CWL Settings			5		nCK	

[Table 44] DR3-1066 Speed Bins

Speed			gDDR3-1066		Units	NOTE
CL-nRCD-nRP			7 - 7 - 7			
Parameter	Symbol	min	max			
Internal read command to first data	tAA	13.125	20		ns	
ACT to internal read or write delay time	tRCD	13.125	-		ns	
PRE command period	tRP	13.125	-		ns	
ACT to ACT or REF command period	tRC	50.625	-		ns	
ACT to PRE command period	tRAS	37.5	9*tREFI		ns	
CL = 5	CWL = 5	tCK(AVG)	3.0	3.3	ns	1,2,3,4,5,11,12
	CWL = 6	tCK(AVG)	Reserved		ns	4
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3,5
	CWL = 6	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 7	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,4,10
CL = 8	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3
Supported CL Settings			5,6,7,8		nCK	
Supported CWL Settings			5,6		nCK	

[Table 45] gDDR3-1333 Speed Bins

Speed			gDDR3-1333		Units	NOTE
CL-nRCD-nRP			9 - 9 - 9			
Parameter	Symbol	min	max			
Internal read command to first data	tAA	13.5 (13.125) ¹⁰	20		ns	
ACT to internal read or write delay time	tRCD	13.5 (13.125) ¹⁰	-		ns	
PRE command period	tRP	13.5 (13.125) ¹⁰	-		ns	
ACT to ACT or REF command period	tRC	49.5 (49.125) ¹⁰	-		ns	
ACT to PRE command period	tRAS	36	9*tREFI		ns	
CL = 5	CWL = 5	tCK(AVG)	3.0	3.3	ns	1,2,3,4,6,11,12
	CWL = 6,7	tCK(AVG)	Reserved		ns	4
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3,6
	CWL = 6	tCK(AVG)	Reserved		ns	1,2,3,4,6
	CWL = 7	tCK(AVG)	Reserved		ns	4
CL = 7	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,4,6
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 8	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,6
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 9	CWL = 5,6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	<1.875	ns	1,2,3,4,10
CL = 10	CWL = 5,6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3
Supported CL Settings			5,6,7,8,9		nCK	
Supported CWL Settings			5,6,7		nCK	

[Table 46] gDDR3-1600 Speed Bins

Speed			gDDR3-1600		Units	NOTE
CL-nRCD-nRP			11-11-11			
Parameter	Symbol	min	max			
Internal read command to first data	tAA	13.75 (13.125) ¹⁰	20		ns	
ACT to internal read or write delay time	tRCD	13.75 (13.125) ¹⁰	-		ns	
PRE command period	tRP	13.75 (13.125) ¹⁰	-		ns	
ACT to ACT or REF command period	tRC	48.75 (48.125) ¹⁰	-		ns	
ACT to PRE command period	tRAS	35	9*tREFI		ns	
CL = 5	CWL = 5	tCK(AVG)	3.0	3.3	ns	1,2,3,4,7,11, 12
	CWL = 6,7,8	tCK(AVG)	Reserved		ns	4
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3,7
	CWL = 6	tCK(AVG)	Reserved		ns	1,2,3,4,7
	CWL = 7, 8	tCK(AVG)	Reserved		ns	4
CL = 7	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,4,7
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4,7
	CWL = 8	tCK(AVG)	Reserved		ns	4
CL = 8	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,7
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4,7
	CWL = 8	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 9	CWL = 5,6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	<1.875	ns	1,2,3,4,7
	CWL = 8	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 10	CWL = 5,6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	<1.875	ns	1,2,3,7
	CWL = 8	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 11	CWL = 5,6,7	tCK(AVG)	Reserved		ns	4
	CWL = 8	tCK(AVG)	1.25	<1.5	ns	1,2,3,10
Supported CL Settings			5,6,7,8,9,10,11		nCK	
Supported CWL Settings			5,6,7,8		nCK	

[Table 47] gDDR3-1866 Speed Bins

Speed			gDDR3-1866		Units	NOTE
CL-nRCD-nRP			13-13-13			
Parameter	Symbol	min	max			
Internal read command to first data	tAA	13.91 (13.125) ¹³	20		ns	
ACT to internal read or write delay time	tRCD	13.91 (13.125) ¹³	-		ns	
PRE command period	tRP	13.91 (13.125) ¹³	-		ns	
ACT to ACT or REF command period	tRC	47.91 (47.125) ¹³	-		ns	
ACT to PRE command period	tRAS	34	9*tREFI		ns	
CL = 5	CWL = 5	tCK(AVG)	3.0	3.3	ns	1,2,3,4,8,11, 12
	CWL = 6,7,8,9	tCK(AVG)	Reserved		ns	4
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3,8
	CWL = 6	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CWL = 7,8,9	tCK(AVG)	Reserved		ns	4
CL = 7	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	2.5	ns	1,2,3,4,8
	CWL = 7,8,9	tCK(AVG)	Reserved		ns	4
CL = 8	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,8
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CWL = 8,9	tCK(AVG)	Reserved		ns	4
CL = 9	CWL = 5,6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	1.875	ns	1,2,3,4,8
	CWL = 8	tCK(AVG)	Reserved		ns	4
	CWL = 9	tCK(AVG)	Reserved		ns	4
CL = 10	CWL = 5,6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	<1.875	ns	1,2,3,8
	CWL = 8	tCK(AVG)	Reserved		ns	1,2,3,4,8
CL = 11	CWL = 5,6,7	tCK(AVG)	Reserved		ns	4
	CWL = 8	tCK(AVG)	1.25	1.5	ns	1,2,3,4,8
	CWL = 9	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 12	CWL = 5,6,7,8	tCK(AVG)	Reserved		ns	4
	CWL = 9	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 13	CWL = 5,6,7,8	tCK(AVG)	Reserved		ns	4
	CWL = 9	tCK(AVG)	1.07	<1.25	ns	1,2,3,10
Supported CL Settings			5,6,7,8,9,10,11,13		nCK	
Supported CWL Settings			5,6,7,8,9		nCK	

[Table 48] gDDR3-2133 Speed Bins

Speed			gDDR3-2133		Units	NOTE
CL-nRCD-nRP			14-14-14			
Parameter	Symbol	min	max			
Internal read command to first data	tAA	13.09	20		ns	
ACT to internal read or write delay time	tRCD	13.09	-		ns	
PRE command period	tRP	13.09	-		ns	
ACT to ACT or REF command period	tRC	46.09	-		ns	
ACT to PRE command period	tRAS	33	9*tREFI		ns	
CL = 5	CWL = 5	tCK(AVG)	3.0	3.3	ns	1,2,3,4,9,11,12
	CWL = 6,7,8,9,10	tCK(AVG)	Reserved		ns	4
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3,9
	CWL = 6	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CWL = 7,8,9,10	tCK(AVG)	Reserved		ns	4
CL = 7	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,9
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CWL = 8,9,10	tCK(AVG)	Reserved		ns	4
CL = 8	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,9
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CWL = 8,9,10	tCK(AVG)	Reserved		ns	4
CL = 9	CWL = 5,6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	<1.875	ns	1,2,3,9
	CWL = 8	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CWL = 9,10	tCK(AVG)	Reserved		ns	4
CL = 10	CWL = 5,6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	<1.875	ns	1,2,3,9
	CWL = 8,9	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CWL = 10	tCK(AVG)	Reserved		ns	4
CL = 11	CWL = 5,6,7	tCK(AVG)	Reserved		ns	4
	CWL = 8	tCK(AVG)	1.25	<1.5	ns	1,2,3,9
	CWL = 9	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CWL = 10	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 12	CWL = 5,6,7,8	tCK(AVG)	Reserved		ns	4
	CWL = 9	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CWL = 10	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 13	CWL = 5,6,7,8	tCK(AVG)	Reserved		ns	4
	CWL = 9	tCK(AVG)	1.07	<1.25	ns	1,2,3,9
	CWL = 10	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 14	CWL = 5,6,7,8,9	tCK(AVG)	Reserved		ns	4
	CWL = 10	tCK(AVG)	0.935	<1.07	ns	1,2,3,10
Supported CL Settings			5,6,7,8,9,10,11,13,14		nCK	
Supported CWL Settings			5,6,7,8,9,10		nCK	

14.3.1 Speed Bin Table Notes

Absolute Specification (T_{OPER} ; $V_{\text{DDQ}} = V_{\text{DD}} = 1.5\text{V} \pm 0.075\text{V}$);

NOTE :

1. The CL setting and CWL setting result in $t_{\text{CK}}(\text{AVG})_{\text{MIN}}$ and $t_{\text{CK}}(\text{AVG})_{\text{MAX}}$ requirements. When making a selection of $t_{\text{CK}}(\text{AVG})$, both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. $t_{\text{CK}}(\text{AVG})_{\text{MIN}}$ limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard $t_{\text{CK}}(\text{AVG})$ value (2.5, 1.875, 1.5, or 1.25 ns) when calculating $\text{CL} [\text{nCK}] = t_{\text{AA}} [\text{ns}] / t_{\text{CK}}(\text{AVG}) [\text{ns}]$, rounding up to the next "Supported CL".
3. $t_{\text{CK}}(\text{AVG})_{\text{MAX}}$ limits: Calculate $t_{\text{CK}}(\text{AVG}) = t_{\text{AA}}_{\text{MAX}} / \text{CL}_{\text{SELECTED}}$ and round the resulting $t_{\text{CK}}(\text{AVG})$ down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is $t_{\text{CK}}(\text{AVG})_{\text{MAX}}$ corresponding to CL SELECTED.
4. "Reserved" settings are not allowed. User must program a different value.
5. Any gDDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
6. Any gDDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any gDDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any gDDR3-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Any gDDR3-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
10. For devices supporting optional downshift to CL=7 and CL=9, $t_{\text{AA}}/t_{\text{RCD}}/t_{\text{RP}}$ min must be 13.125 ns or lower. SPD settings must be programmed to match. For example, gDDR3-1333(CL9) devices supporting downshift to gDDR3-1066(CL7) should program 13.125 ns in SPD bytes for t_{AAmin} (Byte 16), t_{RCDmin} (Byte 18), and t_{RPmin} (Byte 20). gDDR3-1600(CL11) devices supporting downshift to gDDR3-1333(CL9) or gDDR3-1066(CL7) should program 13.125 ns in SPD bytes for t_{AAmin} (Byte16), t_{RCDmin} (Byte 18), and t_{RPmin} (Byte 20). gDDR3-1866(CL13) devices supporting downshift to gDDR3-1600(CL11) or gDDR3-1333(CL9) or gDDR3-1066(CL7) should program 13.125 ns in SPD bytes for t_{AAmin} (Byte16), t_{RCDmin} (Byte 18), and t_{RPmin} (Byte 20). gDDR3-2133(CL14) devices supporting downshift to gDDR3-1866(CL13) or gDDR3-1600(CL11) or gDDR3-1333(CL9) or gDDR3-1066(CL7) should program 13.125 ns in SPD bytes for t_{AAmin} (Byte16), t_{RCDmin} (Byte 18), and t_{RPmin} (Byte 20). Once t_{RP} (Byte 20) is programmed to 13.125ns, t_{RCmin} (Byte 21,23) also should be programmed accordingly. For example, 49.125ns ($t_{\text{RASmin}} + t_{\text{RPmin}} = 36\text{ns} + 13.125\text{ns}$) for gDDR3-1333(CL9) and 48.125ns ($t_{\text{RASmin}} + t_{\text{RPmin}} = 35\text{ns} + 13.125\text{ns}$) for gDDR3-1600(CL11).
11. gDDR3 800 AC timing apply if DRAM operates at lower than 800 MT/s data rate.
12. For CL5 support, refer to DIMM SPD information. DRAM is required to support CL5. CL5 is not mandatory in SPD coding.
13. For devices supporting optional down binning to CL=11, CL=9 and CL=7, $t_{\text{AA}}/t_{\text{RCD}}/t_{\text{RPmin}}$ must be 13.125ns. SPD setting must be programed to match. For example, gDDR3-1866 devices supporting down binning to gDDR3-1600 or gDDR3-1333 or 1066 should program 13.125ns in SPD bytes for t_{AAmin} (byte16), t_{RCDmin} (Byte18) and t_{RPmin} (byte20). Once t_{RP} (Byte20) is programmed to 13.125ns, t_{RCmin} (Byte21,23) also should be programmed accordingly. For example, 47.125ns ($t_{\text{RASmin}} + t_{\text{RPmin}} = 34\text{ns} + 13.125\text{ns}$)

15. Timing Parameters by Speed Grade

[Table 49] Timing Parameters by Speed Bins for gDDR3-800 to gDDR3-1333 (Cont.)

Speed		gDDR3-800		gDDR3-1066		gDDR3-1333		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	8	-	8	-	ns	6
Average Clock Period	tCK(avg)	See Speed Bins Table						ps	
Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ps	
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)	
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)	
Clock Period Jitter	tJIT(per)	-100	100	-90	90	-80	80	ps	
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-90	90	-80	80	-70	70	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	200		180		160		ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	180		160		140		ps	
Cumulative error across 2 cycles	tERR(2per)	- 147	147	- 132	132	- 118	118	ps	
Cumulative error across 3 cycles	tERR(3per)	- 175	175	- 157	157	- 140	140	ps	
Cumulative error across 4 cycles	tERR(4per)	- 194	194	- 175	175	- 155	155	ps	
Cumulative error across 5 cycles	tERR(5per)	- 209	209	- 188	188	- 168	168	ps	
Cumulative error across 6 cycles	tERR(6per)	- 222	222	- 200	200	- 177	177	ps	
Cumulative error across 7 cycles	tERR(7per)	- 232	232	- 209	209	- 186	186	ps	
Cumulative error across 8 cycles	tERR(8per)	- 241	241	- 217	217	- 193	193	ps	
Cumulative error across 9 cycles	tERR(9per)	- 249	249	- 224	224	- 200	200	ps	
Cumulative error across 10 cycles	tERR(10per)	- 257	257	- 231	231	- 205	205	ps	
Cumulative error across 11 cycles	tERR(11per)	- 263	263	- 237	237	- 210	210	ps	
Cumulative error across 12 cycles	tERR(12per)	- 269	269	- 242	242	- 215	215	ps	
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min tERR(nper)max = (1 + 0.68ln(n))*tJIT(per)max						ps	24
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	0.43	-	0.43	-	tCK(avg)	25
Absolute clock Low pulse width	tCL(abs)	0.43	-	0.43	-	0.43	-	tCK(avg)	26
Data Timing									
DQS, $\overline{\text{DQS}}$ to DQ skew, per group, per access	tDQSQ	-	200	-	150	-	125	ps	13
DQ output hold time from DQS, $\overline{\text{DQS}}$	tQH	0.38	-	0.38	-	0.38	-	tCK(avg)	13, g
DQ low-impedance time from CK, $\overline{\text{CK}}$	tLZ(DQ)	-800	400	-600	300	-500	250	ps	13,14, f
DQ high-impedance time from CK, $\overline{\text{CK}}$	tHZ(DQ)	-	400	-	300	-	250	ps	13,14, f
Data setup time to DQS, $\overline{\text{DQS}}$ referenced to V _{IH} (AC)V _{IL} (AC) levels	tDS(base) AC175	75	-	25	-	-	-	ps	d, 17
	tDS(base) AC150	125	-	75	-	30	-	ps	d, 17
Data hold time to DQS, $\overline{\text{DQS}}$ referenced to V _{IH} (AC)V _{IL} (AC) levels	tDH(base) DC100	150	-	100	-	65	-	ps	d, 17
DQ and DM Input pulse width for each input	tDIPW	600	-	490	-	400	-	ps	28
Data Strobe Timing									
DQS, $\overline{\text{DQS}}$ differential READ Preamble	tRPRE	0.9	NOTE 19	0.9	NOTE 19	0.9	NOTE 19	tCK	13, 19, g
DQS, $\overline{\text{DQS}}$ differential READ Postamble	tRPST	0.3	NOTE 11	0.3	NOTE 11	0.3	NOTE 11	tCK	11, 13, b
DQS, $\overline{\text{DQS}}$ differential output high time	tQSH	0.38	-	0.38	-	0.4	-	tCK(avg)	13, g
DQS, $\overline{\text{DQS}}$ differential output low time	tQSL	0.38	-	0.38	-	0.4	-	tCK(avg)	13, g
DQS, $\overline{\text{DQS}}$ differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	tCK	
DQS, $\overline{\text{DQS}}$ differential WRITE Postamble	tWPST	0.3	-	0.3	-	0.3	-	tCK	
DQS, $\overline{\text{DQS}}$ rising edge output access time from rising CK, $\overline{\text{CK}}$	tDQSCK	-400	400	-300	300	-255	255	ps	13,f
DQS, $\overline{\text{DQS}}$ low-impedance time (Referenced from RL-1)	tLZ(DQS)	-800	400	-600	300	-500	250	ps	13,14,f
DQS, $\overline{\text{DQS}}$ high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	400	-	300	-	250	ps	12,13,14
DQS, $\overline{\text{DQS}}$ differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	29, 31
DQS, $\overline{\text{DQS}}$ differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	30, 31
DQS, $\overline{\text{DQS}}$ rising edge to CK, $\overline{\text{CK}}$ rising edge	tDQSS	-0.25	0.25	-0.25	0.25	-0.25	0.25	tCK(avg)	c
DQS, $\overline{\text{DQS}}$ falling edge setup time to CK, $\overline{\text{CK}}$ rising edge	tDSS	0.2	-	0.2	-	0.2	-	tCK(avg)	c, 32
DQS, $\overline{\text{DQS}}$ falling edge hold time to CK, $\overline{\text{CK}}$ rising edge	tDSH	0.2	-	0.2	-	0.2	-	tCK(avg)	c, 32

[Table 49] Timing Parameters by Speed Bins for gDDR3-800 to gDDR3-1333 (Cont.)

Speed		gDDR3-800		gDDR3-1066		gDDR3-1333		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Command and Address Timing									
DLL locking time	tDLLK	512	-	512	-	512	-	nCK	
internal READ Command to PRECHARGE Command delay	tRTP	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		e
Delay from start of internal write transaction to internal read command	tWTR	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		e,18
WRITE recovery time	tWR	15	-	15	-	15	-	ns	e
Mode Register Set command cycle time	tMRD	4	-	4	-	4	-	nCK	
Mode Register Set command update delay	tMOD	max (12nCK,15ns)	-	max (12nCK,15ns)	-	max (12nCK,15ns)	-		
CAS# to CAS# command delay	tCCD	4	-	4	-	4	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup (tRP / tCK(AVG))						nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	nCK	22
ACTIVE to PRECHARGE command period	tRAS	See "Speed Bins and CL, tRCD, tRP, tRC and tRAS for corresponding Bin" on page 42						ns	e
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max (4nCK,10ns)	-	max (4nCK,7.5ns)	-	max (4nCK,6ns)	-		e
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max (4nCK,10ns)	-	max (4nCK,10ns)	-	max (4nCK,7.5ns)	-		e
Four activate window for 1KB page size	tFAW	40	-	37.5	-	30	-	ns	e
Four activate window for 2KB page size	tFAW	50	-	50	-	45	-	ns	e
Command and Address setup time to CK, $\overline{\text{CK}}$ referenced to $V_{IH}(\text{AC}) / V_{IL}(\text{AC})$ levels	tIS(base) AC175	200	-	125	-	65	-	ps	b,16
	tIS(base) AC150	200+150	-	125+150	-	65+125	-	ps	b,16,27
Command and Address hold time from CK, $\overline{\text{CK}}$ referenced to $V_{IH}(\text{AC}) / V_{IL}(\text{AC})$ levels	tIH(base) DC100	275	-	200	-	140	-	ps	b,16
Control & Address Input pulse width for each input	tIPW	900	-	780	-	620	-	ps	28
Calibration Timing									
Power-up and RESET calibration time	tZQinitl	512	-	512	-	512	-	nCK	
Normal operation Full calibration time	tZQoper	256	-	256	-	256	-	nCK	
Normal operation short calibration time	tZQCS	64	-	64	-	64	-	nCK	23
Reset Timing									
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC + 10ns)	-		
Self Refresh Timing									
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5nCK,tRF C + 10ns)	-	max(5nCK,tRF C + 10ns)	-	max(5nCK,tRF C + 10ns)	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-		

[Table 49] Timing Parameters by Speed Bins for gDDR3-800 to gDDR3-1333

Speed		gDDR3-800		gDDR3-1066		gDDR3-1333		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Power Down Timing									
Exit Power Down with DLL on to any valid command;Exit Pre-charge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (3nCK, 7.5ns)	-	max (3nCK, 7.5ns)	-	max (3nCK,6ns)	-		
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max (10nCK, 24ns)	-	max (10nCK, 24ns)	-	max (10nCK, 24ns)	-		2
CKE minimum pulse width	tCKE	max (3nCK, 7.5ns)	-	max (3nCK, 5.625ns)	-	max (3nCK, 5.625ns)	-		
Command pass disable delay	tCPDED	1	-	1	-	1	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCK	15
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	1	-	nCK	20
Timing of PRE command to Power Down entry	tPRPDEN	1	-	1	-	1	-	nCK	20
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 + 1	-	RL + 4 + 1	-	RL + 4 + 1	-		
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRPDEN	WL + 4 +(tWR/ tCK(avg))	-	WL + 4 +(tWR/ tCK(avg))	-	WL + 4 +(tWR/ tCK(avg))	-	nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRAPDEN	WL+4+WR +1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK	10
Timing of WR command to Power Down entry (BL4MRS)	tWRPDEN	WL + 2 +(tWR/ tCK(avg))	-	WL + 2 +(tWR/ tCK(avg))	-	WL + 2 +(tWR/ tCK(avg))	-	nCK	9
Timing of WRA command to Power Down entry (BL4MRS)	tWRAPDEN	WL +2 +WR +1	-	WL + 2 +WR +1	-	WL + 2 +WR +1	-	nCK	10
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	1	-		20,21
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
ODT Timing									
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	2	8.5	2	8.5	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	2	8.5	2	8.5	ns	
RTT turn-on	tAON	-400	400	-300	300	-250	250	ps	7,f
RTT_NOM and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	8,f
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	f
Write Leveling Timing									
First DQS pulse rising edge after tDQSS margining mode is programmed	tWLMRD	40	-	40	-	40	-	tCK	3
DQS/DQS delay after tDQS margining mode is programmed	tWLDQSEN	25	-	25	-	25	-	tCK	3
Write leveling setup time from rising CK, CK crossing to rising DQS, DQS crossing	tWLS	325	-	245	-	195	-	ps	
Write leveling hold time from rising DQS, DQS crossing to rising CK, CK crossing	tWLH	325	-	245	-	195	-	ps	
Write leveling output delay	tWLO	0	9	0	9	0	9	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	ns	

[Table 50] Timing Parameters by Speed Bins for gDDR3-1600 to gDDR3-2133 (Cont.)

Speed		gDDR3-1600		gDDR3-1866		gDDR3-2133		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	8	-	8	-	ns	6
Average Clock Period	tCK(avg)	See Speed Bins Table						ps	
Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ps	
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)	
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)	
Clock Period Jitter	tJIT(per)	-70	70	-60	60	-50	50	ps	
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-60	60	-50	50	-40	40	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	140		120		100		ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	120		100		80		ps	
Cumulative error across 2 cycles	tERR(2per)	-103	103	-88	88	-74	74	ps	
Cumulative error across 3 cycles	tERR(3per)	-122	122	-105	105	-87	87	ps	
Cumulative error across 4 cycles	tERR(4per)	-136	136	-117	117	-97	97	ps	
Cumulative error across 5 cycles	tERR(5per)	-147	147	-126	126	-105	105	ps	
Cumulative error across 6 cycles	tERR(6per)	-155	155	-133	133	-111	111	ps	
Cumulative error across 7 cycles	tERR(7per)	-163	163	-139	139	-116	116	ps	
Cumulative error across 8 cycles	tERR(8per)	-169	169	-145	145	-121	121	ps	
Cumulative error across 9 cycles	tERR(9per)	-175	175	-150	150	-125	125	ps	
Cumulative error across 10 cycles	tERR(10per)	-180	180	-154	154	-128	128	ps	
Cumulative error across 11 cycles	tERR(11per)	-184	184	-158	158	-132	132	ps	
Cumulative error across 12 cycles	tERR(12per)	-188	188	-161	161	-134	134	ps	
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min tERR(nper)max = (1 + 0.68ln(n))*tJIT(per)max						ps	24
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	0.43	-	0.43	-	tCK(avg)	25
Absolute clock Low pulse width	tCL(abs)	0.43	-	0.43	-	0.43	-	tCK(avg)	26
Data Timing									
DQS, $\overline{\text{DQS}}$ to DQ skew, per group, per access	tDQSQ	-	100	-	85	-	75	ps	13
DQ output hold time from DQS, $\overline{\text{DQS}}$	tQH	0.38	-	0.38	-	0.38	-	tCK(avg)	13, g
DQ low-impedance time from CK, $\overline{\text{CK}}$	tLZ(DQ)	-450	225	-390	195	-360	180	ps	13, 14, f
DQ high-impedance time from CK, $\overline{\text{CK}}$	tHZ(DQ)	-	225	-	195	-	180	ps	13, 14, f
Data setup time to DQS, $\overline{\text{DQS}}$ referenced to V _{IH} (AC)V _{IL} (AC) levels	tDS(base) AC175	-	-	-	-	-	-	ps	d, 17
	tDS(base) AC150	10	-	-	-	-	-	ps	d, 17
	tDS(base) AC135	-	-	0	-	-15	-	ps	d, 17
Data hold time to DQS, $\overline{\text{DQS}}$ referenced to V _{IH} (AC)V _{IL} (AC) levels	tDH(base) DC100	45	-	20	-	5	-	ps	d, 17
DQ and DM Input pulse width for each input	tDIPW	360	-	320	-	280	-	ps	28
Data Strobe Timing									
DQS, $\overline{\text{DQS}}$ differential READ Preamble	tRPRE	0.9	NOTE 19	0.9	NOTE 19	0.9	NOTE 19	tCK	13, 19, g
DQS, $\overline{\text{DQS}}$ differential READ Postamble	tRPST	0.3	NOTE 11	0.3	NOTE 11	0.3	NOTE 11	tCK	11, 13, b
DQS, $\overline{\text{DQS}}$ differential output high time	tQSH	0.4	-	0.4	-	0.4	-	tCK(avg)	13, g
DQS, $\overline{\text{DQS}}$ differential output low time	tQSL	0.4	-	0.4	-	0.4	-	tCK(avg)	13, g
DQS, $\overline{\text{DQS}}$ differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	tCK	
DQS, $\overline{\text{DQS}}$ differential WRITE Postamble	tWPST	0.3	-	0.3	-	0.3	-	tCK	
DQS, $\overline{\text{DQS}}$ rising edge output access time from rising CK, $\overline{\text{CK}}$	tDQSCK	-225	225	-195	195	-180	180	ps	13, f
DQS, $\overline{\text{DQS}}$ low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-390	195	-360	180	ps	13, 14, f
DQS, $\overline{\text{DQS}}$ high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	-	195	-	180	ps	12, 13, 14
DQS, $\overline{\text{DQS}}$ differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	29, 31
DQS, $\overline{\text{DQS}}$ differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	30, 31
DQS, $\overline{\text{DQS}}$ rising edge to CK, $\overline{\text{CK}}$ rising edge	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK(avg)	c
DQS, $\overline{\text{DQS}}$ falling edge setup time to CK, $\overline{\text{CK}}$ rising edge	tDSS	0.18	-	0.18	-	0.18	-	tCK(avg)	c, 32
DQS, $\overline{\text{DQS}}$ falling edge hold time to CK, $\overline{\text{CK}}$ rising edge	tDSH	0.18	-	0.18	-	0.18	-	tCK(avg)	c, 32

[Table 50] Timing Parameters by Speed Bins for gDDR3-1600 to gDDR3-2133 (Cont.)

Speed		gDDR3-1600		gDDR3-1866		gDDR3-2133		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Command and Address Timing									
DLL locking time	tDLLK	512	-	512	-	512	-	nCK	
internal READ Command to PRECHARGE Command delay	tRTP	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		e
Delay from start of internal write transaction to internal read command	tWTR	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		e,18
WRITE recovery time	tWR	15	-	15	-	15	-	ns	e
Mode Register Set command cycle time	tMRD	4	-	4	-	4	-	nCK	
Mode Register Set command update delay	tMOD	max (12nCK,15ns)	-	max (12nCK,15ns)	-	max (12nCK,15ns)	-		
CAS# to CAS# command delay	tCCD	4	-	4	-	4	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup (tRP / tCK(AVG))						nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	nCK	22
ACTIVE to PRECHARGE command period	tRAS	See "Speed Bins and CL, tRCD, tRP, tRC and tRAS for corresponding Bin" on page 42						ns	e
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max (4nCK,6ns)	-	max (4nCK, 5ns)	-	max (4nCK, 5ns)	-		e
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max (4nCK,7.5ns)	-	max (4nCK, 6ns)	-	max (4nCK, 6ns)	-		e
Four activate window for 1KB page size	tFAW	30	-	27	-	25	-	ns	e
Four activate window for 2KB page size	tFAW	40	-	35	-	35	-	ns	e
Command and Address setup time to CK, $\overline{\text{CK}}$ referenced to $V_{IH}(\text{AC}) / V_{IL}(\text{AC})$ levels	tIS(base) AC175	45	-	-	-	-	-	ps	b,16
	tIS(base) AC150	45+125	-	-	-	-	-	ps	b,16
	tIS(base) AC135	-	-	65	-	60	-	ps	b,16
	tIS(base) AC125	-	-	150	-	135	-	ps	b,16,27
Command and Address hold time from CK, $\overline{\text{CK}}$ referenced to $V_{IH}(\text{AC}) / V_{IL}(\text{AC})$ levels	tIH(base) DC100	120	-	100	-	95	-	ps	b,16
Control & Address Input pulse width for each input	tIPW	560	-	535	-	470	-	ps	28
Calibration Timing									
Power-up and RESET calibration time	tZQinitl	512	-	max(512nCK,640ns)	-	max(512nCK,640ns)	-	nCK	
Normal operation Full calibration time	tZQoper	256	-	max(256nCK,320ns)	-	max(256nCK,320ns)	-	nCK	
Normal operation short calibration time	tZQCS	64	-	max(64nCK,80ns)	-	max(64nCK,80ns)	-	nCK	23
Reset Timing									
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC(min) + 10ns)	-	max(5nCK, tRFC(min) + 10ns)	-		
Self Refresh Timing									
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5nCK,tRFC + 10ns)	-	max(5nCK,tRFC(min) + 10ns)	-	max(5nCK,tRFC(min) + 10ns)	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min) + 1tCK	-	tCKE(min) + 1nCK	-	tCKE(min) + 1nCK	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-		

[Table 50] Timing Parameters by Speed Bins for gDDR3-1600 to gDDR3-2133

Speed		gDDR3-1600		gDDR3-1866		gDDR3-2133		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Power Down Timing									
Exit Power Down with DLL on to any valid command;Exit Pre-charge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (3nCK,6ns)	-	max(3nCK,6ns)	-	max(3nCK,6ns)	-		
Exit Precharge Power Down with DLL frozen to commands re-quiring a locked DLL	tXPDLL	max (10nCK,24ns)	-	max(10nCK,24 ns)	-	max(10nCK,2 4ns)	-		2
CKE minimum pulse width	tCKE	max (3nCK,5ns)	-	max(3nCK,5ns)	-	max(3nCK,5n s)	-		
Command pass disable delay	tCPDED	1	-	2	-	2	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCK	15
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	2	-	nCK	20
Timing of PRE command to Power Down entry	tPRPDEN	1	-	1	-	2	-	nCK	20
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 + 1	-	RL + 4 + 1	-	RL + 4 + 1	-		
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL + 4 +(tWR/ tCK(avg))	-	WL + 4 +(tWR/ tCK(avg))	-	WL + 4 +(tWR/ tCK(avg))	-	nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL + 4 +WR +1	-	WL + 4 +WR +1	-	WL + 4 +WR +1	-	nCK	10
Timing of WR command to Power Down entry (BL4MRS)	tWRPDEN	WL + 2 +(tWR/ tCK(avg))	-	WL + 2 +(tWR/ tCK(avg))	-	WL + 2 +(tWR/ tCK(avg))	-	nCK	9
Timing of WRA command to Power Down entry (BL4MRS)	tWRAPDEN	WL +2 +WR +1	-	WL +2 +WR +1	-	WL +2 +WR +1	-	nCK	10
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	2	-		20,21
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
ODT Timing									
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL fro-zen)	tAONPD	2	8.5	2	8.5	2	8.5	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL fro-zen)	tAOFPD	2	8.5	2	8.5	2	8.5	ns	
RTT turn-on	tAON	-225	225	-195	195	-180	180	ps	7,f
RTT_NOM and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	8,f
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	f
Write Leveling Timing									
First DQS pulse rising edge after tDQSS margining mode is pro-grammed	tWLMRD	40	-	40	-	40	-	tCK	3
DQS/DQS delay after tDQS margining mode is programmed	tWLDQSEN	25	-	25	-	25	-	tCK	3
Write leveling setup time from rising CK, CK crossing to rising DQS, DQS crossing	tWLS	165	-	140	-	125	-	ps	
Write leveling hold time from rising DQS, DQS crossing to rising CK, CK crossing	tWLH	165	-	140	-	125	-	ps	
Write leveling output delay	tWLO	0	7.5	0	7.5	0	7.5	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	ns	

15.1 Jitter Notes

- Specific Note a** Unit 'tCK(avg)' represents the actual tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.ex) tMRD = 4 [nCK] means; if one Mode Register Set command is registered at Tm, another Mode Register Set command may be registered at Tm+4, even if (Tm+4 - Tm) is 4 x tCK(avg) + tERR(4per),min.
- Specific Note b** These parameters are measured from a command/address signal (CKE, $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/ $\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
- Specific Note c** These parameters are measured from a data strobe signal (DQS(L/U), $\overline{\text{DQS}}$ (L/U)) crossing to its respective clock signal (CK, $\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
- Specific Note d** These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc.) transition edge to its respective data strobe signal (DQS(L/U), $\overline{\text{DQS}}$ (L/U)) crossing.
- Specific Note e** For these parameters, the gDDR3 SDRAM device supports tnPARAM [nCK] = RU{ tPARAM [ns] / tCK(avg) [ns] }, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support tnRP = RU{tRP / tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For gDDR3-800 6-6-6, of which tRP = 15ns, the device will support tnRP = RU{tRP / tCK(avg)} = 6, as long as the input clock jitter specifications are met, i.e. Pre-charge command at Tm and Active command at Tm+6 is valid even if (Tm+6 - Tm) is less than 15ns due to input clock jitter.
- Specific Note f** When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(mper),act of the input clock, where 2 ≤ m ≤ 12. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a gDDR3-800 SDRAM has tERR(mper),act,min = - 172 ps and tERR(mper),act,max = + 193 ps, then tDQSCK,min(derated) = tDQSCK,min - tERR(mper),act,max = - 400 ps - 193 ps = - 593 ps and tDQSCK,max(derated) = tDQSCK,max - tERR(mper),act,min = 400 ps + 172 ps = + 572 ps. Similarly, tLZ(DQ) for gDDR3-800 derates to tLZ(DQ),min(derated) = - 800 ps - 193 ps = - 993 ps and tLZ(DQ),max(derated) = 400 ps + 172 ps = + 572 ps. (Caution on the min/max usage!)
- Note that tERR(mper),act,min is the minimum measured value of tERR(nper) where 2 ≤ n ≤ 12, and tERR(mper),act,max is the maximum measured value of tERR(nper) where 2 ≤ n ≤ 12.
- Specific Note g** When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per),act of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a gDDR3-800 SDRAM has tCK(avg),act = 2500 ps, tJIT(per),act,min = - 72 ps and tJIT(per),act,max = + 93 ps, then tRPRE,min(derated) = tRPRE,min + tJIT(per),act,min = 0.9 x tCK(avg),act + tJIT(per),act,min = 0.9 x 2500 ps - 72 ps = + 2178 ps. Similarly, tQH,min(derated) = tQH,min + tJIT(per),act,min = 0.38 x tCK(avg),act + tJIT(per),act,min = 0.38 x 2500 ps - 72 ps = + 878 ps. (Caution on the min/max usage!)

15.2 Timing Parameter Notes

1. Actual value dependant upon measurement level definitions which are TBD.
2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register
5. Value must be rounded-up to next higher integer value
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
7. For definition of RTT turn-on time tAON see "Device Operation & Timing Diagram Datasheet"
8. For definition of RTT turn-off time tAOF see "Device Operation & Timing Diagram Datasheet".
9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
10. WR in clock cycles as programmed in MR0
11. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. See "Device Operation & Timing Diagram Datasheet".
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD
13. Value is only valid for RON34
14. Single ended signal parameter. Refer to chapter 8 and chapter 9 for definition and measurement method.
15. tREFI depends on T_{OPER}
16. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, $\overline{\text{CK}}$ differential slew rate, Note for DQ and DM signals, $V_{\text{REF}}(\text{DC}) = V_{\text{REFDQ}}(\text{DC})$. For input only pins except RESET, $V_{\text{REF}}(\text{DC}) = V_{\text{REFCA}}(\text{DC})$.
See "Address/Command Setup, Hold and Derating ." on page 54. .
17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, $\overline{\text{DQS}}$ differential slew rate. Note for DQ and DM signals, $V_{\text{REF}}(\text{DC}) = V_{\text{REFDQ}}(\text{DC})$. For input only pins except RESET, $V_{\text{REF}}(\text{DC}) = V_{\text{REFCA}}(\text{DC})$.
See "Data Setup, Hold and Slew Rate Derating ." on page 61.
18. Start of internal write transaction is defined as follows ;
For BL8 (fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL
For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL
19. The maximum read preamble is bound by tLZDQS(min) on the left side and tDQSCK(max) on the right side. See "Device Operation & Timing Diagram Datasheet"
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
21. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required. See "Device Operation & Timing Diagram Datasheet".
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct a minimum of 0.5 % (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application specific parameters.
One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{TSens} \times \text{Tdriftrate}) + (\text{VSens} \times \text{Vdriftrate})}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5% / °C, VSens = 0.15% / mV, Tdriftrate = 1°C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128\text{ms}$$

24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.
25. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
26. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
27. The tIS(base) AC150 specifications are adjusted from the tIS(base) AC175 specification by adding an additional 125 ps for gDDR3-800/1066 or 100ps for gDDR3-1333/1600 of derating to accommodate for the lower alternate threshold of 150mV and another 25ps to account for the earlier reference point [(175mV - 150 mV) / 1 V/ns].
28. Pulse width of a input signal is defined as the width between the first crossing of V_{REF}(DC) and the consecutive crossing of V_{REF}(DC)
29. tDQSL describes the instantaneous differential input low pulse width on DQS- $\overline{\text{DQS}}$, as measured from one falling edge to the next consecutive rising edge.
30. tDQSH describes the instantaneous differential input high pulse width on DQS- $\overline{\text{DQS}}$, as measured from one rising edge to the next consecutive falling edge.
31. tDQSH, act + tDQSL, act = 1 tCK, act ; with tXYZ, act being the actual measured value of the respective timing parameter in the application.
32. tDSH, act + tDSS, act = 1 tCK, act ; with tXYZ, act being the actual measured value of the respective timing parameter in the application.
33. The tIS(base) AC125 specifications are adjusted from the tIS(base) AC135 specification by adding an additional 75ps for gDDR3-1866 and 65ps for gDDR3-2133 to accommodate for the lower alternate threshold of 125mV and another 10ps to account for the earlier reference point [(135mV - 125mV) / 1 V/ns].

15.3 Address/Command Setup, Hold and Derating :

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value (see Table 51) to the ΔtIS and ΔtIH derating value (see Table 52) respectively.

Example: tIS (total setup time) = tIS(base) + ΔtIS Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF}(DC)$ and the first crossing of $V_{IH}(AC)_{min}$. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF}(DC)$ and the first crossing of $V_{IL}(AC)_{max}$. If the actual signal is always earlier than the nominal slew rate line between shaded ' $V_{REF}(DC)$ to ac region', use nominal slew rate for derating value (see Figure 21). If the actual signal is later than the nominal slew rate line anywhere between shaded ' $V_{REF}(DC)$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 23).

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL}(DC)_{max}$ and the first crossing of $V_{REF}(DC)$. Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH}(DC)_{min}$ and the first crossing of $V_{REF}(DC)$. If the actual signal is always later than the nominal slew rate line between shaded 'dc to $V_{REF}(DC)$ region', use nominal slew rate for derating value (see Figure 22). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF}(DC)$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF}(DC)$ level is used for derating value (see Figure 24).

For a valid transition the input signal has to remain above/below $V_{IH/IL}(AC)$ for some time tVAC (see Table 56).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL}(AC)$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL}(AC)$.

For slew rates in between the values listed in Table 52, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

[Table 51] ADD/CMD Setup and Hold Base-Values for 1V/ns

[ps]	gDDR3-800	gDDR3-1066	gDDR3-1333	gDDR3-1600	gDDR3-1866	gDDR3-2133	reference
tIS(base) AC175	200	125	65	45	-	-	$V_{IH/IL}(AC)$
tIS(base) AC150	350	275	190	170	-	-	$V_{IH/IL}(AC)$
tIS(base)-AC135	-	-	-	-	65	60	$V_{IH/IL}(AC)$
tIS(base)-AC125	-	-	-	-	150	135	$V_{IH/IL}(AC)$
tIH(base)-DC100	275	200	140	120	100	95	$V_{IH/IL}(DC)$

NOTE :

- AC/DC referenced for 1V/ns Address/Command slew rate and 2 V/ns differential CK-CK slew rate
- The tIS(base)-AC150 specifications are adjusted from the tIS(base) AC175 specification by adding an additional 125ps for gDDR3-800/1066 or 100ps for gDDR3-1333/1600 of derating to accommodate for the lower alternate threshold of 150mV and another 25ps to account for the earlier reference point [(175mV-150mV)/1 V/ns]
- The tIS(base) AC125 specifications are adjusted from the tIS(base) AC135 specification by adding an additional 75ps for gDDR3-1866 and 65ps for gDDR3-2133 to accommodate for the lower alternate threshold of 125mV and another 10ps to account for the earlier reference point [(135mV-125mV)/1V/ns].

[Table 52] Derating values gDDR3-800/1066/1333/1600 tIS/tIH-AC/DC based AC175 Threshold

$\Delta t_{IS}, \Delta t_{IH}$ Derating [ps] AC/DC based Alternate AC175 Threshold -> $V_{IH}(AC) = V_{REF}(DC) + 175mV$, $V_{IL}(AC) = V_{REF}(DC) - 175mV$																	
		CLK,CLK Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
CMD/ ADD Slew rate V/ns	2.0	88	50	88	50	88	50	96	58	104	66	112	74	120	84	128	100
	1.5	59	34	59	34	59	34	67	42	75	50	83	58	91	68	99	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	-2	-4	-2	-4	-2	-4	6	4	14	12	22	20	30	30	38	46
	0.8	-6	-10	-6	-10	-6	-10	2	-2	10	6	18	14	26	24	34	40
	0.7	-11	-16	-11	-16	-11	-16	-3	-8	5	0	13	8	21	18	29	34
	0.6	-17	-26	-17	-26	-17	-26	-9	-18	-1	-10	7	-2	15	8	23	24
	0.5	-35	-40	-35	-40	-35	-40	-27	-32	-19	-24	-11	-16	-2	-6	5	10
0.4	-62	-60	-62	-60	-62	-60	-54	-52	-46	-44	-38	-36	-30	-26	-22	-10	

[Table 53] Derating values gDDR3-800/1066/1333/1600 tIS/tIH-AC/DC based - Alternate AC150 Threshold

$\Delta tIS, \Delta tIH$ Derating [ps] AC/DC based Alternate AC150 Threshold $\rightarrow V_{IH}(AC) = V_{REF}(DC) + 150mV, V_{IL}(AC) = V_{REF}(DC) - 150mV$																	
		CLK,CLK Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ ADD Slew rate V/ns	2.0	75	50	75	50	75	50	83	58	91	66	99	74	107	84	115	100
	1.5	50	34	50	34	50	34	58	42	66	50	74	58	82	68	90	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	0	-4	0	-4	0	-4	8	4	16	12	24	20	32	30	40	46
	0.8	0	-10	0	-10	0	-10	8	-2	16	6	24	14	32	24	40	40
	0.7	0	-16	0	-16	0	-16	8	-8	16	0	24	8	32	18	40	34
	0.6	-1	-26	-1	-26	-1	-26	7	-18	15	-10	23	-2	31	8	39	24
	0.5	-10	-40	-10	-40	-10	-40	-2	-32	6	-24	14	-16	22	-6	30	10
	0.4	-25	-60	-25	-60	-25	-60	-17	-52	-9	-44	-1	-36	7	-26	15	-10

[Table 54] Derating values gDDR3-1866/2133 tIS/tIH-AC/DC based Alternate AC135 Threshold

$\Delta tIS, \Delta tIH$ Derating [ps] AC/DC based Alternate AC125 Threshold $\rightarrow V_{IH}(AC) = V_{REF}(DC) + 135mV, V_{IL}(AC) = V_{REF}(DC) - 135mV$																	
		CLK,CLK Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ ADD Slew rate V/ns	2.0	68	50	68	50	68	50	76	58	84	66	92	74	100	84	108	100
	1.5	45	34	45	34	45	34	53	42	61	50	69	58	77	68	85	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	2	-4	2	-4	2	-4	10	4	18	12	26	20	34	30	42	46
	0.8	3	-10	3	-10	3	-10	11	-2	19	6	27	14	35	24	43	40
	0.7	6	-16	6	-16	6	-16	14	-8	22	0	30	8	38	18	46	34
	0.6	9	-26	9	-26	9	-26	17	-18	25	-10	33	-2	41	8	49	24
	0.5	5	-40	5	-40	5	-40	13	-32	21	-24	29	-16	37	-6	45	10
	0.4	-3	-60	-3	-60	-3	-60	6	-52	14	-44	22	-36	30	-26	38	-10

[Table 55] Derating values gDDR3-1866/2133 tIS/tIH-AC/DC based - Alternate AC125 Threshold

$\Delta tIS, \Delta tIH$ Derating [ps] AC/DC based Alternate AC125 Threshold $\rightarrow V_{IH}(AC) = V_{REF}(DC) + 125mV, V_{IL}(AC) = V_{REF}(DC) - 125mV$																	
		CLK,CLK Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ ADD Slew rate V/ns	2.0	63	50	63	50	63	50	71	58	79	66	87	74	95	84	103	100
	1.5	42	34	42	34	42	34	50	42	58	50	66	58	74	68	82	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	4	-4	4	-4	4	-4	12	4	20	12	28	20	36	30	44	46
	0.8	6	-10	6	-10	6	-10	14	-2	22	6	30	14	38	24	46	40
	0.7	11	-16	11	-16	11	-16	19	-8	27	0	35	8	43	18	51	34
	0.6	16	-26	16	-26	16	-26	24	-18	32	-10	40	-2	48	8	56	24
	0.5	15	-40	15	-40	15	-40	23	-32	31	-24	39	-16	47	-6	55	10
	0.4	13	-60	13	-60	13	-60	21	-52	29	-44	37	-36	45	-26	53	-10

[Table 56] Required time t_{VAC} above $V_{IH}(AC)$ (blow $V_{IL}(AC)$) for valid ADD/CMD transition

Slew Rate[V/ns]	t_{VAC} @175mV [ps]		t_{VAC} @150mV [ps]		t_{VAC} @135mV [ps]		t_{VAC} @125mV [ps]	
	min	max	min	max	min	max	min	max
>2.0	75	-	175	-	TBD	-	TBD	-
2.0	57	-	170	-	TBD	-	TBD	-
1.5	50	-	167	-	TBD	-	TBD	-
1.0	38	-	163	-	TBD	-	TBD	-
0.9	34	-	162	-	TBD	-	TBD	-
0.8	29	-	161	-	TBD	-	TBD	-
0.7	22	-	159	-	TBD	-	TBD	-
0.6	13	-	155	-	TBD	-	TBD	-
0.5	0	-	150	-	TBD	-	TBD	-
< 0.5	0	-	150	-	TBD	-	TBD	-

NOTE :Clock and Strobe are drawn on a different time scale.

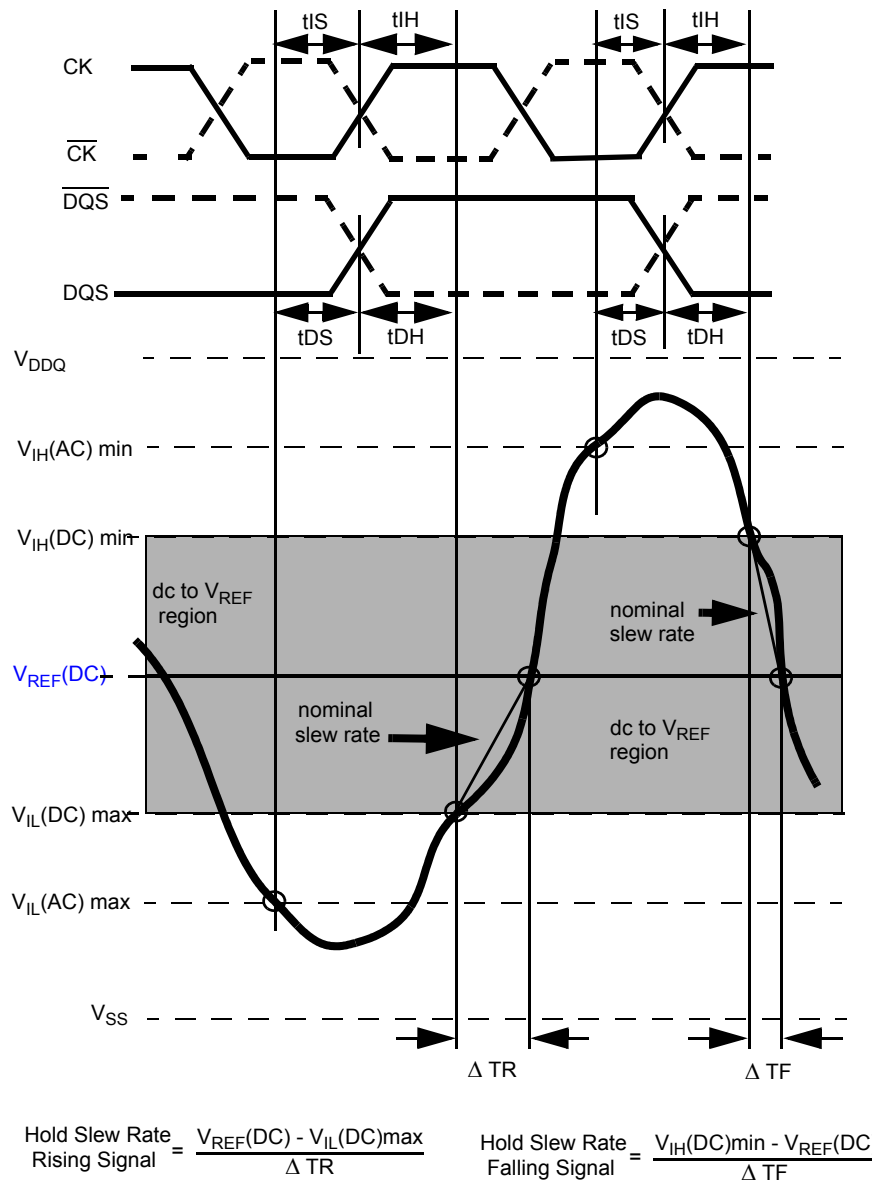


Figure 22. Illustration of nominal slew rate for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock).

NOTE :Clock and Strobe are drawn on a different time scale.

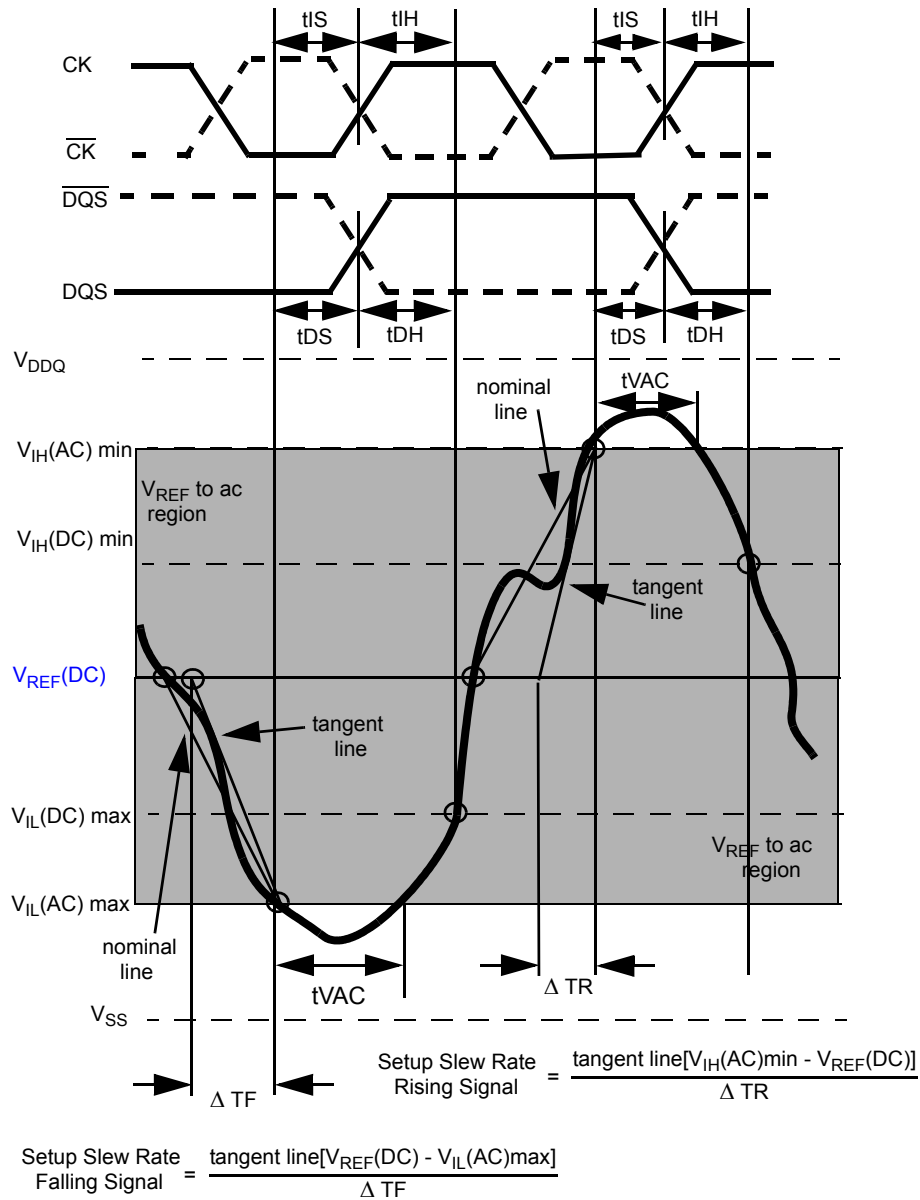


Figure 23. Illustration of tangent line for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

NOTE :Clock and Strobe are drawn on a different time scale.

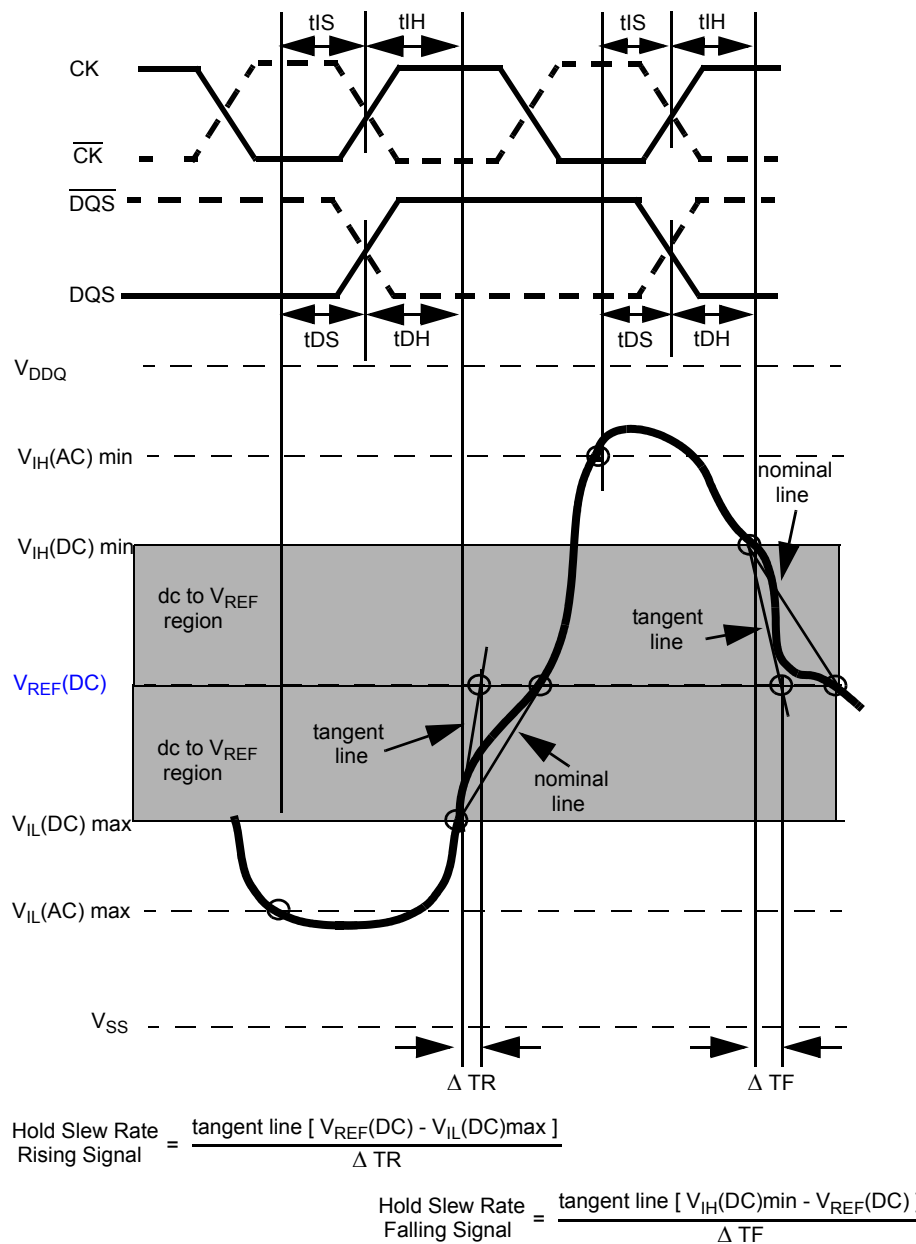


Figure 24. Illustration of tangent line for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock)

15.4 Data Setup, Hold and Slew Rate Derating :

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value (see Table 57) to the ΔtDS and ΔtDH (see Table 55) derating value respectively. Example: tDS (total setup time) = tDS(base) + ΔtDS .

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF}(DC)$ and the first crossing of $V_{IH}(AC)_{min}$.

Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF}(DC)$ and the first crossing of $V_{IL}(AC)_{max}$ (see Figure 25). If the actual signal is always earlier than the nominal slew rate line between shaded ' $V_{REF}(DC)$ to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded ' $V_{REF}(DC)$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 27).

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL}(DC)_{max}$ and the first crossing of $V_{REF}(DC)$.

Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH}(DC)_{min}$ and the first crossing of $V_{REF}(DC)$ (see Figure). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF}(DC)$ region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF}(DC)$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF}(DC)$ level is used for derating value (see Figure 28).

For a valid transition the input signal has to remain above/below $V_{IH/IL}(AC)$ for some time tVAC (see Table 56).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL}(AC)$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL}(AC)$.

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

[Table 57] Data Setup and Hold Base-Values

[ps]	gDDR3-800	gDDR3-1066	gDDR3-1333	gDDR3-1600	gDDR3-1866	gDDR3-2133	reference
tDS(base) AC175	75	25	-	-	-	-	$V_{IH/IL}(AC)$
tDS(base) AC150	125	75	30	10	-	-	$V_{IH/IL}(AC)$
tDS(base) AC135	-	-	-	-	0	-15	$V_{IH/IL}(AC)$
tDH(base) DC100	150	100	65	45	20	5	$V_{IH/IL}(DC)$

NOTE : AC/DC referenced for 1V/ns DQ-slew rate and 2 V/ns DQS slew rate)

[Table 58] Derating values gDDR3-800/1066 tDS/tDH - (AC175)

$\Delta tDS, \Delta tDH$ Derating in [ps] AC/DC based ¹																	
		DQS,DQS Differential Slew Rate															
gDDR3 - 800/ 1066	DQ Slew rate V/ns	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
		2.0	88	50	88	50	88	50	-	-	-	-	-	-	-	-	-
		1.5	59	34	59	34	59	34	67	42	-	-	-	-	-	-	-
		1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-
		0.9	-	-	-2	-4	-2	-4	6	4	14	12	22	20	-	-	-
		0.8	-	-	-	-	-6	-10	2	-2	10	6	18	14	26	24	-
		0.7	-	-	-	-	-	-	-3	-8	5	0	13	8	21	18	29
		0.6	-	-	-	-	-	-	-	-	-1	-10	7	-2	15	8	23
		0.5	-	-	-	-	-	-	-	-	-	-	-11	-16	-2	-6	6
		0.4	-	-	-	-	-	-	-	-	-	-	-	-	-30	-26	-22

NOTE : 1. Cell contents shaded in red are defined as 'not supported'.

[Table 59] Derating values for gDDR3-800/1066/1333/1600 tDS/tDH - (AC150)

$\Delta tDS, \Delta tDH$ Derating in [ps] AC/DC based ¹																	
		DQS,DQS Differential Slew Rate															
DQ Slew rate V/ns		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
		2.0	75	50	75	50	75	50	-	-	-	-	-	-	-	-	-
		1.5	50	34	50	34	50	34	58	42	-	-	-	-	-	-	-
		1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-
		0.9	-	-	0	-4	0	-4	8	4	16	12	24	20	-	-	-
		0.8	-	-	-	-	0	-10	8	-2	16	6	24	14	32	24	-
		0.7	-	-	-	-	-	-	8	-8	16	0	24	8	32	18	40
		0.6	-	-	-	-	-	-	-	-	15	-10	23	-2	31	8	39
		0.5	-	-	-	-	-	-	-	-	-	-	14	-16	22	-6	30
		0.4	-	-	-	-	-	-	-	-	-	-	-	-	7	-26	15

NOTE : 1. Cell contents shaded in red are defined as 'not supported'.

[Table 60] Derating values for gDDR3-1866/2133 tDS/tDH - (AC135)

Δt_{DS} , Δt_{DH} Derating in [ps] AC/DC based ¹																	
DQS, DQS Differential Slew Rate																	
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}
DQ Slew rate V/ns	2.0	68	50	68	50	68	50	-	-	-	-	-	-	-	-	-	-
	1.5	45	34	45	34	45	34	53	42	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	2	-4	2	-4	10	4	18	12	26	20	-	-	-	-
	0.8	-	-	-	-	3	-10	11	-2	19	6	27	14	35	24	-	-
	0.7	-	-	-	-	-	-	14	-8	22	0	30	8	38	18	46	34
	0.6	-	-	-	-	-	-	-	-	25	-10	33	-2	41	8	49	24
	0.5	-	-	-	-	-	-	-	-	-	-	29	-16	37	-6	45	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	30	-26	38	-10

NOTE : 1. Cell contents shaded in red are defined as 'not supported'.

[Table 61] Required time t_{VAC} above $V_{IH}(AC)$ (below $V_{IL}(AC)$) for valid DQ transition

Slew Rate[V/ns]	t_{VAC} [ps] gDDR3-1066 (AC175)		t_{VAC} [ps] gDDR3-1066/1333/1600 (AC150)		t_{VAC} [ps] gDDR3-1866 (AC135)		t_{VAC} [ps] gDDR3-2133 (AC135)	
	min	max	min	max	min	max	min	max
>2.0	75	-	175	-	114	-	89	-
2.0	57	-	170	-	109	-	86	-
1.5	50	-	167	-	66	-	41	-
1.0	38	-	163	-	TBD	-	TBD	-
0.9	34	-	162	-	TBD	-	TBD	-
0.8	29	-	161	-	TBD	-	TBD	-
0.7	22	-	159	-	TBD	-	TBD	-
0.6	13	-	155	-	TBD	-	TBD	-
0.5	0	-	155	-	TBD	-	TBD	-
<0.5	0	-	150	-	TBD	-	TBD	-

NOTE :Clock and Strobe are drawn on a different time scale.

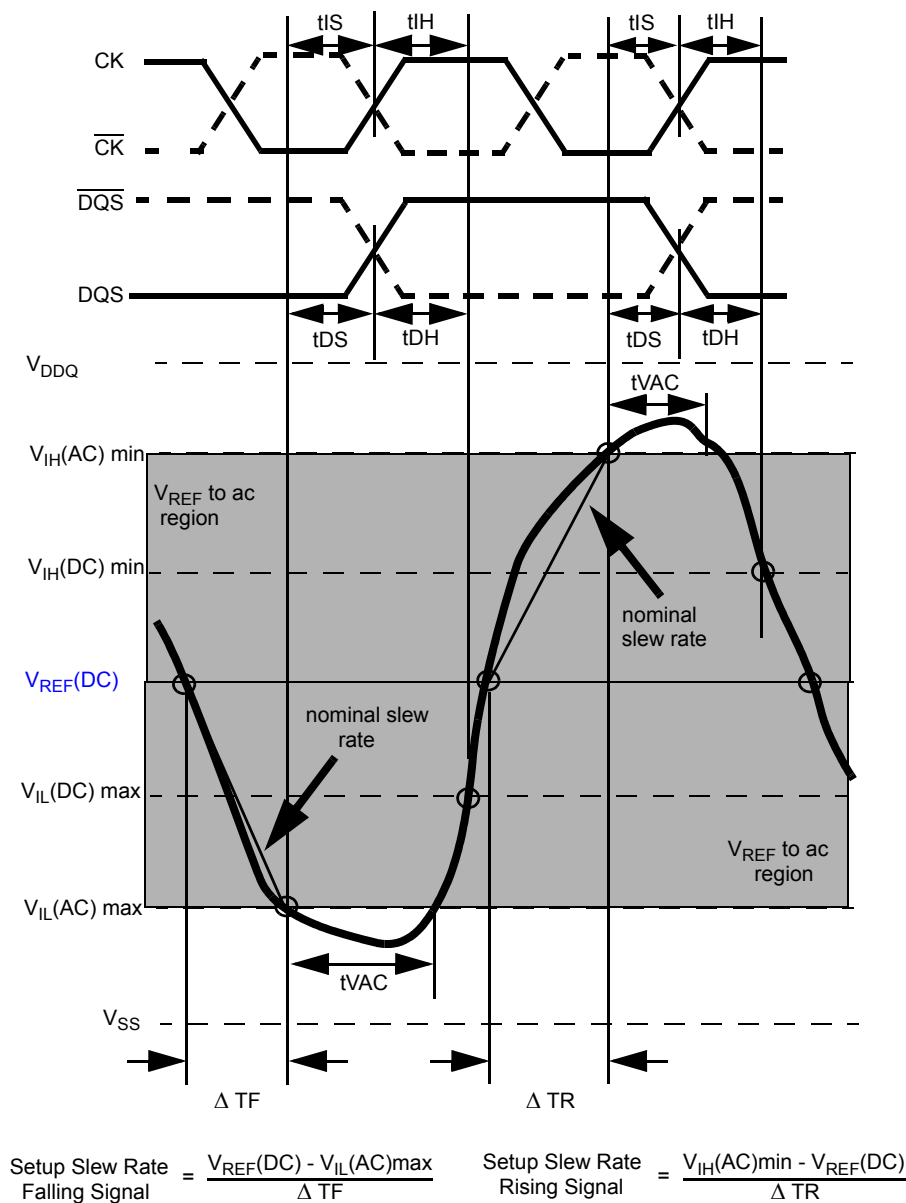


Figure 25. Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock).

NOTE :Clock and Strobe are drawn on a different time scale.

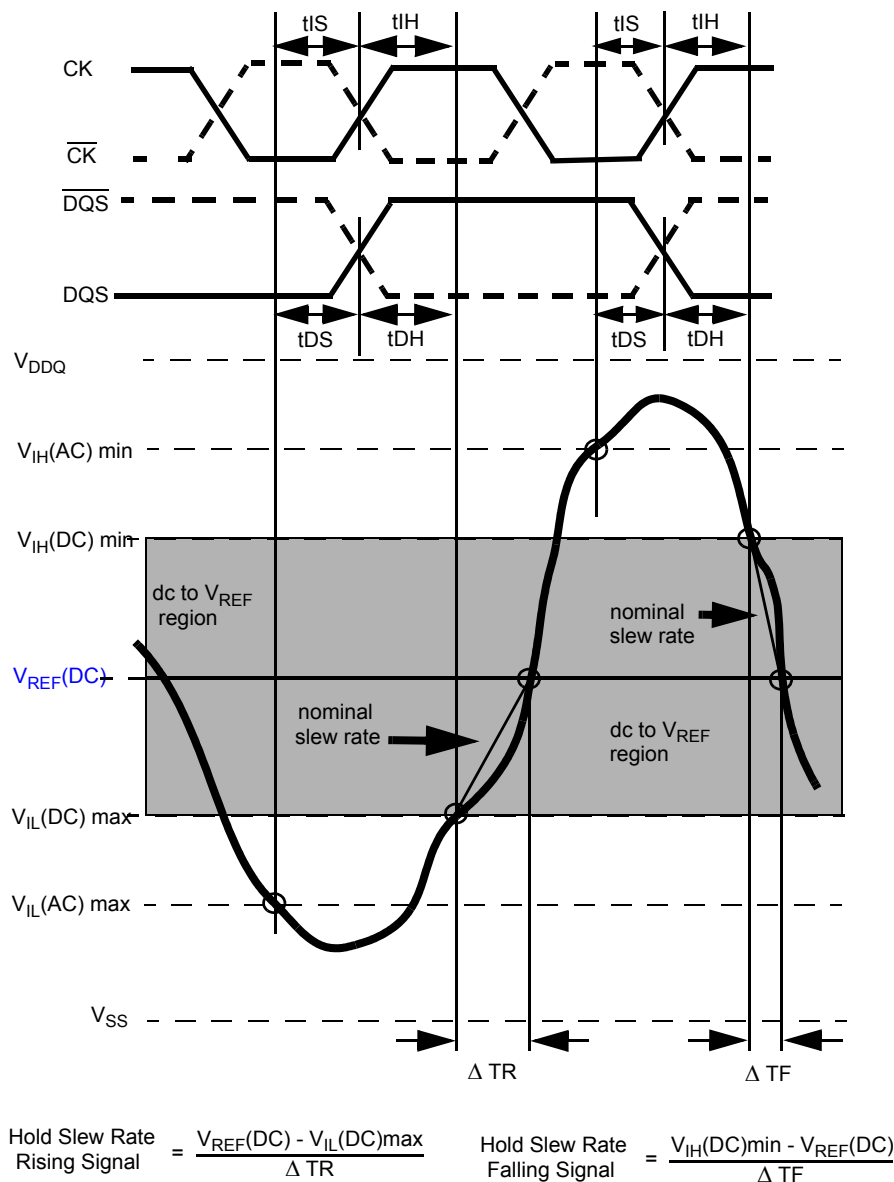


Figure 26. Illustration of nominal slew rate for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock).

NOTE :Clock and Strobe are drawn on a different time scale.

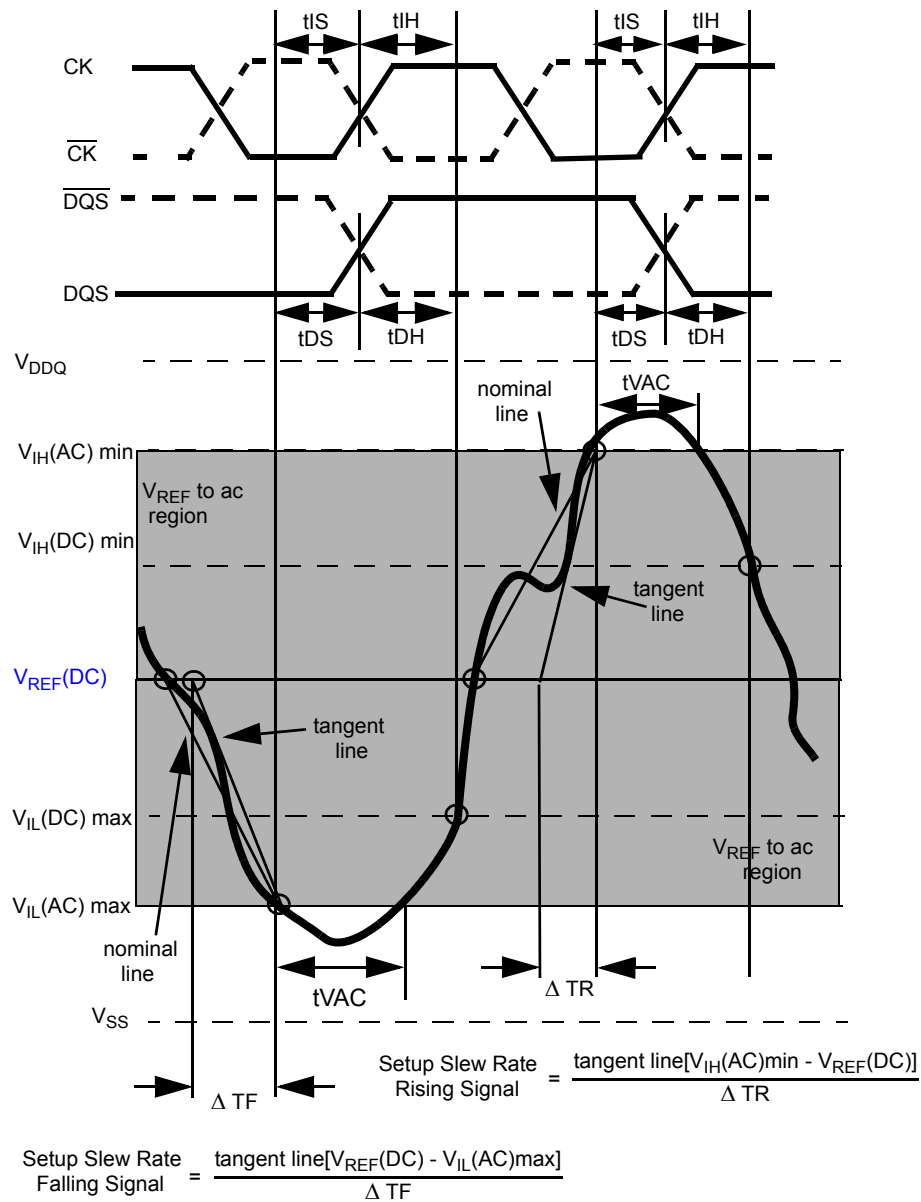


Figure 27. Illustration of tangent line for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

NOTE :Clock and Strobe are drawn on a different time scale.

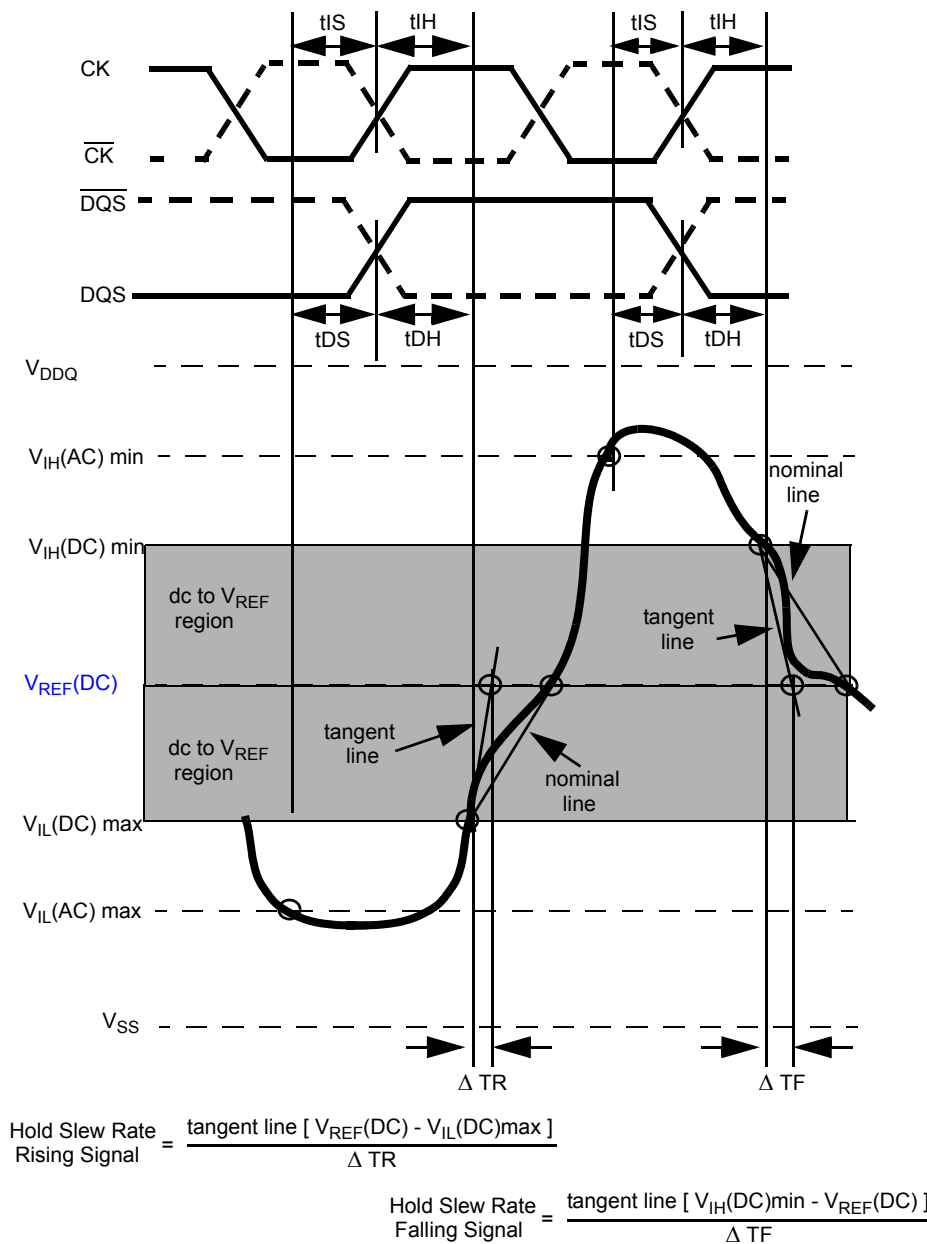


Figure 28. Illustration of tangent line for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock)

16. Functional Description

16.1 Simplified State Diagram

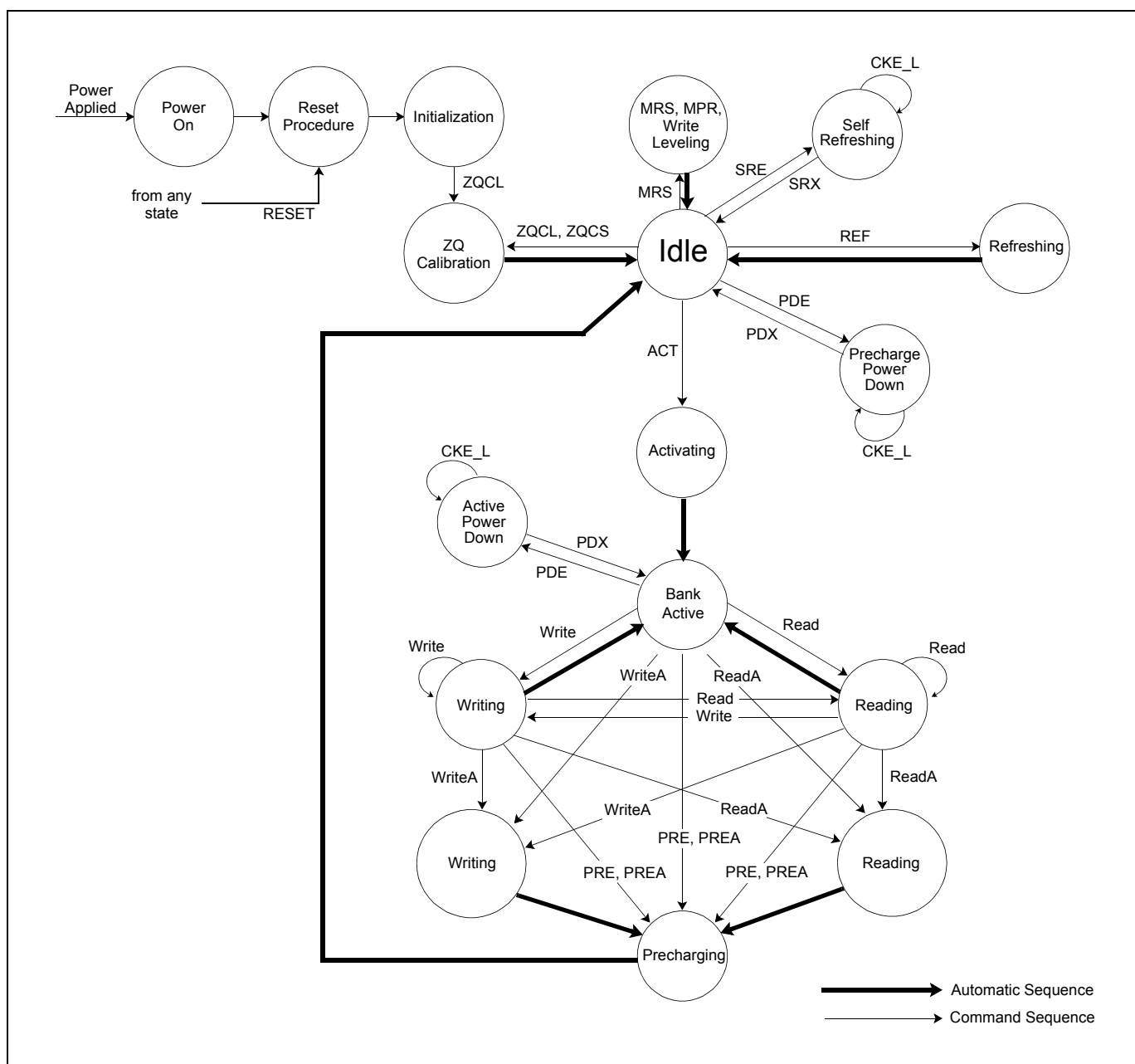


Figure 29. Simplified State Diagram

[Table 62] State Diagram Command Definitions

Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Activate	Read	RD,RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA,RDAS4, RDAS8	PDX	Exit Power-down
PREA	Precharge All	Write	WR, WRS4, WRS8	SRE	Self-Refresh entry
MRS	Mode Register Set	Write A	WRA,WRAS4, WRAS8	SRX	Self-Refresh exit
REF	Refresh	<u>RESET</u>	Start RESET procedure	MPR	Multi Purpose Register
ZQCL	ZQ Calibration Long	ZQCS	ZQ Calibration Short	-	-

NOTE : This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

16.2 Basic Functionality

The gDDR3 SDRAM is a high-speed CMOS, dynamic random-access memory internally configured as a eight-bank DRAM. The gDDR3 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the gDDR3 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the gDDR3 SDRAM are burst oriented, start at a selected location, and continue for a burst length of four or eight in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed (BA0-BA2 select the bank; A0-A15 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10/AP), and the select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register. Prior to normal operation, the gDDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation.

16.3 RESET and Initialization Procedure

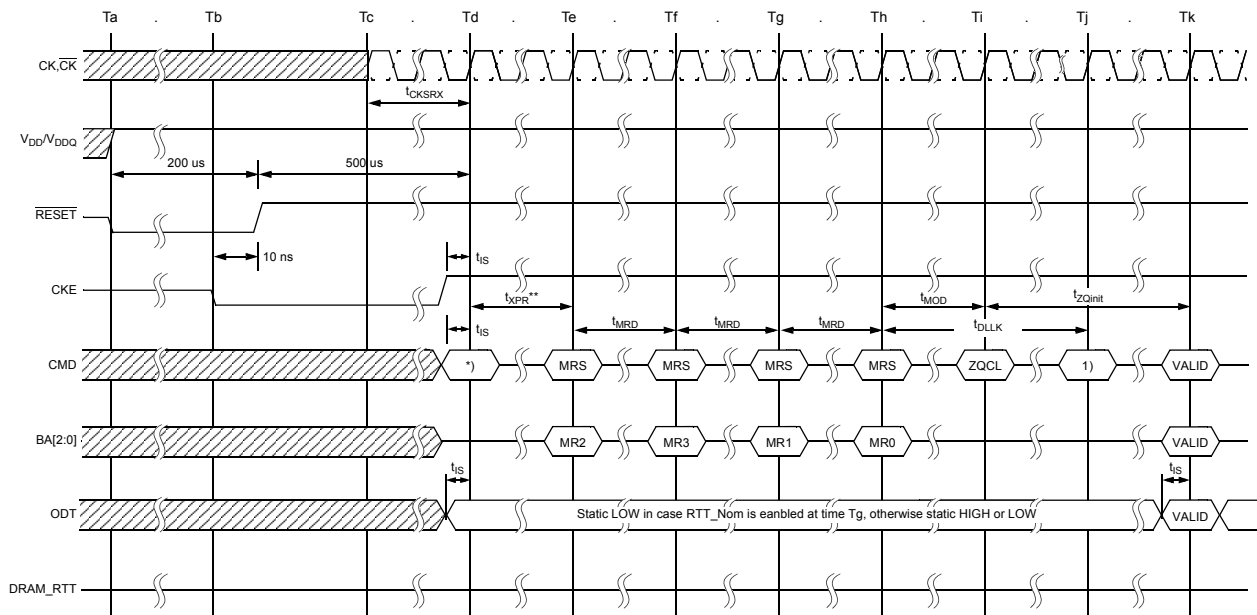
16.3.1 Power-up Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power and attempt to maintain $\overline{\text{RESET}}$ below $0.2 \cdot V_{DD}$ (all other inputs may be undefined). $\overline{\text{RESET}}$ needs to be maintained for minimum 200us with stable power. CKE is pulled "Low" anytime before $\overline{\text{RESET}}$ being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to V_{DD} min must be no longer than 200ms; and during the ramp, $V_{DD} > V_{DDQ}$ and $V_{DD} - V_{DDQ} < 0.3\text{volts}$.
 - V_{DD} and V_{DDQ} are driven from a single power converter output, AND
 - The voltage levels on all pins other than $V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ}$ must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side. In addition, V_{TT} is limited to 0.95V max once power ramp is finished, AND
 - Vref tracks $V_{DDQ}/2$.

or

 - Apply V_{DD} without any slope reversal before or at the same time as V_{DDQ}
 - Apply V_{DDQ} without any slope reversal before or at the same time as V_{TT} & Vref.
 - The voltage levels on all pins other than $V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ}$ must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side.
2. After $\overline{\text{RESET}}$ is de-asserted, wait for another 500us until CKE becomes active. During this time, the DRAM will start internal initialization; this will be done independently of external clocks.
3. Clocks (CK, $\overline{\text{CK}}$) need to be started and stabilized for at least 10ns or 5tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding setup time to clock (tIS) must be met. Also a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of tDLLK and tZQinit.
4. The gDDR3 SDRAM keeps its on-die termination in high-impedance state as long as $\overline{\text{RESET}}$ is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after $\overline{\text{RESET}}$ deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1 and the on-die termination is required to remain in the high impedance state, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.
5. After CKE is registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. (tXPR=Max(tXS, 5tCK))
6. Issue MRS Command to load MR2 with all application settings. (To issue MRS command for MR2, provide "Low" to BA0 and BA2, "High" to BA1.)
7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide "Low" to BA2, "High" to BA0 and BA1.)
8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue "DLL Enable" command, provide "Low" to A0, "Low" to A0, "High" to BA0 and "Low" to BA1-BA2)
9. Issue MRS Command to load MR0 with all application settings and "DLL reset". (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-2).
10. Issue ZQCL command to starting ZQ calibration
11. Wait for both tDLLK and tZQ init completed
12. The gDDR3 SDRAM is now ready for normal operation.

**NOTE :**

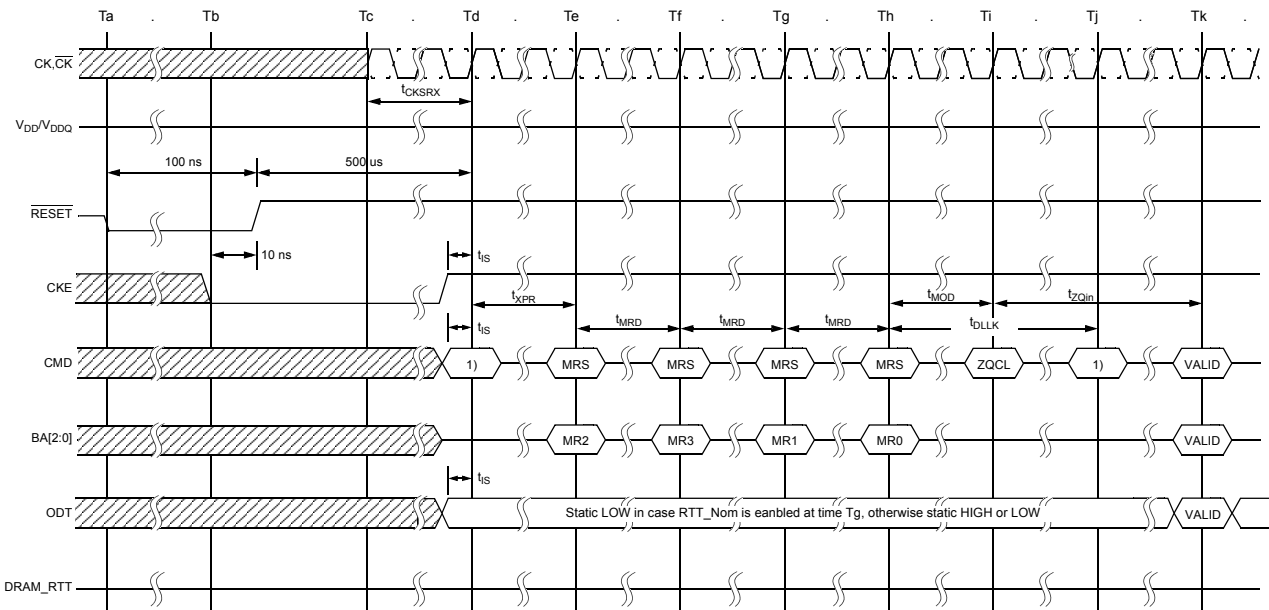
1) From time point 'Td' until 'Tk', NOP or DES commands must be applied between MRS and ZQCL commands

Figure 30. RESET and Initialization Sequence at Power-on Ramping

16.3.2 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Asserted RESET below $0.2 \times V_{DD}$ anytime when reset is needed (all other inputs may be undefined). RESET needs to be maintained for minimum 100 ns. CKE is pulled "LOW" before RESET being de-asserted (min. time 10 ns).
2. Follow Power-up Initialization Sequence step 2 to 11.
3. The Reset sequence is now completed, gDDR3 SDRAM is ready for normal operation.

**NOTE :**

1) From time point 'Td' until 'Tk', NOP or DES commands must be applied between MRS and ZQCL commands

Figure 31. RESET procedure at Power stable condition

16.4 Register Definition

16.4.1 Programming the Mode Registers

For application flexibility, various functions, features, and modes are programmable in four Mode Registers, provided by the gDDR3 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers (MR#) are not defined, contents of Mode Registers must be fully initialized and/or re-initialized, i.e., written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents.

The mode register set command cycle time, t_{MRD} is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown in Figure 32

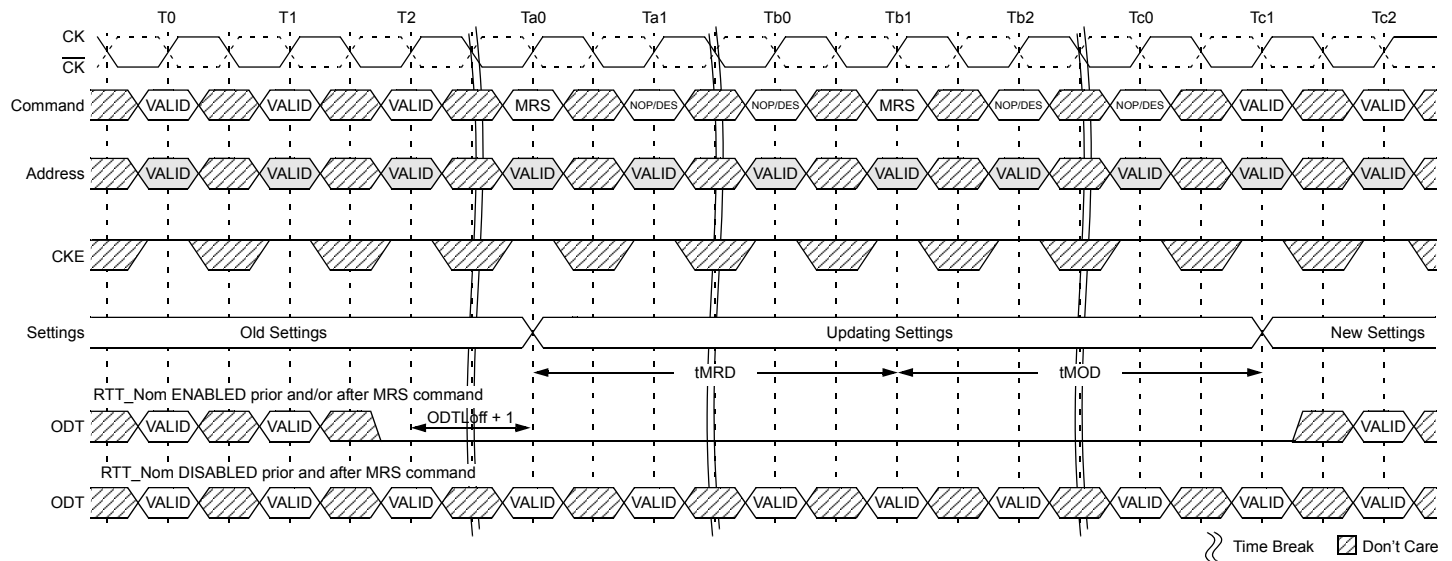


Figure 32. t_{MRD} Timing

The MRS command to Non-MRS command delay, t_{MOD} , is required for the DRAM to update the features, except DLL reset, and is the minimum time required from an MRS command to a non-MRS command excluding NOP and DES shown in Figure 33

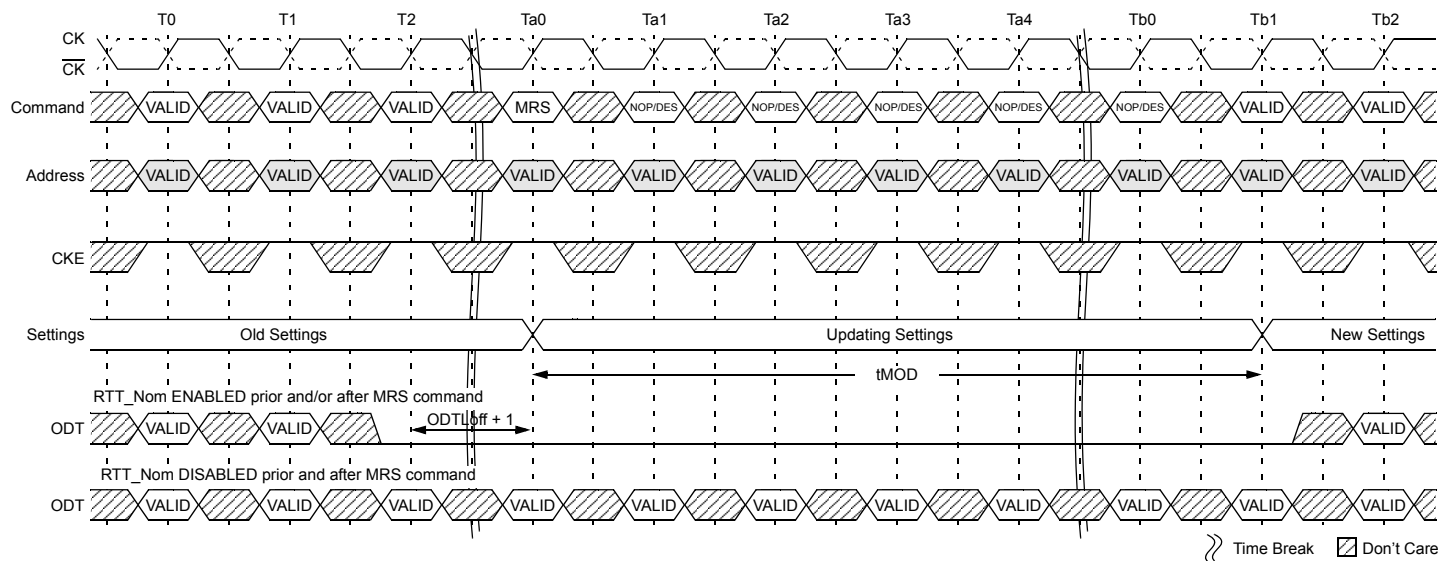


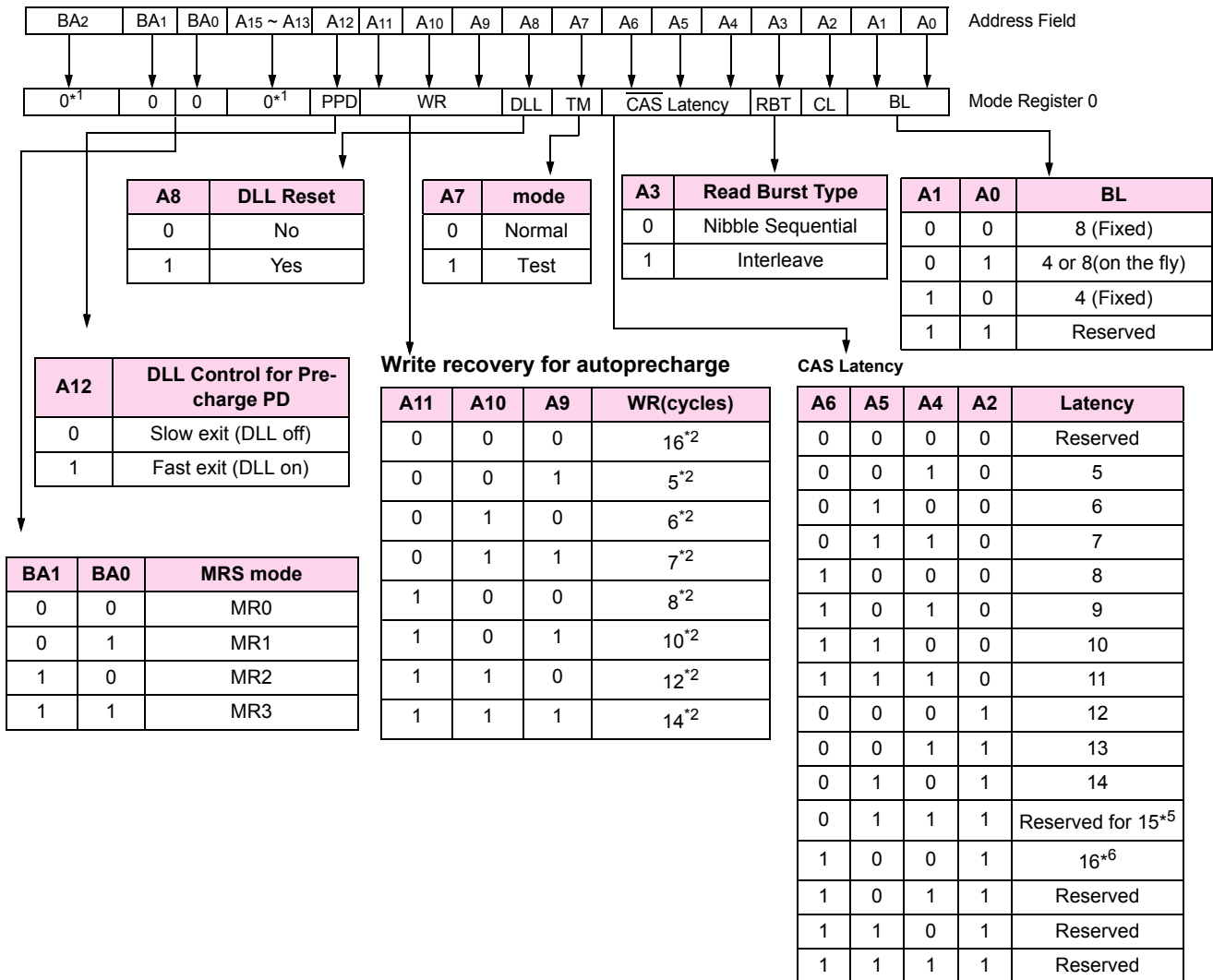
Figure 33. t_{MOD} Timing

15.4.1 Programming the Mode Registers (Cont)

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e., all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. If the RTT_NOM feature is enabled in the Mode Register prior and/or after an MRS Command, the ODT Signal must continuously be registered LOW ensuring RTT is in an off State prior to the MRS command. The ODT Signal may be registered high after tMOD has expired. If the RTT_NOM Feature is disabled in the Mode Register prior and after an MRS command, the ODT Signal can be registered either LOW or HIGH before, during and after the MRS command. The mode registers are divided into various fields depending on the functionality and/or modes.

16.4.2 Mode Register MR0

The mode register MR0 stores the data for controlling various operating modes of gDDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR and DLL control for precharge power down, which include various vendor specific options to make gDDR3 SDRAM useful for various applications. The mode register is written by asserting low on CS, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, BA0, BA1 and BA2, while controlling the states of address pins according to the Figure below.



NOTE :

*1 : BA2 and A13~A15 are RFU and must be programmed to 0 during MRS.

*2 : WR(write recovery for autprecharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer: $WR_{min}[\text{cycles}] = \text{Roundup}(tWR[\text{ns}]/tCK[\text{ns}])$. The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.

*3 : The table only shows the encodings for a given Cas Latency. For actual supported Cas Latency, please refer to speedbin tables for each frequency

*4 : The table only shows the encodings for Write Recovery. For actual Write recovery timing, please refer to AC timingtable

*5 : RFU(Reserved for Future Use)

*6 : CL16 is used for gDDR3 1Gb S-die at 2400Mbps operation.

Figure 34. MR0 Definition

16.4.2.1 Burst Length, Type and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 as shown in Figure 34. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in Table 63. The burst length is defined by bits A0-A1. Burst length options include fixed BC4, fixed BL8, and 'on the fly' which allows BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/BC.

[Table 63] Burst Type and Burst Order

Burst Length	READ/ WRITE	Starting Column ADDRESS (A2,A1,A0)	burst type = Sequential (decimal) A3 = 0	burst type = Interleaved (decimal) A3 = 1	Notes
4 Chop	READ	0 0 0	0,1,2,3,T,T,T,T	0,1,2,3,T,T,T,T	1, 2, 3
		0 0 1	1,2,3,0,T,T,T,T	1,0,3,2,T,T,T,T	1, 2, 3
		0 1 0	2,3,0,1,T,T,T,T	2,3,0,1,T,T,T,T	1, 2, 3
		0 1 1	3,0,1,2,T,T,T,T	3,2,1,0,T,T,T,T	1, 2, 3
		1 0 0	4,5,6,7,T,T,T,T	4,5,6,7,T,T,T,T	1, 2, 3
		1 0 1	5,6,7,4,T,T,T,T	5,4,7,6,T,T,T,T	1, 2, 3
		1 1 0	6,7,4,5,T,T,T,T	6,7,4,5,T,T,T,T	1, 2, 3
		1 1 1	7,4,5,6,T,T,T,T	7,6,5,4,T,T,T,T	1, 2, 3
	WRITE	0,V,V	0,1,2,3,X,X,X,X	0,1,2,3,X,X,X,X	1, 2, 4, 5
		1,V,V	4,5,6,7,X,X,X,X	4,5,6,7,X,X,X,X	1, 2, 4, 5
8	READ	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2
		0 0 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6	2
		0 1 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5	2
		0 1 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4	2
		1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3	2
		1 0 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2	2
		1 1 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1	2
		1 1 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0	2
	WRITE	V,V,V	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2, 4

NOTE :

1. In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/BC, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.
2. 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.
3. T: Output driver for data and strobes are in high impedance.
4. V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.
5. X: Don't Care.

16.4.2.2 CAS Latency

The CAS Latency is defined by MR0(bits A4-A6) as shown in Figure 34. CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. gDDR3 SDRAM does not support any half clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL); $RL = AL + CL$. For more information on the supported CL and AL settings based on the operating clock frequency, refer to "Standard Speed Bins" on each component datasheet. For detailed Read operation refer to "READ Operation" on page 92

16.4.2.3 Test Mode

The normal operating mode is selected by MR0(bit A7 = 0) and all other bits set to the desired values shown in Figure 34. Programming bit A7 to a '1' places the gDDR3 SDRAM into a test mode that is only used by the DRAM Manufacturer and should NOT be used. No operations or functionality is guaranteed if A7 = 1.

16.4.2.4 DLL Reset

The DLL Reset bit is self-clearing, meaning it returns back to the value of '0' after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e. Read commands or ODT synchronous operations).

16.4.2.5 Write Recovery

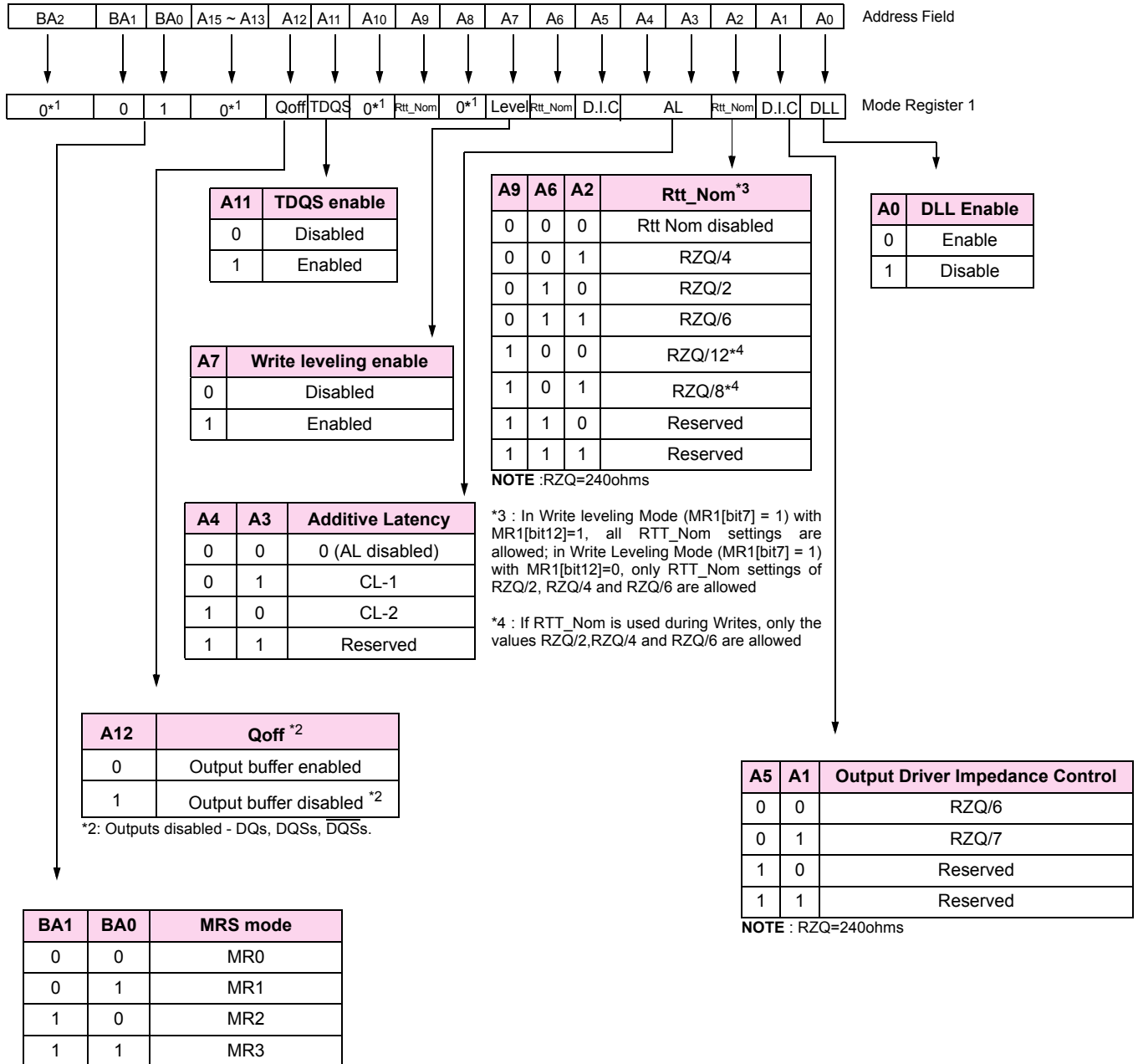
The programmed WR value MR0(bits A9, A10, and A11) is used for the auto precharge feature along with tRP to determine tDAL WR(write recovery for auto-precharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer: $WR_{min}[\text{cycles}] = \text{Roundup}(tWR[\text{ns}]/tCK[\text{ns}])$. The WR must be programmed to be equal or larger than tWR(min).

16.4.2.6 Precharge PD DLL

MR0 (bit A12) is used to select the DLL usage during precharge power-down mode. When MR0(A12 = 0), or "slow-exit", the DLL is frozen after entering precharge power-down (for potential power savings) and upon exit requires tXPDLL to be met prior to the next valid command. When MR0(A12 = 1), or "fast-exit", the DLL is maintained after entering precharge power-down and upon exiting power-down requires tXP to be met prior to the next valid command.

16.4.3 Mode Register MR1

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, Rtt_Nom impedance, additive latency, Write leveling enable, TDQS enable and Qoff. The Mode Register 1 is written by asserting low on CS, RAS, CAS, WE, high on BA0 and low on BA1 and BA2 while controlling the states of address pins according to the Figure below.



* 1 : BA2 and A8, A10 and A13 ~ A15 are RFU and must be programmed to 0 during MRS

Figure 35. MR1 Definition

16.4.3.1 DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1(A0 = 0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled upon exit of Self-Refresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON or tAOF parameters. During tDLLK, CKE must continuously be registered high. gDDR3 SDRAM does not require DLL for any Write operation. For more detailed information on DLL Disable operation refer to "DLL-off Mode" on page 80

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2{A10, A9}={0,0}, to disable Dynamic ODT externally.

16.4.3.2 Output Driver Impedance Control

The output driver impedance of the gDDR3 SDRAM device is selected by MR1(bits A1 and A5) as shown in Figure 35

16.4.3.3 ODT Rtt Values

gDDR3 SDRAM is capable of providing two different termination values (Rtt_Nom and Rtt_WR). The nominal termination value Rtt_Nom is programmed in MR1. A separate value (Rtt_WR) may be programmed in MR2 to enable a unique RTT value when ODT is enabled during writes. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.

16.4.3.4 Additive Latency (AL)

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidths in gDDR3 SDRAM. In this operation, the gDDR3 SDRAM allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings. A summary of the AL register options are shown in Table 64

[Table 64] Additive Latency (AL) Settings

A4	A3	AL
0	0	0 (AL Disabled)
0	1	CL - 1
1	0	CL - 2
1	1	Reserved

NOTE : AL has a value of CL - 1 or CL - 2 as per the CL values programmed in the MR0 register.

16.4.3.5 Write leveling

For better signal integrity, gDDR3 memory module adopted fly by topology for the commands, addresses, control signals and clocks. The fly by topology has benefits from reducing number of stubs and their length but in other aspect, causes flight time skew between clock and strobe at every DRAM on DIMM. It makes it difficult for the Controller to maintain tDQSS, tDSS and tDSH specification. Therefore, the gDDR3 SDRAM supports 'write leveling' feature to allow the controller to compensate for skew. See "Write Leveling" on page 84. for more details.

16.4.3.6 Output Disable

The gDDR3 SDRAM outputs may be enabled/disabled by MR1(bit A12) as shown in Figure 35. When this feature is enabled (A12 = 1), all output pins (DQs, DQS, $\overline{\text{DQS}}$, etc.) are disconnected from the device removing any loading of the output drivers. This feature may be useful when measuring module power for example. For normal operation, A12 should be set to '0'.

16.4.3.7 TDQS, $\overline{\text{TDQS}}$

TDQS (Termination Data Strobe) is a feature of X8 gDDR3 SDRAM that provides additional termination resistance outputs that may be useful in some system configurations.

TDQS is not supported in X4 or X16 configurations. When enabled via the mode register, the same termination resistance function is applied to the $\overline{\text{TDQS}}$ /TDQS pins that is applied to the DQS/ $\overline{\text{DQS}}$ pins.

In contrast to the RDQS function of DDR2 SDRAM, TDQS provides the termination resistance function only. The data strobe function of RDQS is not provided by TDQS.

The TDQS and DM functions share the same pin. When the TDQS function is enabled via the mode register, the DM function is not supported. When the TDQS function is disabled, the DM function is provided and the $\overline{\text{TDQS}}$ pin is not used. Table 65 for details.

The TDQS function is available in X8 gDDR3 SDRAM only and must be disabled via the mode register A11=0 in MR1 for X4 and X16 configurations.

[Table 65] TDQS, $\overline{\text{TDQS}}$ Function Matrix

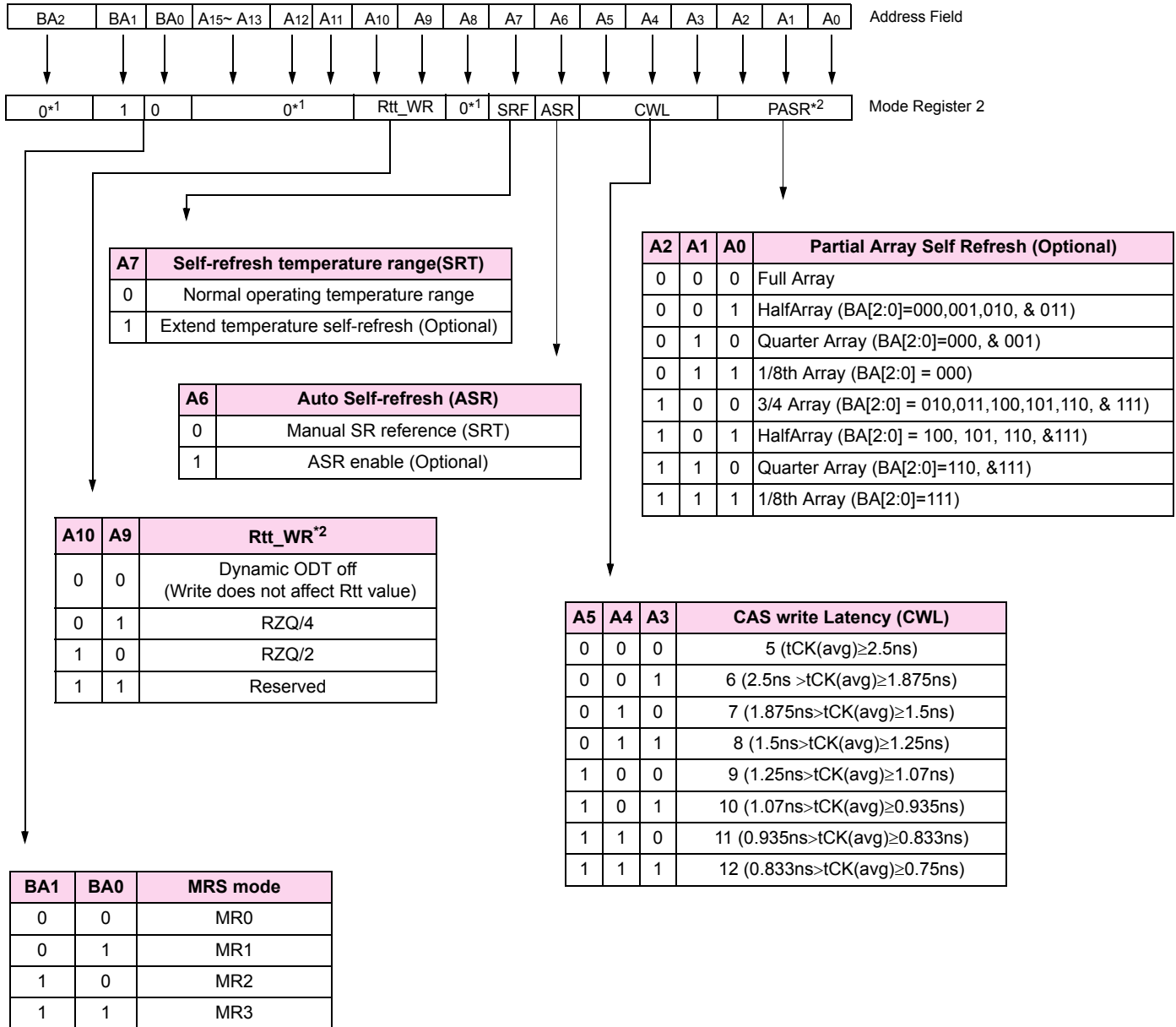
MR1(A11)	DM / TDQS	NU / $\overline{\text{TDQS}}$
0 (TDQS Disabled)	DM	Hi-Z
1 (TDQS Enabled)	TDQS	$\overline{\text{TDQS}}$

NOTE :

1. If TDQS is enabled, the DM function is disabled.
2. When not used, TDQS function can be disabled to save termination power.
3. TDQS function is only available for x8 DRAM and must be disabled for x4 and x16.

16.4.4 Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, Rtt_WR impedance, and CAS write latency. The Mode Register 2 is written by asserting low on $\overline{CS}$, RAS, $\overline{CAS}$, $\overline{WE}$, high on BA1 and low on BA0 and BA2, while controlling the states of address pins according to the table below.



* 1 : BA2, A5, A8, A11 ~ A15 are RFU and must be programmed to 0 during MRS.

* 2 : The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.
During write leveling, Dynamic ODT is not available.

Figure 36. MR2 Definition

16.4.4.1 Partial Array Self-Refresh (PASR)

Optional in gDDR3 SDRAM: Users should refer to the DRAM component data sheet and/or the DIMM SPD to determine if gDDR3 SDRAM devices support the following options or requirements referred to in this material. If PASR (Partial Array Self-Refresh) is enabled, data located in areas of the array beyond the specified address range shown in Figure 36 will be lost if Self-Refresh is entered. Data integrity will be maintained if tREFI conditions are met and no

Self-Refresh command is issued.

16.4.4.2 CAS Write Latency (CWL)

The CAS Write Latency is defined by MR2 (bits A3-A5), as shown in Figure 36. CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. gDDR3 SDRAM does not support any half clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL); WL = AL + CWL. For more information on the supported CWL and AL settings based on the operating clock frequency, refer to "Standard Speed Bins" on each component datasheet. For detailed Write operation refer to "WRITE Operation" on page 103

16.4.4.3 Auto Self-Refresh (ASR) and Self-Refresh Temperature (SRT)

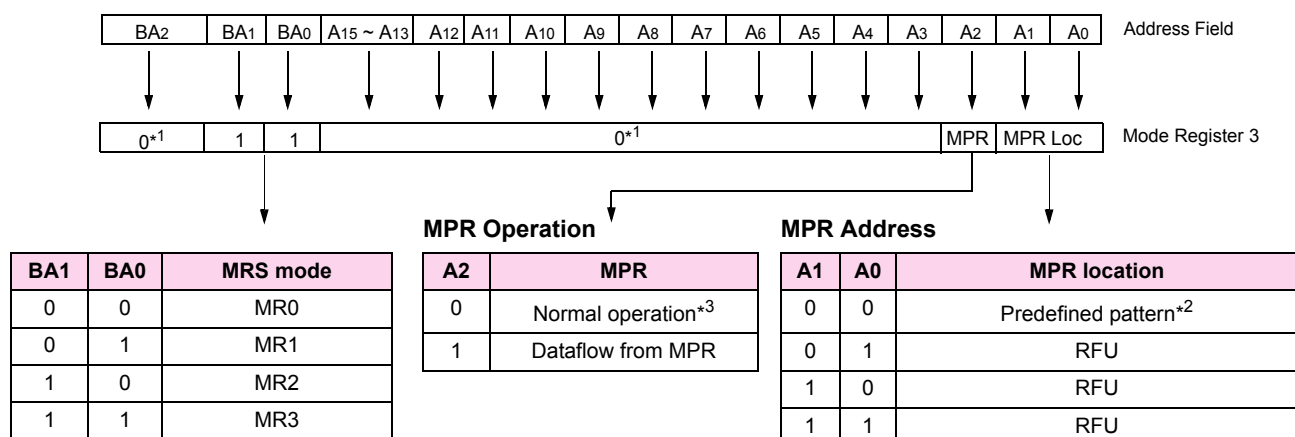
Optional in gDDR3 SDRAM: Users should refer to the DRAM component data sheet and/or the DIMM SPD to determine if gDDR3 SDRAM devices support the following options or requirements referred to in this material. For more details refer to 'Extended Temperature Usage' gDDR3 SDRAM's must support Self-Refresh operation at all supported temperatures. Applications requiring Self-Refresh operation in the Extended Temperature Range must use the optional ASR function or program the SRT bit appropriately.

16.4.4.4 Dynamic ODT (Rtt_WR)

gDDR3 SDRAM introduces a new feature "Dynamic ODT". In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the gDDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT settings. In Write leveling mode, only RTT_Nom is available. For details on ODT operation, refer to "Dynamic ODT" on page 124.

16.4.5 Mode Register MR3

The Mode Register MR3 controls Multi purpose registers. The Mode Register 3 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA1 and BA0, while controlling the states of address pins according to the table below.



* 1 : BA2, A3 - A15 are RFU and must be programmed to 0 during MRS.

* 2 : The predefined pattern will be used for read synchronization.

* 3 : When MPR control is set for normal operation, MR3 A[2]=0, MR3 A[1:0] will be ignored

Figure 37. MR3 Definition

16.4.5.1 Multi-Purpose Register (MPR)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP/tRPA met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Power-Down mode, Self-Refresh, and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode. For detailed MPR operation refer to "Multi Purpose Register" on page 88.

17. gDDR3 SDRAM Command Description and Operation

17.1 Command Truth Table

a) Note 1,2,3 and 4 apply to the entire Command truth table

(b) Note 5 applies to all Read/Write commands.

[BA=Bank Address, RA=Row Address, CA=Column Address, $\overline{BC}$ =Burst Chop, X=Don't care, V=Valid]

[Table 66] Command Truth Table

Function	Abbreviation	CKE		CS	RAS	CAS	WE	BA0 - BA2	A13 - A15	A12 / BC	A10 / AP	A0 - A9,A11	NOTE
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	V	V	V	X	X	X	X	X	7,8,9,12
				L	H	H	H	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BL4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BL4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BL4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BL4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BL4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BL4, on the Fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BL4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BL4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
ZQ calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,12
				H	V	X	X	X	X	X	X	X	
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	

NOTE :

- All gDDR3 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock. The MSB of BA, RA, and CA are device density and configuration dependant
- $\overline{RESET}$ is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
- Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register
- "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level"
- Burst reads or writes cannot be terminated or interrupted and Fixed/on the fly BL will be defined by MRS
- The Power Down Mode does not perform any refresh operations.
- The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
- Self refresh exit is asynchronous.
- V_{REF} (Both V_{REFDQ} and V_{REFCA}) must be maintained during Self Refresh operation. V_{refDQ} supply man be turned OFF in system during Self Refresh operation, provided that V_{refDQ} is valid and stable prior to CKE going back High and that first Write operation may not occur earlier than 512nCK after exit from Self Refresh.
- The No Operation command should be used in cases when the gDDR3 SDRAM is in an idle or a wait state. The purpose of the No Operation command (NOP) is to prevent the gDDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.
- The Deselect command performs the same function as a No Operation command.
- Refer to the CKE Truth Table for more detail with CKE transition

17.2 Clock Enable (CKE) Truth Table

- (a) Note 1~7 apply to the entire Command truth table
 (b) For Power-down entry and exit parameters See 17.17, ?\$paratext>,? on page 113
 (c) CKE low is allowed only if tMRD and tMOD are satisfied

[Table 67] CKE Truth Table

Current State ²	CKE		Command (N) ³ $\overline{\text{RAS}}, \overline{\text{CAS}}, \overline{\text{WE}}, \overline{\text{CS}}$	Action (N) ³	NOTE
	Previous Cycle ¹ (N-1)	Current Cycle ¹ (N)			
Power Down	L	L	X	Maintain Power-Down	14, 15
	L	H	DESELECT or NOP	Power Down Exit	11, 14
Self Refresh	L	L	X	Maintain Self Refresh	15, 16
	L	H	DESELECT or NOP	Self Refresh Exit	8, 12, 16
Bank(s) Active	H	L	DESELECT or NOP	Active Power Down Entry	11, 13, 14
Reading	H	L	DESELECT or NOP	Power Down Entry	11, 13, 14, 17
Writing	H	L	DESELECT or NOP	Power Down Entry	11, 13, 14, 17
Precharging	H	L	DESELECT or NOP	Power Down Entry	11, 13, 14, 17
Refreshing	H	L	DESELECT or NOP	Precharge Power Down Entry	11
All Banks Idle	H	L	DESELECT or NOP	Precharge Power Down Entry	11,13, 14, 18
	H	L	REFRESH	Self Refresh Entry	9, 13, 18
For more details with all signals See Table 66 "Command Truth Table" on page 78					10

NOTE :

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the gDDR3 SDRAM immediately prior to clock edge N
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh
6. CKE must be registered with the same value on tCKEmin consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the tCKEmin clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + tCKEmin + tIH.
7. DESELECT and NOP are defined in the Command truth table
8. On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.
9. Self Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power Down Entry and Exit are NOP and DESELECT only.
12. Valid commands for Self Refresh Exit are NOP and DESELECT only.
13. Self Refresh can not be entered while Read or Write operations. See Figure 17.16 and Figure 17.17 for a detailed list of restrictions.
14. The Power Down does not perform any refresh operations.
15. "X" means "don't care (including floating around V_{REF})" in Self Refresh and Power Down. It also applies to Address pins
16. V_{REF} (Both V_{REFDQ} and V_{REFCA}) must be maintained during Self Refresh operation. VrefDQ supply may be turned OFF in system during Self Refresh operation, provided that VrefDQ is valid and stable prior to CKE going back High and that first Write operation may not occur earlier than 512nCK after exit from Self Refresh.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power Down is entered, otherwise Active Power Down is entered
18. 'Idle state' means that all banks are closed(tRP,tDAL,etc. satisfied) and CKE is high and all timings from previous operations are satisfied (tMRD,tMOD,tRFC,tZQinit,tZQoper,tZQCS,etc)as well as all SRF exit and Power Down exit parameters are satisfied (tXS,tXP,tXPDLL,etc)

17.3 No OPeration (NOP) Command

The No Operation (NOP) command is used to instruct the selected gDDR3 SDRAM to perform a NOP ($\overline{\text{CS}}$ LOW and $\overline{\text{RAS}}, \overline{\text{CAS}}$, and $\overline{\text{WE}}$ HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

17.4 Deselect Command

The DESELECT function ($\overline{\text{CS}}$ HIGH) prevents new commands from being executed by the gDDR3 SDRAM. The gDDR3 SDRAM is effectively deselected. Operations already in progress are not affected.

17.5 DLL-off Mode

gDDR3 DLL-off mode is entered by setting MR1 bit A0 to "1"; this will disable the DLL for subsequent operations until A0 bit set back to "0". The MR1 A0 bit for DLL control can be switched either during initialization or later. Refer to "Input clock frequency change" on page 83.

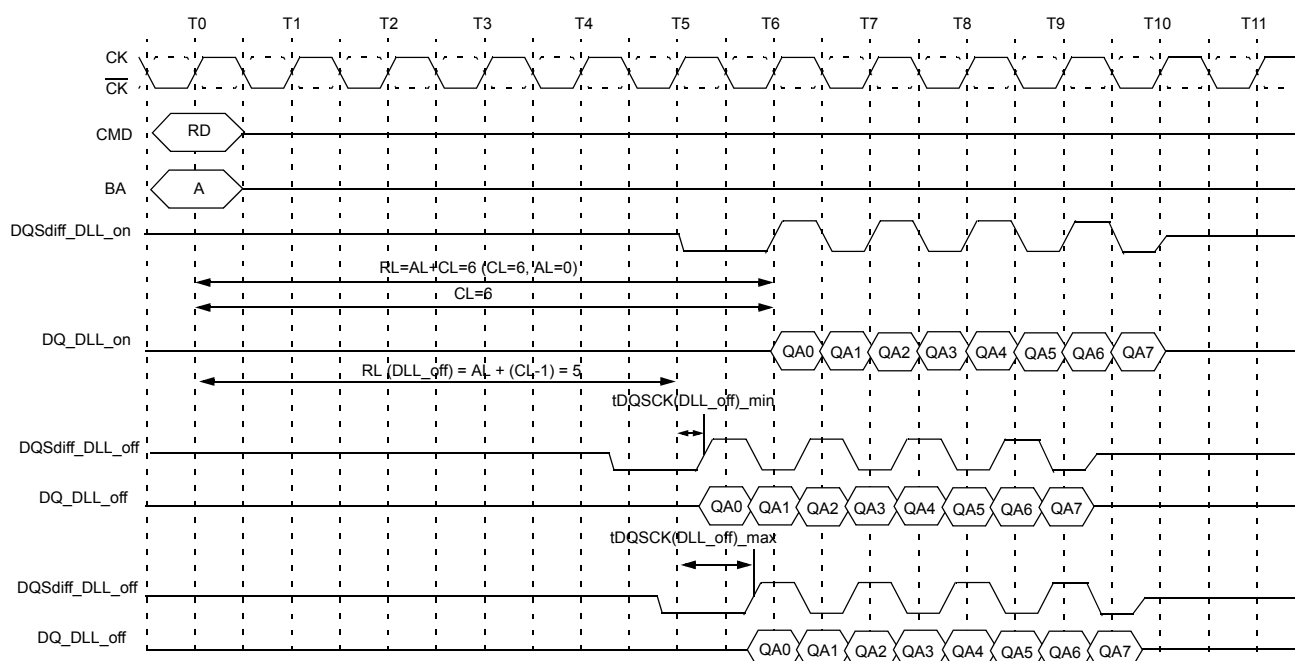
The DLL-off Mode operations listed below are an optional feature for gDDR3. The maximum clock frequency for DLL-off Mode is specified by the parameter tCKDLL-OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, tREFI.

Due to latency counter and timing restrictions, only one value of CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL=6 and CWL=6.

DLL-off mode will affect the Read data Clock to Data Strobe relationship (tDQSCK), but not the Data Strobe to Data relationship (tDQSQ, tQH). Special attention is needed to line up Read data to controller time domain.

Comparing with DLL-on mode, where tDQSCK starts from the rising clock edge (AL+CL) cycles after the Read command, the DLL-off mode tDQSCK starts (AL+CL - 1) cycles after the read command. Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK) and the difference between tDQSCKmin and tDQSCKmax is significantly larger than in DLL-on mode.

The timing relations on DLL-off mode READ operation have shown at following Timing Diagram (CL=6, BL=8):



NOTE : The tDQSCK is used here for DQS, $\overline{\text{DQS}}$ and DQ to have a simplified diagram; the DLL_off shift will affect both timings in the same way and the skew between all DQ and DQS, $\overline{\text{DQS}}$ signals will still be tDQSCK.

Figure 38. DLL-off mode READ Timing Operation

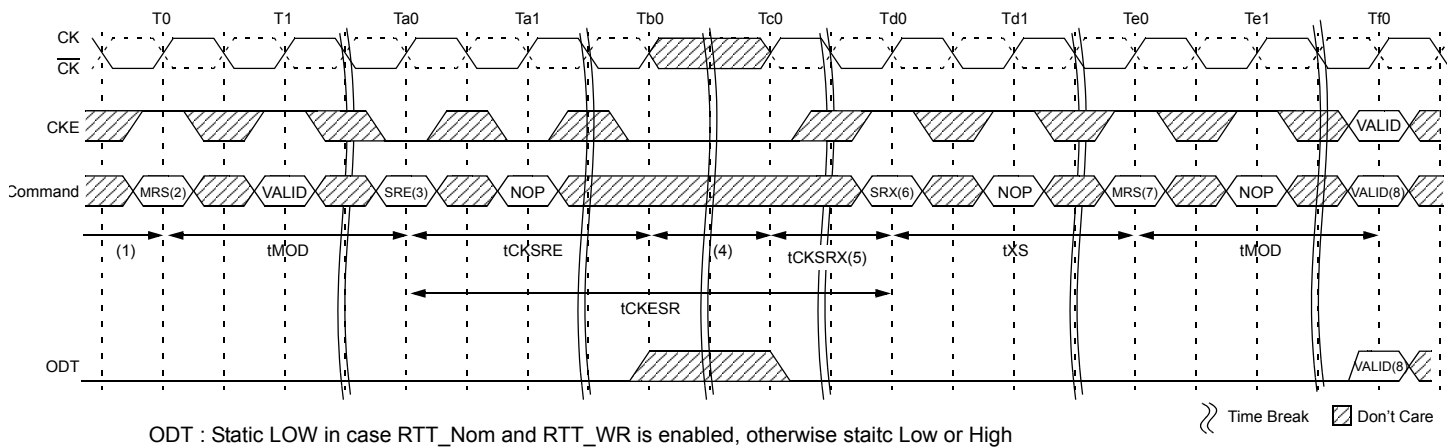
17.6 DLL on/off switching procedure

gDDR3 DLL-off mode is entered by setting MR1 bit A0 to "1"; this will disable the DLL for subsequent operations until A0 bit set back to "0".

17.6.1 DLL "on" to DLL "off" Procedure

To switch from DLL "on" to DLL "off" requires the frequency to be changed during Self-Refresh outlined in the following procedure:

- Starting from Idle state (All banks pre-charged, all timings fulfilled, and DRAMs On-die Termination resistors, RTT, must be in high impedance state before MRS to MR1 to disable the DLL.)
- Set MR1 bit A0 to "1" to disable the DLL.
- Wait tMOD.
- Enter Self Refresh Mode; wait until (tCKSRE) is satisfied.
- Change frequency, in guidance with "Input clock frequency change" on page 83
- Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
- Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until all tMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until all tMOD timings from any MRS command are satisfied. If both ODT features were disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.
- Wait tXS, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. A ZQCL command may also be issued after tXS)
- Wait for tMOD, then DRAM is ready for next command.



NOTE :

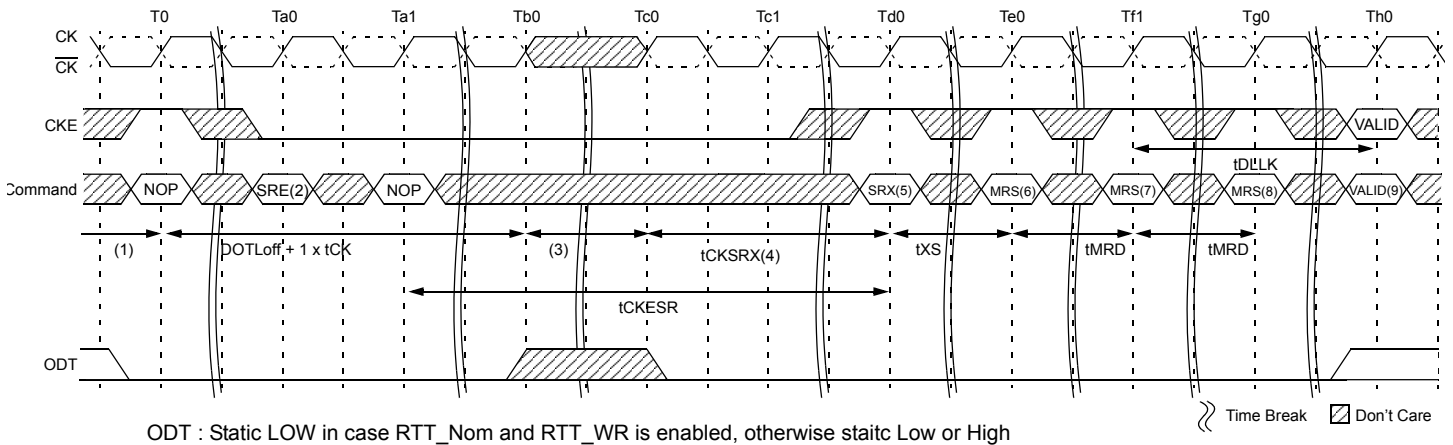
- Starting with Idle State, RTT in Hi-Z state
- Disable DLL by setting MR1 Bit A0 to 1
- Enter SR
- Change Frequency
- Clock must be stable tCKSRX
- Exit SR
- Update Mode registers with DLL off parameters setting
- Any valid command

Figure 39. DLL Switch Sequence from DLL-on to DLL-off

17.6.2 DLL "off" to DLL "on" Procedure

To switch from DLL "off" to DLL "on" (with required frequency change) during Self-Refresh:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled and DRAMs On-die Termination resistors (RTT) must be in high impedance state before Self-Refresh mode is entered.)
2. Enter Self Refresh Mode, wait until t_{CKSRE} satisfied.
3. Change frequency, in guidance with "Input clock frequency change" on page 83
4. Wait until a stable clock is available for at least (t_{CKSRX}) at DRAM inputs.
5. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until t_{DLLK} timing from subsequent DLL Reset command is satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until t_{DLLK} timings from subsequent DLL Reset command is satisfied. If both ODT features are disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.
6. Wait t_{XS} , then set MR1 bit A0 to "0" to enable the DLL.
7. Wait t_{MRD} , then set MR0 bit A8 to "1" to start DLL Reset.
8. Wait t_{MRD} , then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. After t_{MOD} satisfied from any proceeding MRS command, a ZQCL command may also be issued during or after t_{DLLK} .)
9. Wait for t_{MOD} , then DRAM is ready for next command (Remember to wait t_{DLLK} after DLL Reset before applying command requiring a locked DLL!). In addition, wait also for t_{ZQoper} in case a ZQCL command was issued.



NOTE :

1. Starting with Idle State
2. Enter SR
3. Change Frequency
4. Clock must be stable t_{CKSRX}
5. Exit SR
6. Set DLL on by MR1 A0=0
7. Update Mode registers
8. Any valid command

Figure 40. DLL Switch Sequence from DLL-off to DLL-on

17.7 Input clock frequency change

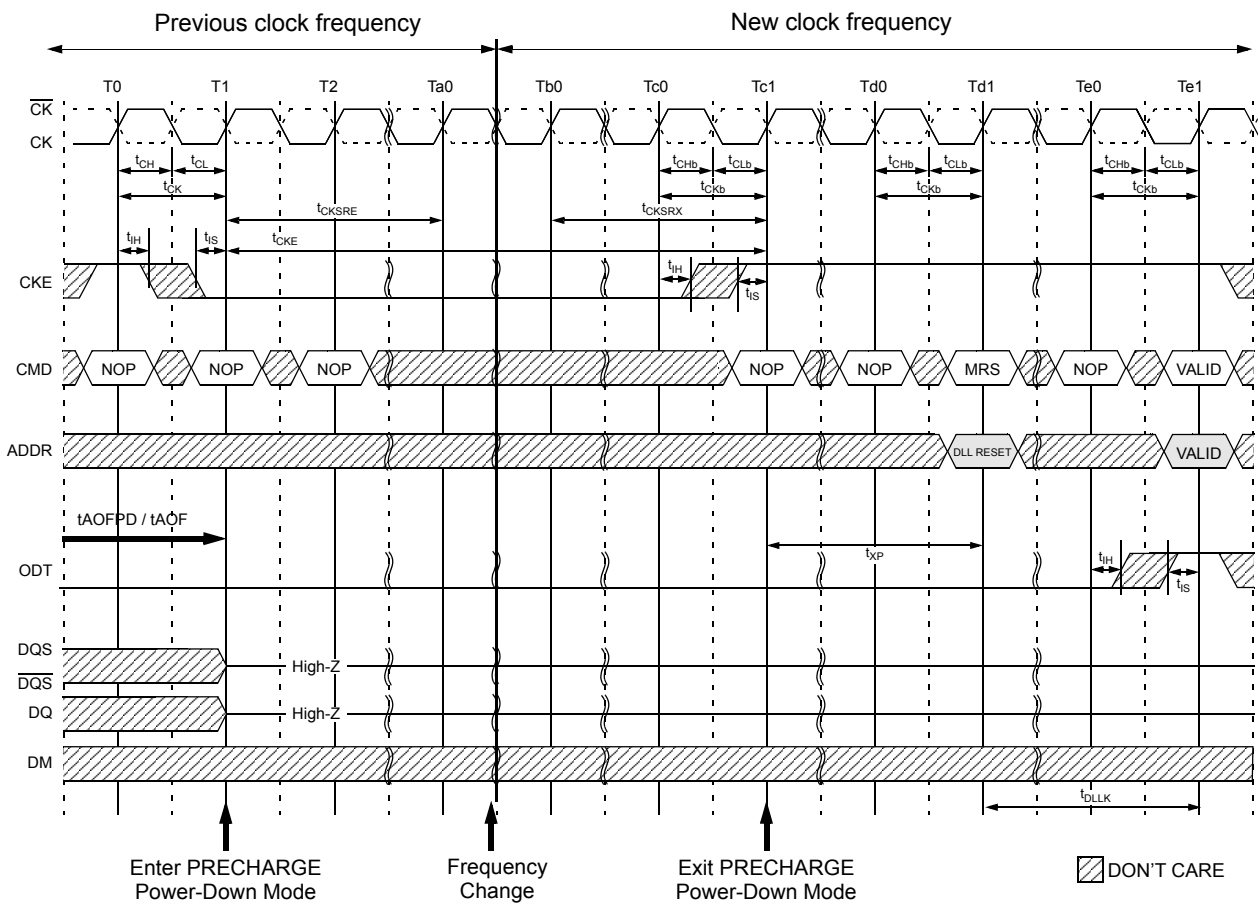
Once the gDDR3 SDRAM is initialized, the gDDR3 SDRAM requires the clock to be "stable" during almost all states of normal operation. This means once the clock frequency has been set and is to be in the "stable state", the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under two conditions:

(1) Self-Refresh mode and (2) Precharge Power-down mode. Outside of these two modes, it is illegal to change the clock frequency.

For the first condition, once the gDDR3 SDRAM has been successfully placed in to Self-Refresh mode and t_{CKSRE} has been satisfied, the state of the clock becomes a don't care. Once a don't care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to t_{CKSRX} . When entering and exiting Self-Refresh mode for the sole purpose of changing the clock frequency, the Self-Refresh entry and exit specifications must still be met as outlined in See Figure 17.16. The gDDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL_on-mode -> DLL_off -mode transition sequence, refer to "DLL on/off switching procedure" on page 81

The second condition is when the gDDR3 SDRAM is in Precharge Power-down mode (either fast exit mode or slow exit mode). If the RTT_NOM feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state. If the RTT_NOM feature was disabled in the mode register prior to entering Precharge power down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case.. A minimum of t_{CKSRE} must occur after CKE goes LOW before the clock frequency may change. The gDDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. During the input clock frequency change, ODT and CKE must be held at stable LOW levels. Once the input clock frequency is changed, stable new clocks must be provided to the DRAM t_{CKSRX} before Precharge Power-down may be exited; after Precharge Power-down is exited and t_{XP} has expired, the DLL must be RESET via MRS. Depending on the new clock frequency additional MRS commands may need to be issued to appropriately set the WR, CL, and CWL with CKE continuously registered high. During DLL re-lock period, ODT must remain LOW and CKE must remain HIGH. After the DLL lock time, the DRAM is ready to operate with new clock frequency. This process is depicted in Figure 41 below.



NOTE :

1. Applicable for both SLOW EXIT and FAST EXIT Precharge Power-down
2. t_{AOFPD} and t_{AOF} must be satisfied and outputs High-Z prior to T1; refer to ODT timing section for exact requirements
3. If the RTT_NOM feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state, as shown in Figure 41. If the RTT_NOM feature was disabled in the mode register prior to entering Precharge power down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case.

Figure 41. Change Frequency during Precharge Power-down

17.8 Write Leveling

For better signal integrity, gDDR3 memory module adopted fly by topology for the commands, addresses, control signals and clocks. The fly by topology has benefits from reducing number of stubs and their length but in other aspect, causes flight time skew between clock and strobe at every DRAM on DIMM. It makes it difficult for the Controller to maintain tDQSS, tDSS and tDSH specification. Therefore, the controller should support 'write leveling' in gDDR3 SDRAM to compensate the skew.

The memory controller can use the 'write leveling' feature and feedback from the gDDR3 SDRAM to adjust the $\overline{DQS} - \overline{DQS}$ to $\overline{CK} - \overline{CK}$ relationship. The memory controller involved in the leveling must have adjustable delay setting on $\overline{DQS} - \overline{DQS}$ to align the rising edge of $\overline{DQS} - \overline{DQS}$ with that of the clock at the DRAM pin. DRAM asynchronously feeds back $\overline{CK} - \overline{CK}$, sampled with the rising edge of $\overline{DQS} - \overline{DQS}$, through the DQ bus. The controller repeatedly delays $\overline{DQS} - \overline{DQS}$ until a transition from 0 to 1 is detected.

The $\overline{DQS} - \overline{DQS}$ delay established through this exercise would ensure tDQSS specification. Besides tDQSS, tDSS and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the $\overline{DQS} - \overline{DQS}$ signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in the chapter "AC Timing Parameters" in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme is shown in Figure 42.

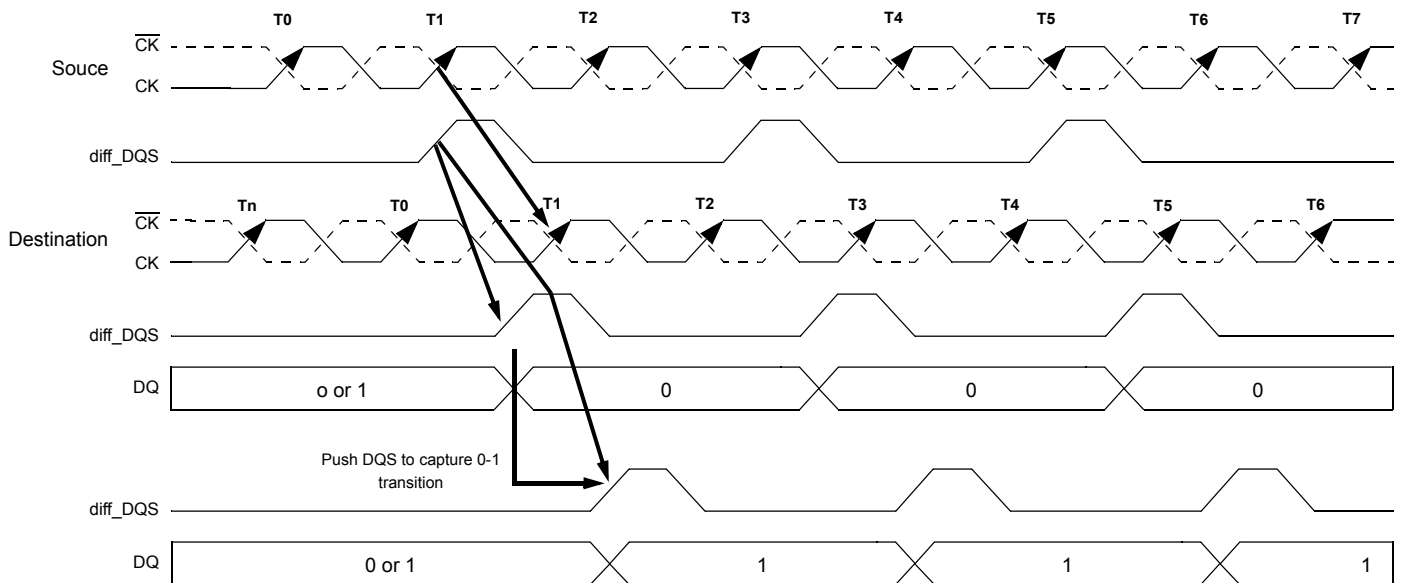


Figure 42. Write leveling concept

$\overline{DQS}/\overline{DQS}$ driven by the controller during leveling mode must be terminated by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

One or more data bits should carry the leveling feedback to the controller across the DRAM configurations X4, X8, and X16. On a X16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper $\overline{diff_DQS}(\overline{diff_UDQS})$ to clock relationship whereas the lower data bits would indicate the lower $\overline{diff_DQS}(\overline{diff_LDQS})$ to clock relationship.

17.8.1 DRAM setting for write leveling & DRAM termination function in that mode

DRAM enters into Write leveling mode if A7 in MR1 set "High" and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set "Low" (Table 68). Note that in write leveling mode, only $\overline{DQS}/\overline{DQS}$ terminations are activated and deactivated via ODT pin not like normal operation (Table 69).

[Table 68] MR setting involved in the leveling procedure

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Qoff)	A12	0	1

[Table 69] DRAM termination function in the leveling mode

ODT pin @DRAM	$\overline{DQS}/\overline{DQS}$ termination	DQs termination
De-asserted	Off	Off
Asserted	On	Off

NOTE : In Write Leveling Mode with its output buffer disabled (MR1[bit7] = 1 with MR1[bit12] = 1) all RTT_Nom settings are allowed; in Write Leveling Mode with its output buffer enabled (MR1[bit7] = 1 with MR1[bit12] = 0) only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

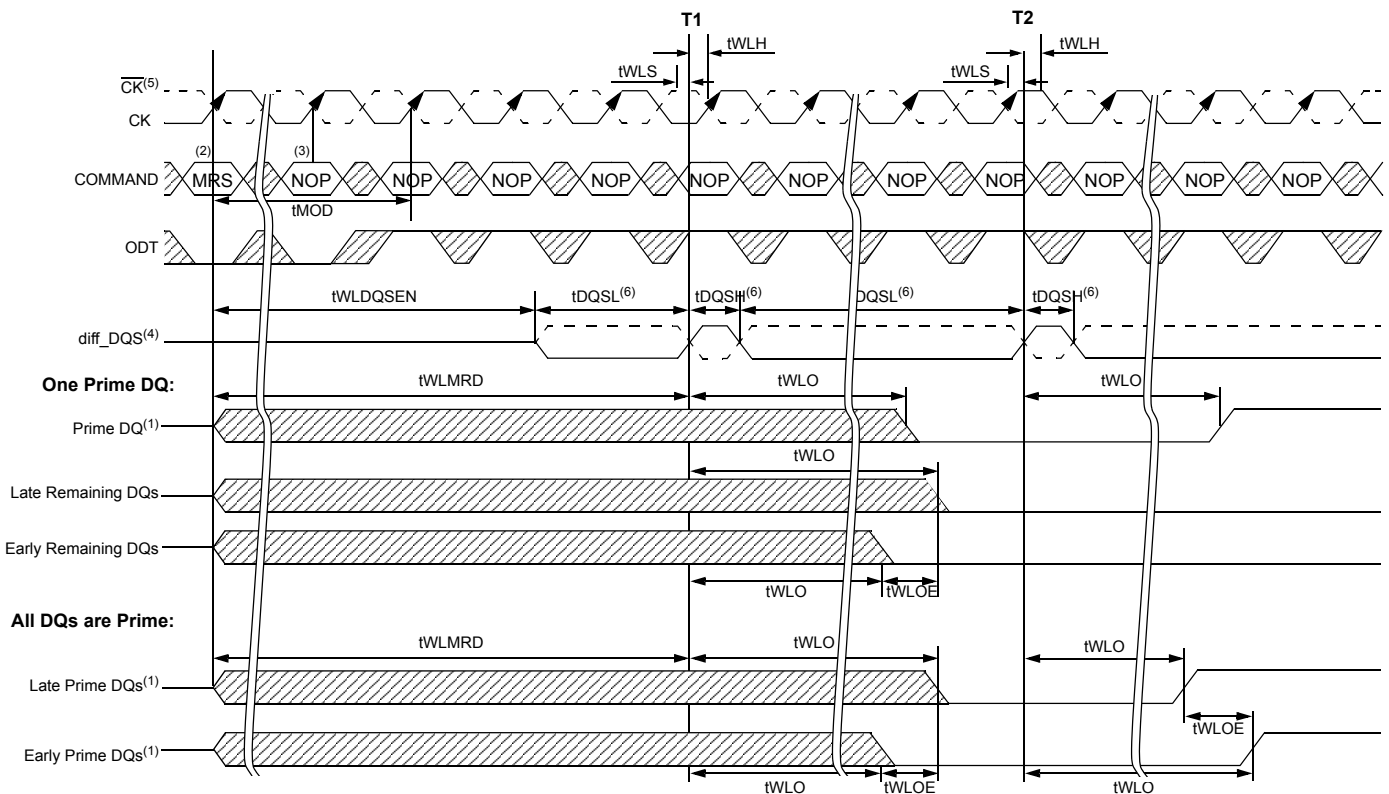
17.8.2 Procedure Description

The Memory controller initiates Leveling mode of all DRAMs by setting bit 7 of MR1 to 1. With entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only NOP or DESELECT commands are allowed, as well as an MRS command to change Qoff bit (MR1[A12]) and an MRS command to exit (MR1[A7]). Upon exiting write leveling mode, the MRS command performing the exit (MR1[A7]=0) may also change MR1 bits of A12-A11, A9, A6-A5 and A2-A1. Since the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1. The controller may assert ODT after tMOD, at which time the DRAM is ready to accept the ODT signal.

The Controller may drive DQS low and $\overline{\text{DQS}}$ high after a delay of tWLDQSEN, at which time DRAM has applied on-die termination on these signals. After tDQSL and tWLMRD, controller provides a single DQS, $\overline{\text{DQS}}$ edge which is used by the DRAM to sample CK driven from controller. tWLMRD(max) timing is controller dependent.

DRAM samples CK status with rising edge of DQS and provides feedback on all the DQ bits asynchronously after tWLO timing. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits; there are no read strobes (DQS/ $\overline{\text{DQS}}$) needed for these DQs. Controller samples incoming DQ and decides to increment or decrement DQS delay setting and launches the next DQS/ $\overline{\text{DQS}}$ pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS delay setting and write leveling is achieved for the device.

Figure 43 describes the timing diagram and parameters for the overall Write Leveling procedure.



NOTE *:

1. DRAM has the option to drive leveling feedback on a prime DQ or all DQs. If feedback is driven only on one DQ, the remaining DQs must be driven low, as shown in above Figure, and maintained at this state through out the leveling procedure.
2. MRS : Load MR1 to enter write leveling mode
3. NOP : NOP or deselect
4. diff_DQS is the differential data strobe (DQS- $\overline{\text{DQS}}$). Timing reference points are the zero crossings. DQS is shown with solid line, $\overline{\text{DQS}}$ is shown with dotted line
5. CK/ $\overline{\text{CK}}$: CK is shown with solid dark line, where as $\overline{\text{CK}}$ is drawn with dotted line.
6. DQS, $\overline{\text{DQS}}$ needs to fulfill minimum pulse width requirements tDQSH(min) and tDQSL(min) as defined for regular Writes; the max pulse width is system dependent

Figure 43. Timing details of Write leveling sequence [DQS- $\overline{\text{DQS}}$ is capturing CK- $\overline{\text{CK}}$ low at T1 and CK- $\overline{\text{CK}}$ high at T2]

17.8.3 Write Leveling Mode Exit

The following sequence describes how the Write Leveling Mode should be exited:

1. After the last rising strobe (see ~T111) edge, stop driving the strobe signals (see ~T128). Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until t_{MOD} after the respective MR command (see T145).
2. Drive ODT pin low (t_{IS} must be satisfied) and keep it low. (see T128).
3. After the RTT is switched off, disable Write Level Mode via MR command (see T132).
4. After t_{MOD} is satisfied (T145), a any valid command may be registered. (MR commands may already be issued after t_{MRD} (see T136).

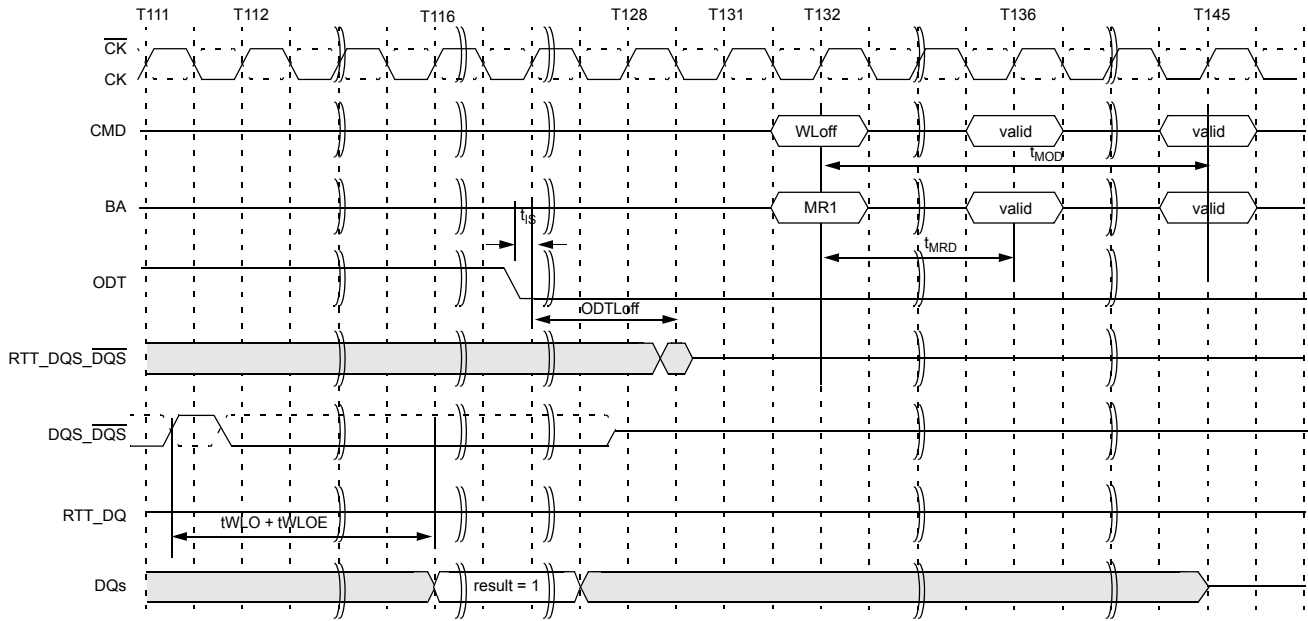


Figure 44. Timing details of Write leveling exit

17.9 Extended Temperature Usage

The following sequence describes how Write Leveling Mode should be exited:

1. After the last rising strobe (see ~T111) edge, stop driving the strobe signals (see ~T128). Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until tMOD after the respective MR command (T145).
2. Drive ODT pin low (tIS must be satisfied) and keep it low. (see T128).
3. After the RTT is switched off, disable Write Level Mode via MR command (see T132).
4. After tMOD is satisfied (T145), a any valid command may be registered. (MR commands may already be issued after tMRD (T136).

[Table 70] Mode Register Description

Field	Bits	Description
ASR	MR2(A6)	Auto Self-Refresh (ASR) (Optional) When enabled, gDDR3 SDRAM automatically provides Self-Refresh power management functions for all supported operating temperature values. If not enabled, the SRT bit must be programmed to indicate T _{OPER} during subsequent Self-Refresh operation. 0 = Manual SR Reference (SRT) 1 = ASR enable (optional)
SRT	MR2(A7)	Self-Refresh Temperature (SRT) Range If ASR = 0, the SRT bit must be programmed to indicate T _{OPER} during subsequent Self-Refresh operation If ASR = 1, SRT bit must be set to 0b 0 = Normal operating temperature range 1 = Extended (optional) operating temperature range

17.9.1 Auto Self-Refresh mode - ASR Mode (optional)

gDDR3 SDRAM provides an Auto Self-Refresh mode (ASR) for application ease. ASR mode is enabled by setting MR2 bit A6=1b and RR2 bit A7=0b. The DRAM will also manage Self-Refresh entry in either the Normal or Extended (optional) Temperature Ranges. In this mode, the DRAM will also manage Self-Refresh power consumption when the DRAM operating temperature changes, lower at low temperatures and higher at high temperatures.

If the ASR option is not supported by the DRAM, MR2 bit A6 must be set to 0b.

If the ASR mode is not enabled (MR2 bit. A6=0b), the SRT bit(MR2 A7) must be manually programmed with the operating temperature range required during Self-Refresh operation.

Support of the ASR option does not automatically imply support of the Extended Temperature Range and Auto Self-Refresh option availability.

17.9.2 Self-Refresh Temperature Range - SRT

SRT applies to devices supporting Extended Temperature Range only. If ASR = '0', the Self-Refresh Temperature (SRT) Range bit must be programmed to guarantee proper self-refresh operation. If SRT = '0', then the DRAM will set an appropriate refresh rate for Self-Refresh operation in the Normal Temperature Range. If SRT = '1' then the DRAM will set an appropriate, potentially different, refresh rate to allow Self-Refresh operation in either the Normal or Extended Temperature Ranges. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.

For parts that do not support the Extended Temperature Range, MR2 bit A7 must be set to '0' and the DRAM should not be operated outside the Normal Temperature Range.

Please refer to the component data sheet and/or the DIMM SPD for Extended Temperature Range availability.

[Table 71] Self-Refresh mode summary

MR2 A[6]	MR2 A[7]	Self-Refresh operation	Allowed Operating Temperature Range for Self-Refresh Mode
0	0	Self-refresh rate appropriate for the Normal Temperature Range	Normal (0 - 85 °C)
0	1	Self-refresh rate appropriate for either the Normal or Extended Temperature Ranges. The DRAM must support Extended Temperature Range. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.	Normal and Extended (0 - 95 °C)
1	0	ASR enabled (not supported). Self-Refresh power consumption is temperature dependent	Normal (0 - 85 °C)
1	0	ASR enabled (not supported). Self-Refresh power consumption is temperature dependent	Normal and Extended (0 - 95 °C)
1	1	Illegal	

17.10 Multi Purpose Register

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. The basic concept of the MPR is shown in Figure 45.

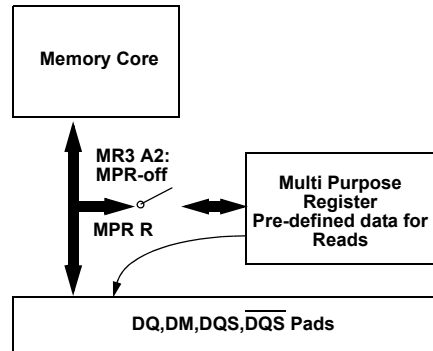


Figure 45. MPR Block Diagram

To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1, as shown in Table 72. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP/tRPA met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. The resulting operation when a RD or RDA command is issued is defined by MR3 bits A[1:0] when the MPR is enabled as shown in Table 73. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Power-Down mode, Self-Refresh, and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

[Table 72] MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function
MPR	MPR-Loc	
0b	don't care (0b or 1b)	Normal operation, no MPR transaction. All subsequent Reads will come from DRAM array. All subsequent Write will go to DRAM array.
1b	see Table 75 on page 120	Enable MPR mode, subsequent RD/RDA commands defined by MR3 A[1:0].

17.10.1 MPR Functional Description

- One bit wide logical interface via all DQ pins during READ operation.
- Register Read on x4:
 - DQ[0] drives information from MPR.
 - DQ[3:0] either drive the same information as DQ[0], or they drive 0b.
- Register Read on x8:
 - DQ[0] drives information from MPR.
 - DQ[7:1] either drive the same information as DQ[0], or they drive 0b.
- Register Read on x16:
 - DQL[0] and DQU[0] drive information from MPR.
 - DQL[7:1] and DQU[7:1] either drive the same information as DQL[0], or they drive 0b.
- Addressing during for Multi Purpose Register reads for all MPR agents:
 - BA[2:0]: don't care
 - A[1:0]: A[1:0] must be equal to '00'. Data read burst order in nibble is fixed
 - A[2]: For BL=8, A[2] must be equal to 0b, burst order is fixed to [0,1,2,3,4,5,6,7], *) For Burst Chop 4 cases, the burst order is switched on nibble base A[2]=0b, Burst order: 0,1,2,3 *) A[2]=1b, Burst order : 4,5,6,7 *)
 - A[9:3]: don't care
 - A10/AP: don't care
 - A12/BC: Selects burst chop mode on-the-fly, if enabled within MR0.
 - A11, A13,... (if available): don't care
- Regular interface functionality during register reads:
 - Support two Burst Ordering which are switched with A2 and A[1:0]=00.
 - Support of read burst chop (MRS and on-the-fly via A12/BC)
 - All other address bits (remaining column address bits including A10, all bank address bits) will be ignored by the gDDR3 SDRAM.
 - Regular read latencies and AC timings apply.
 - DLL must be locked prior to MPR Reads.

NOTE* : Burst order bit 0 is assigned to LSB and burst order bit 7 is assigned to MSB of the selected MPR agent.

17.10.2 MPR Register Address Definition

Table 73 provides an overview of the available data locations, how they are addressed by MR3 A[1:0] during a MRS to MR3, and how their individual bits are mapped into the burst order bits during a Multi Purpose Register Read.

[Table 73] MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function	Burst Length	Read Address A[2:0]	Burst Order and Data Pattern
1b	00b	Read Predefined Pattern for System Calibration	BL8	000b	Burst order 0,1,2,3,4,5,6,7 Pre-defined Data Pattern [0,1,0,1,0,1,0,1]
			BC4	000b	Burst order 0,1,2,3 Pre-defined Data Pattern [0,1,0,1]
			BC4	100b	Burst order 4,5,6,7 Pre-defined Data Pattern [0,1,0,1]
1b	01b	RFU	BL8	000b	BL8 000b Burst order 0,1,2,3,4,5,6,7
			BC4	000b	BC4 000b Burst order 0,1,2,3
			BC4	100b	BC4 100b Burst order 4,5,6,7
1b	10b	RFU	BL8	000b	BL8 000b Burst order 0,1,2,3,4,5,6,7
			BC4	000b	BC4 000b Burst order 0,1,2,3
			BC4	100b	BC4 100b Burst order 4,5,6,7
1b	11b	RFU	BL8	000b	BL8 000b Burst order 0,1,2,3,4,5,6,7
			BC4	000b	BC4 000b Burst order 0,1,2,3
			BC4	100b	BC4 100b Burst order 4,5,6,7

NOTE : Burst order bit 0 is assigned to LSB and the burst order bit 7 is assigned to MSB of the selected MPR agent.

17.10.3 Relevant Timing Parameters

The following AC timing parameters are important for operating the Multi Purpose Register: tRP, tMRD, tMOD, and tMPRR. For more details refer to "Electrical Characteristics & AC Timing for gDDR3-800 to gDDR3-1600" on each component datasheet.

17.10.4 Protocol Example

Protocol Example (This is one example) : Read out predetermined read-calibration pattern.

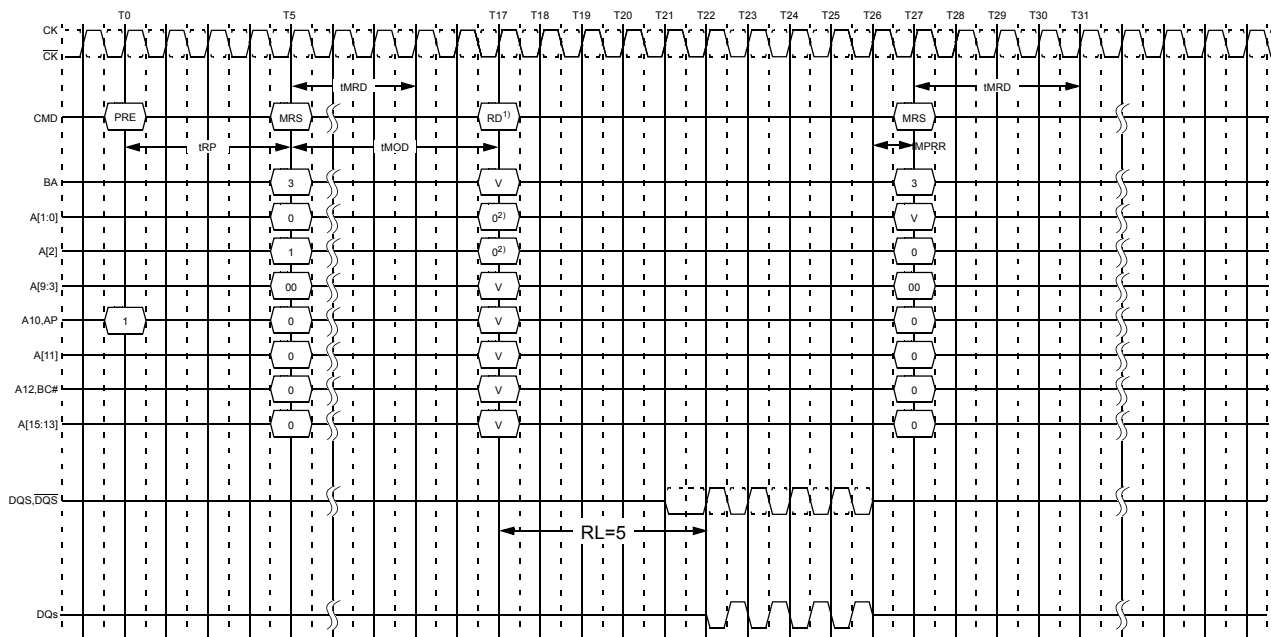
Description: Multiple reads from Multi Purpose Register, in order to do system level read timing calibration based on predetermined and standardized pattern.

Protocol Steps:

- Precharge All.
- Wait until tRP is satisfied.
- MRS MR3, Opcode "A2 = 1b" and "A[1:0] = 00b"
Redirect all subsequent reads into the Multi Purpose Register, and load Pre-defined pattern into MPR.
- Wait until tMRD and tMOD are satisfied (Multi Purpose Register is then ready to be read). During the period MR3 A2 =1, no data write operation is allowed.
- Read:
 - A[1:0] = '00'b (Data burst order is fixed starting at nibble, always '00b' here)
 - A[2] = '0'b (For BL=8, burst order is fixed as 0,1,2,3,4,5,6,7)
 - A12/BC = 1 (use regular burst length of 8)
 - All other address pins (including BA[2:0] and A10/AP): don't care

Readout of predefined pattern for system read calibration with BL8

(RL=5tCK, Fixed Burst order and Single Readout)



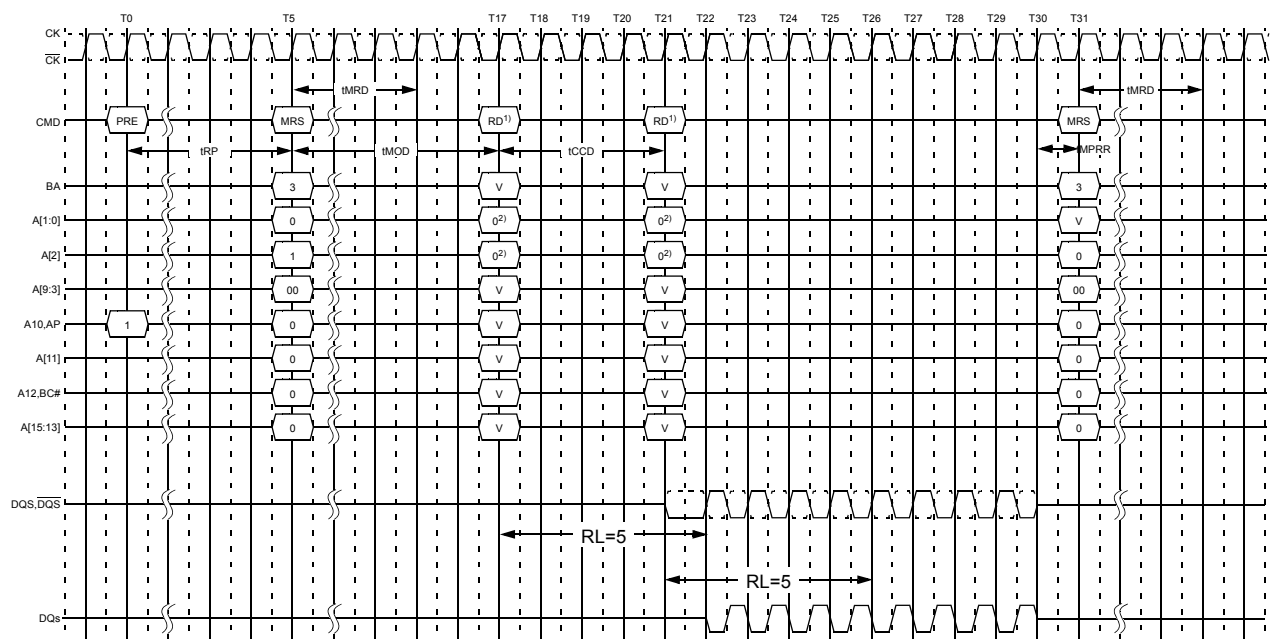
NOTE :

- 1) RD with BL8 either by MRS or On the fly
- 2) Memory Controller must drive Low on A[2:0]

Figure 46. MPR Readout of predefined pattern, BL8 fixed burst order, single readout

Readout of predefined pattern for system read calibration with BL8

(RL=5tCK, Fixed Burst order and Back-to-Back Readout)

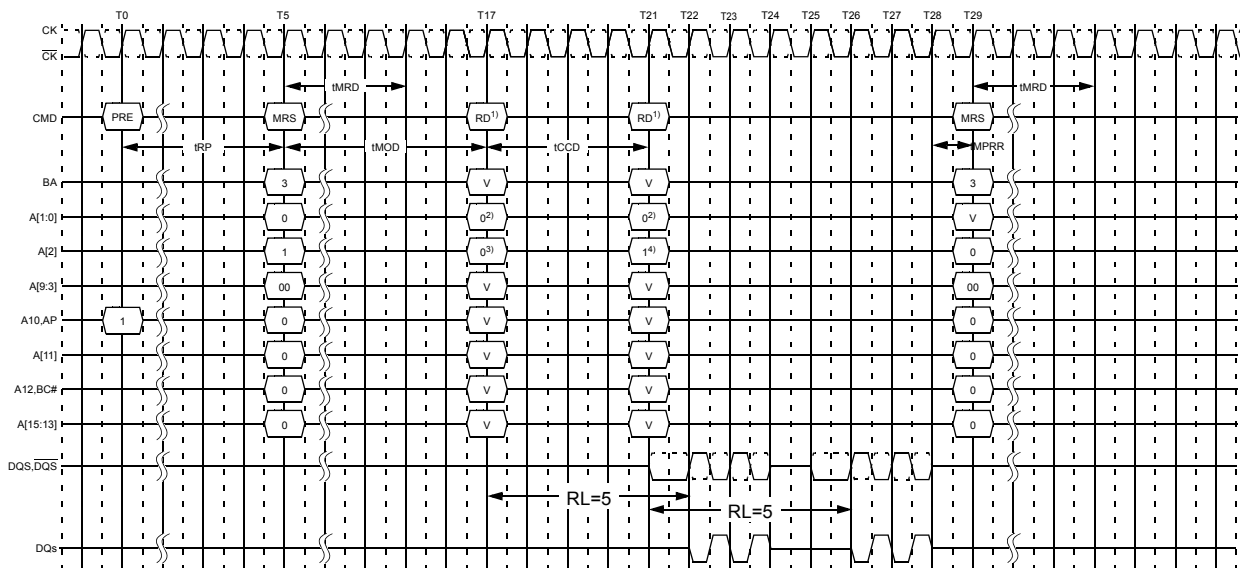


NOTE :

- 1) RD with BL8 either by MRS or On the fly
- 2) Memory Controller must drive Low on A[2:0]

Figure 47. MPR Readout of predefined pattern, BL8 fixed burst order, back-to-back readout

Readout of predefined pattern for system read calibration with BC4
(RL=5tCK, First Lower Nibble than Upper Nibble)

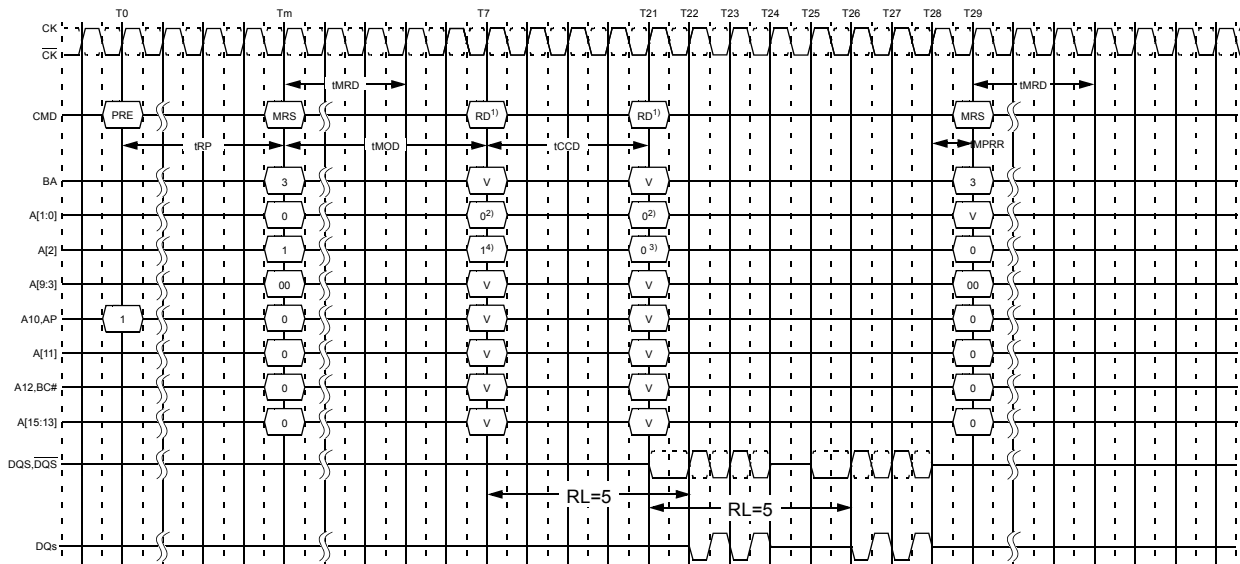


NOTE :

- 1) RD with BL4 either by MRS or On the fly
- 2) Memory Controller must drive Low on A[2:0]
- 3) A[2]=0 selects lower 4 nibble bits 0...3
- 4) A[2]=1 selects upper 4 nibble bits 4...7

Figure 48. MPR Readout predefined pattern, BC4, lower nibble then upper nibble

Readout of predefined pattern for system read calibration with BC4
(RL=5tCK, First Upper Nibble than Lower Nibble)



NOTE :

- 1) RD with BL4 either by MRS or On the fly
- 2) Memory Controller must drive Low on A[2:0]
- 3) A[2]=0 selects lower 4 nibble bits 0...3
- 4) A[2]=1 selects upper 4 nibble bits 4...7

Figure 49. MPR Readout of predefined pattern, BC4, upper nibble then lower nibble

17.11 ACTIVE Command

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0-BA2 inputs selects the bank, and the address provided on inputs A0-A15 selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

17.12 PRECHARGE Command

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (t_{RP}) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

17.13 READ Operation

Any system or application incorporating random access memory products should be properly designed, tested and qualified to ensure proper use or access of such memory products. Disproportionate, excessive and/or repeated access to a particular address or addresses may result in reduction of product life.

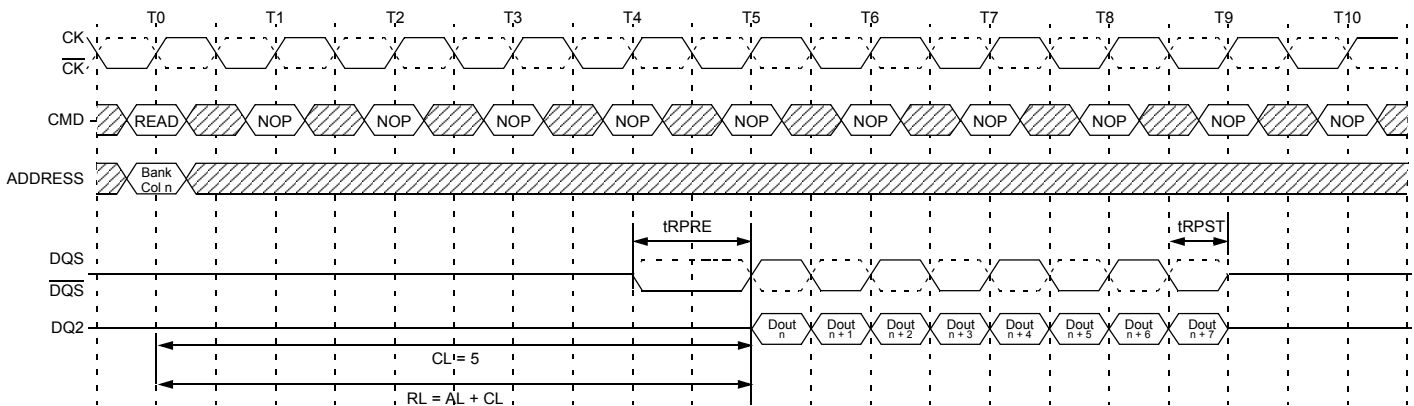
17.13.1 READ Burst Operation

During a READ or WRITE command, gDDR3 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (AUTO PRECHARGE can be enabled or disabled).

A12 = 0, BC4 (BC4 = burst chop, $t_{CCD} = 4$)

A12 = 1, BL8

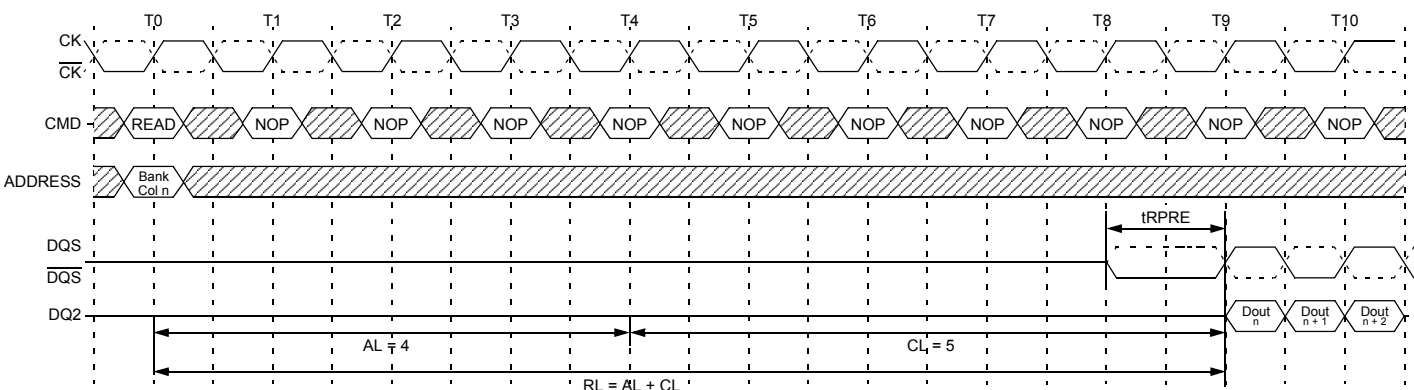
A12 is used only for burst length control, not as a column address.



NOTE :

1. BL8, RL = 5, AL = 0, CL = 5.
2. DOUT n = data-out from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either $MR0[A1:0 = 00]$ or $MR0[A1:0 = 01]$ and A12 = 1 during READ command at T_0 .

Figure 50. READ Burst Operation $RL = 5$ ($AL = 0$, $CL = 5$, $BL8$)



NOTE :

1. BL8, RL = 9, AL = (CL - 1), CL = 5.
2. DOUT n = data-out from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.

4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.

Figure 51. READ Burst Operation RL = 9 (AL = 4, CL = 5, BL8)

17.13.2 READ Timing Definitions

Read timing is shown in Figure 52 and is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:

- tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK, $\overline{\text{CK}}$.
- tDQSCK is the actual position of a rising strobe edge relative to CK, $\overline{\text{CK}}$.
- tQSH describes the DQS, $\overline{\text{DQS}}$ differential output high time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tQSL describes the DQS, $\overline{\text{DQS}}$ differential output low time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.
- tDQSQ; both rising/falling edges of DQS, no tAC defined.

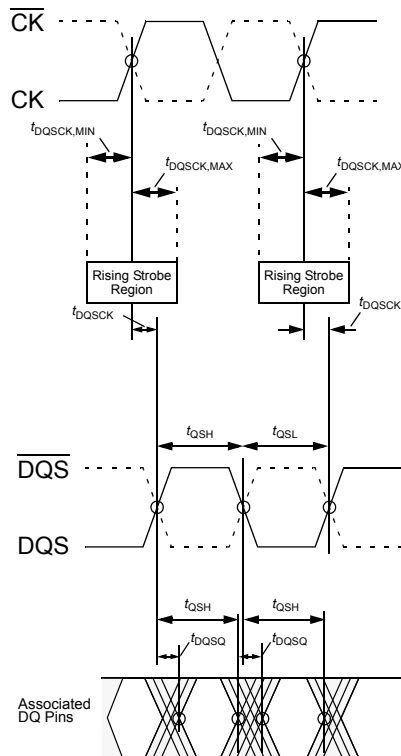


Figure 52. Read Timing Definition

17.13.2.1 gDDR3 Clock to Data Strobe relationship

Clock to Data Strobe relationship is shown in Figure 53 and is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:

- t_{DQSK} min/max describes the allowed range for a rising data strobe edge relative to $\overline{CK}$, $\overline{CK}$.
- t_{DQSK} is the actual position of a rising strobe edge relative to $\overline{CK}$, $\overline{CK}$.

- t_{QSH} describes the data strobe high pulse width.

Falling data strobe edge parameters:

- t_{QSL} describes the data strobe low pulse width.

$t_{LZ}(DQS)$, $t_{HZ}(DQS)$ for preamble/postamble (see 17.13.2.3 and Figure 55)

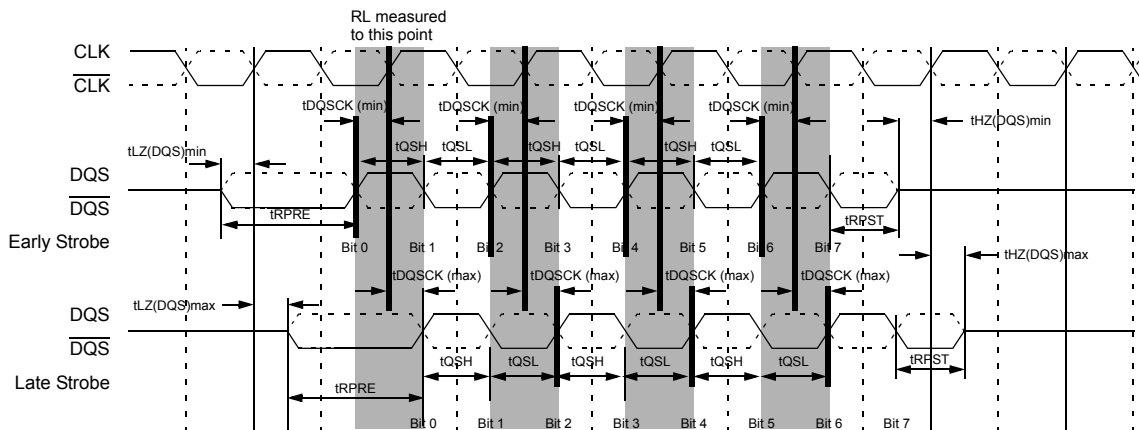


Figure 53. Clock to Data Strobe Relationship

NOTE :

1. Within a burst, rising strobe edge is not necessarily fixed to be always at $t_{DQSK}(\min)$ or $t_{DQSK}(\max)$. Instead, rising strobe edge can vary between $t_{DQSK}(\min)$ and $t_{DQSK}(\max)$.
2. Notwithstanding note 1, a rising strobe edge with $t_{DQSK}(\max)$ at $T(n)$ can not be immediately followed by a rising strobe edge with $t_{DQSK}(\min)$ at $T(n+1)$. This is because other timing relationships (t_{QSH} , t_{QSL}) exist:
if $t_{DQSK}(n+1) < 0$:
$$t_{DQSK}(n) < 1.0 \text{ tCK} - (t_{QSH}(\min) + t_{QSL}(\min)) - |t_{DQSK}(n+1)|$$
3. The $\overline{DQS}$, $\overline{DQS}$ differential output high time is defined by t_{QSH} and the $\overline{DQS}$, $\overline{DQS}$ differential output low time is defined by t_{QSL} .
4. Likewise, $t_{LZ}(DQS)_{\min}$ and $t_{HZ}(DQS)_{\min}$ are not tied to $t_{DQSK}(\min)$ (early strobe case) and $t_{LZ}(DQS)_{\max}$ and $t_{HZ}(DQS)_{\max}$ are not tied to $t_{DQSK}(\max)$ (late strobe case).
5. The minimum pulse width of read preamble is defined by $t_{RPST}(\min)$.
6. The maximum read postamble is bound by $t_{DQSK}(\min)$ plus $t_{QSH}(\min)$ on the left side and $t_{HZDSQ}(\max)$ on the right side.
7. The minimum pulse width of read postamble is defined by $t_{RPST}(\min)$.
8. The maximum read preamble is bound by $t_{LZDQS}(\min)$ on the left side and $t_{DQSK}(\max)$ on the right side.

17.13.2.2 gDDR3 Data Strobe to Data relationship

The Data Strobe to Data relationship is shown in Figure 54 and is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

tDQSQ; both rising/falling edges of DQS, no tAC defined

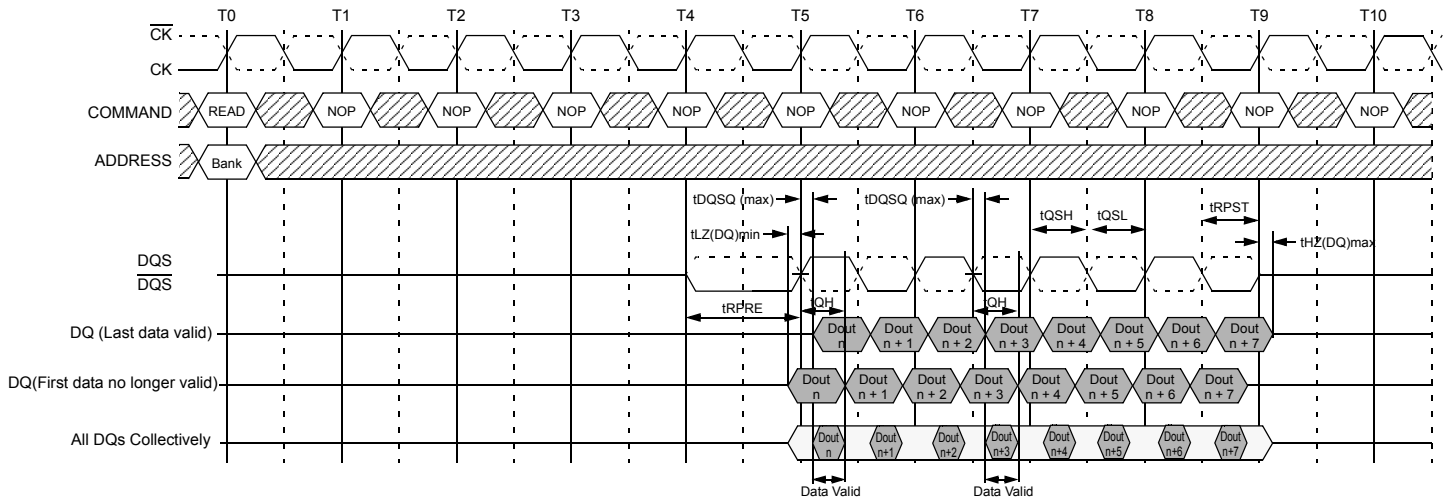


Figure 54. Data Strobe to Data Relationship

NOTE :

1. BL = 8, RL = 5 (AL = 0, CL = 5)
2. DOUT n = data-out from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.
5. Output timings are referenced to $V_{DDQ}/2$, and DLL on for locking.
6. tDQSQ defines the skew between DQS, $\overline{DQS}$ to Data and does not define DQS, $\overline{DQS}$ to Clock.
7. Early Data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst.

17.13.2.3 tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation

tHZ and tLZ transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ). Figure 55 shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as singled ended.

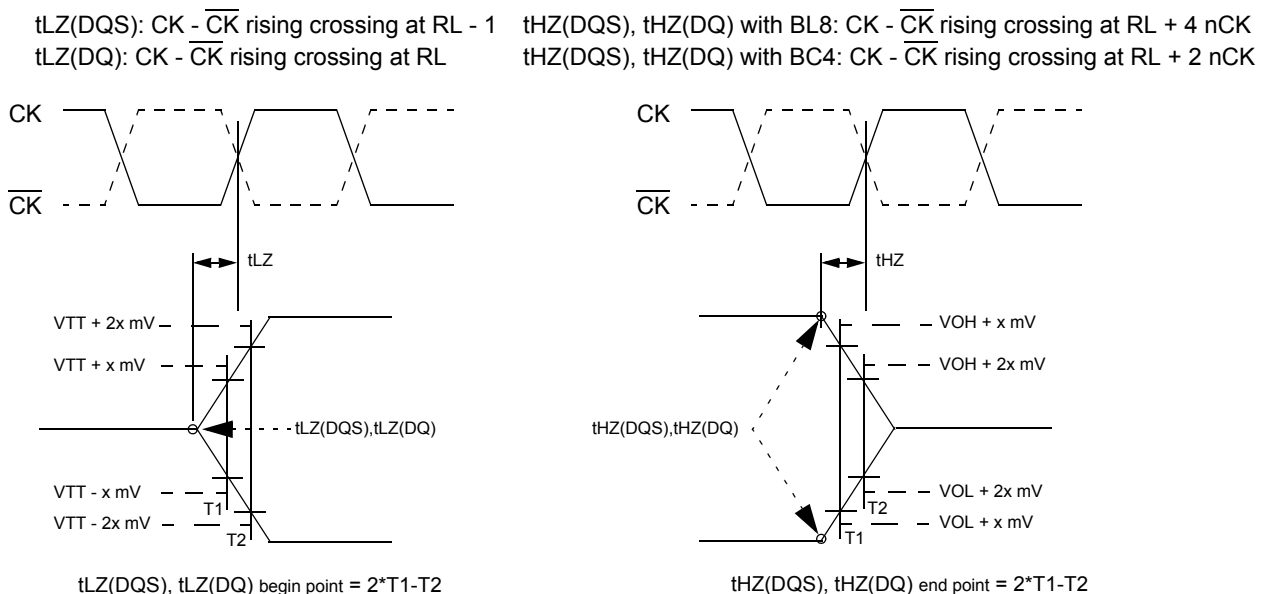


Figure 55. tLZ and tHZ method for calculating transitions and endpoints

17.13.2.4 tRPRE Calculation

Method for calculating differential pulse widths for tRPRE.

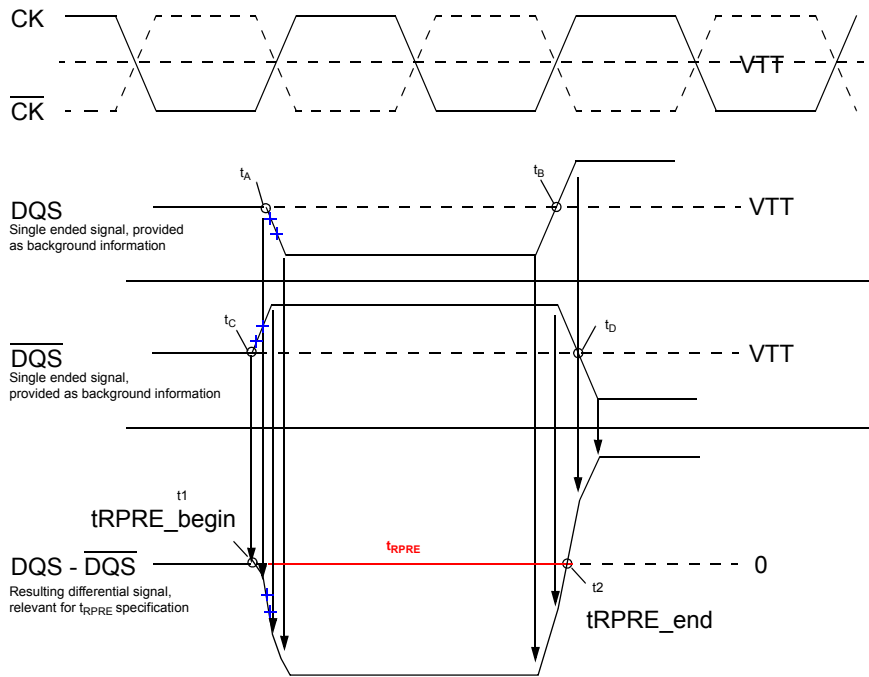


Figure 56. Method for calculating tRPRE transitions and endpoints

17.13.2.5 tRPST Calculation

Method for calculating differential pulse widths for tRPST.

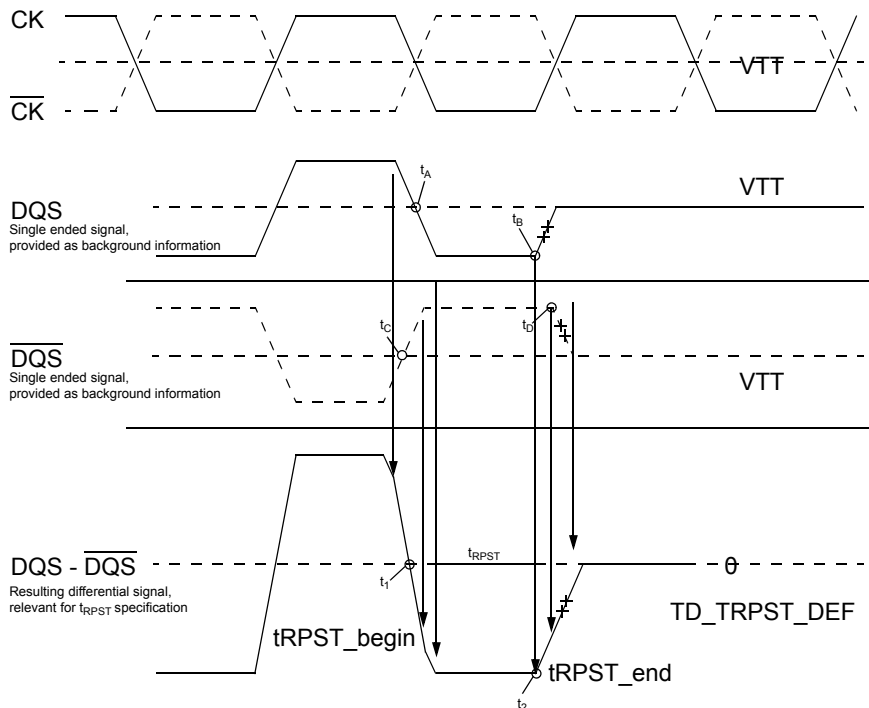
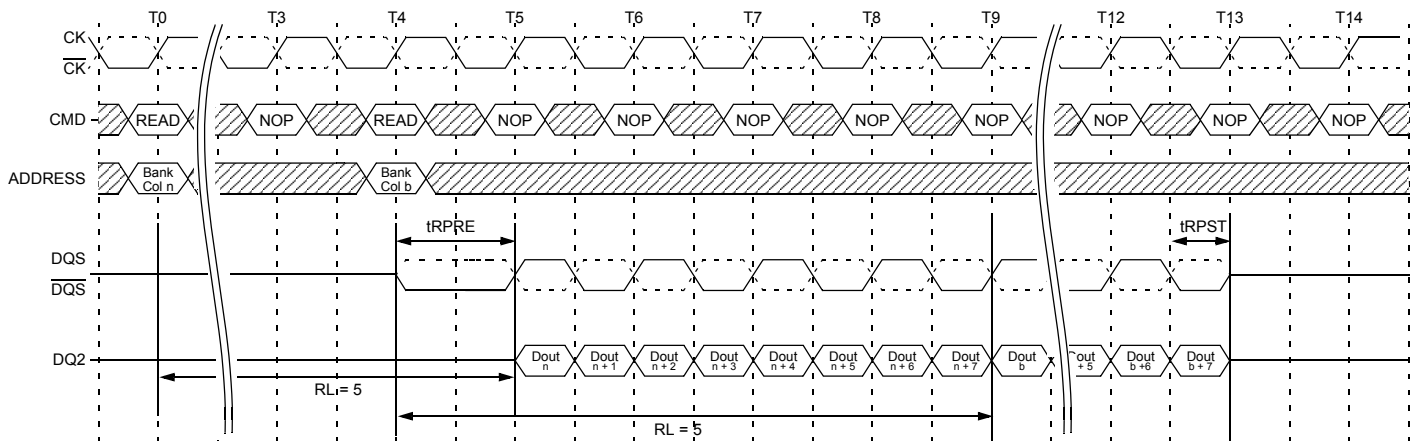
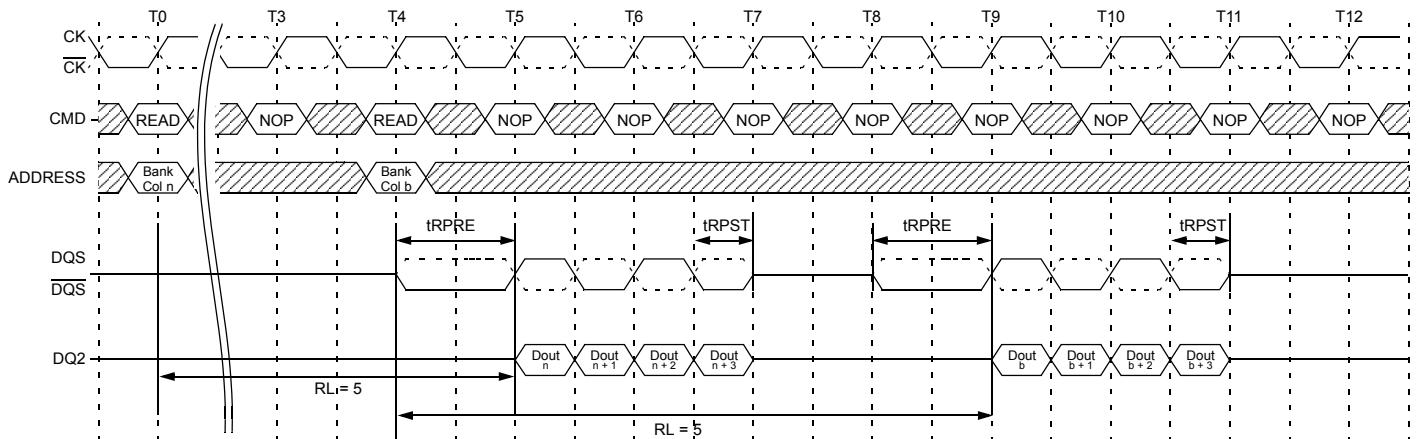


Figure 57. Method for calculating tRPST transitions and endpoints

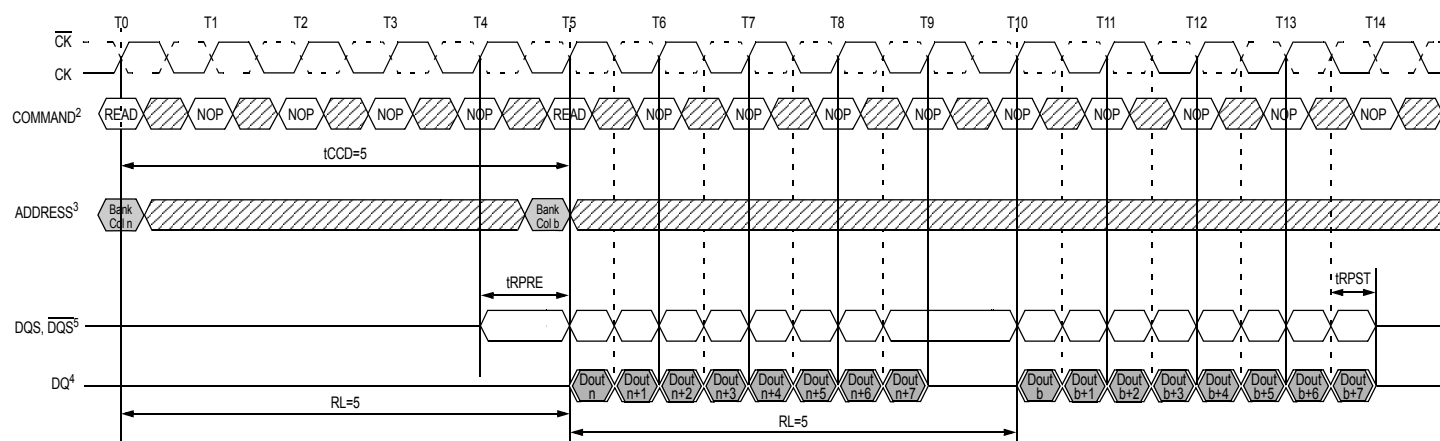
**NOTE :**

1. BL8, RL = 5 (CL = 5, AL = 0)
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0 = 01] and A12 = 1 during READ commands at T0 and T4.

Figure 58. READ (BL8) to READ (BL8)**NOTE :**

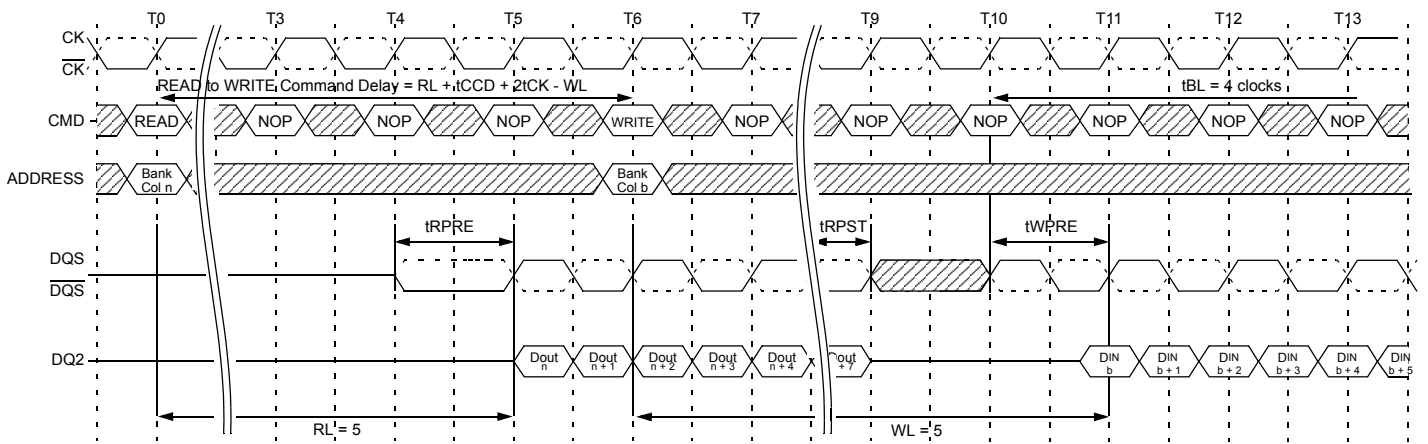
1. BL4, RL = 5 (CL = 5, AL = 0)
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0 = 01] and A12 = 0 during READ commands at T0 and T4.

Figure 59. READ (BC4) to READ (BC4)

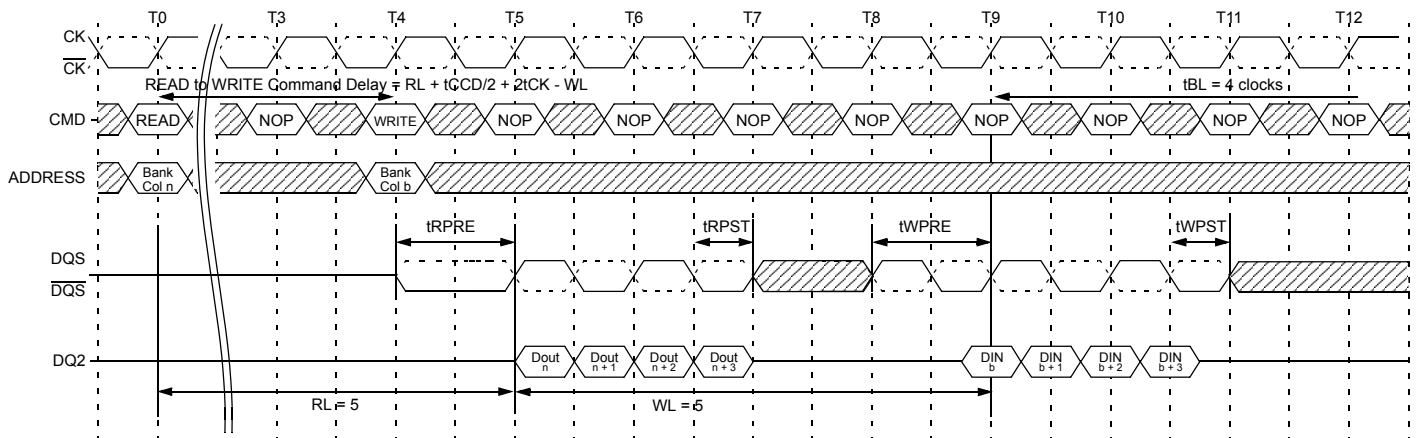
**NOTE :**

1. BL8, RL = 5 (CL = 5, AL = 0), tCCD=5
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0 = 01] and A12 = 1 during READ commands at T0 and T5.
5. DQS-DQS is held logic low at T9.

Figure 60. Nonconsecutive READ (BL8) to READ (BL8)

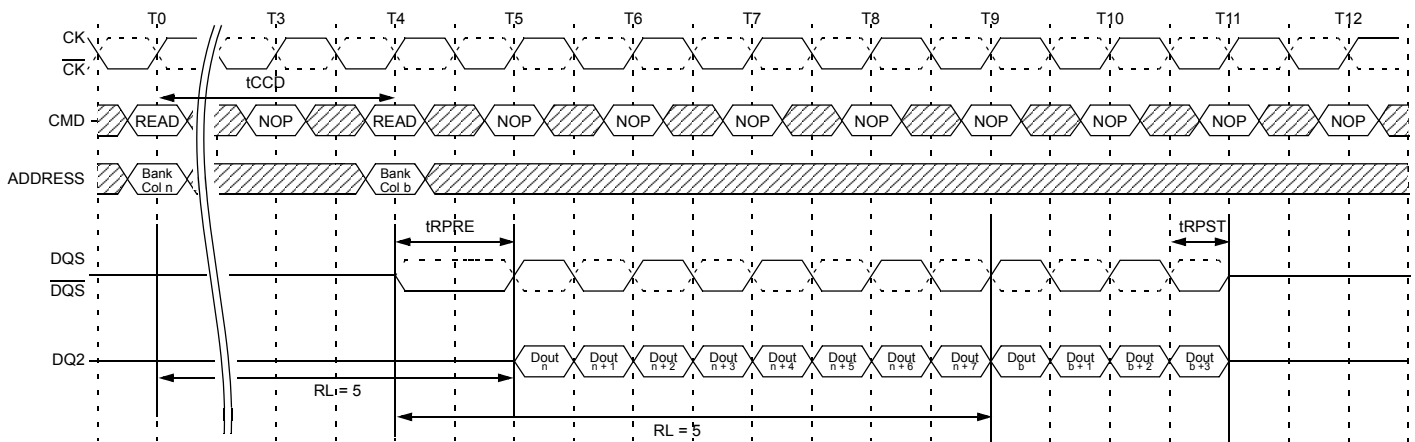
**NOTE :**

1. BL8, RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. Dout n = data-out from column, DIN b = data-in from column b.
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0 = 01] and A12 = 1 during READ commands at T0 and WRITE command at T6.

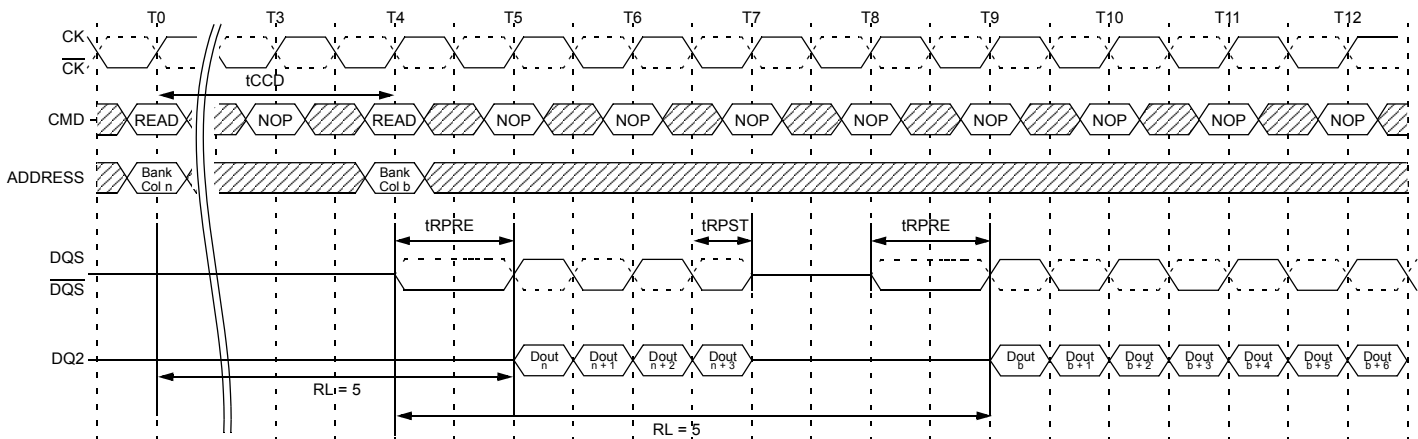
Figure 61. READ (BL8) to WRITE (BL8)**NOTE :**

1. BL4, RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. Dout n = data-out from column, DIN b = data-in from column b.
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL4 setting activated by either MR0[A1:0=00] or MR0[A1:0 = 01] and A12 = 1 during READ commands at T0 and WRITE command at T4.

Figure 62. READ (BC4) to WRITE (BC4) OTF

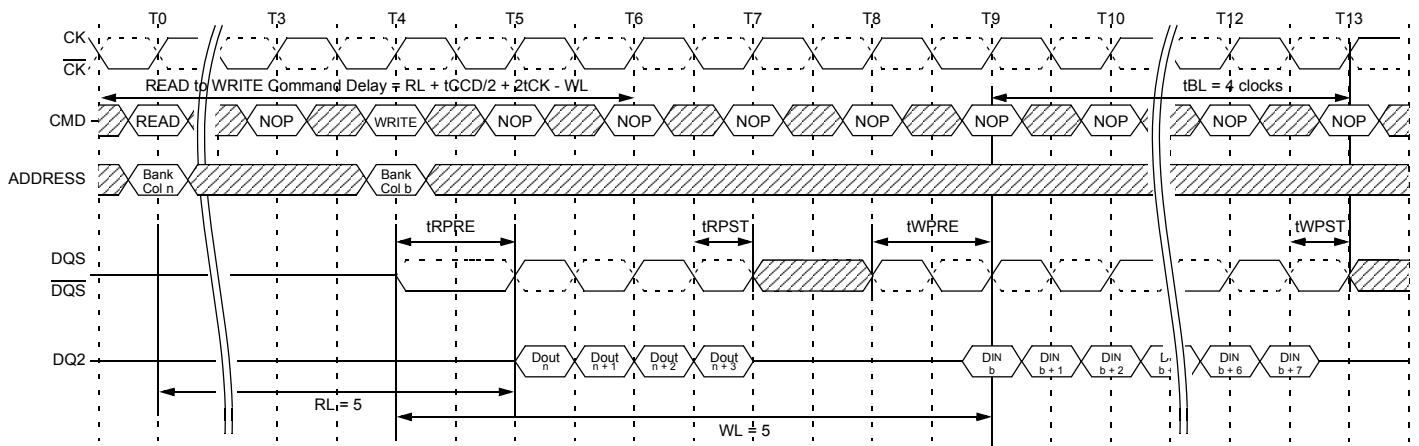
**NOTE :**

1. RL = 5 (CL = 5, AL = 0)
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] and A12 = 1 during READ commands at T0.
BC4 setting activated by either MR0[A1:0=01] and A12 = 0 during READ commands at T4.

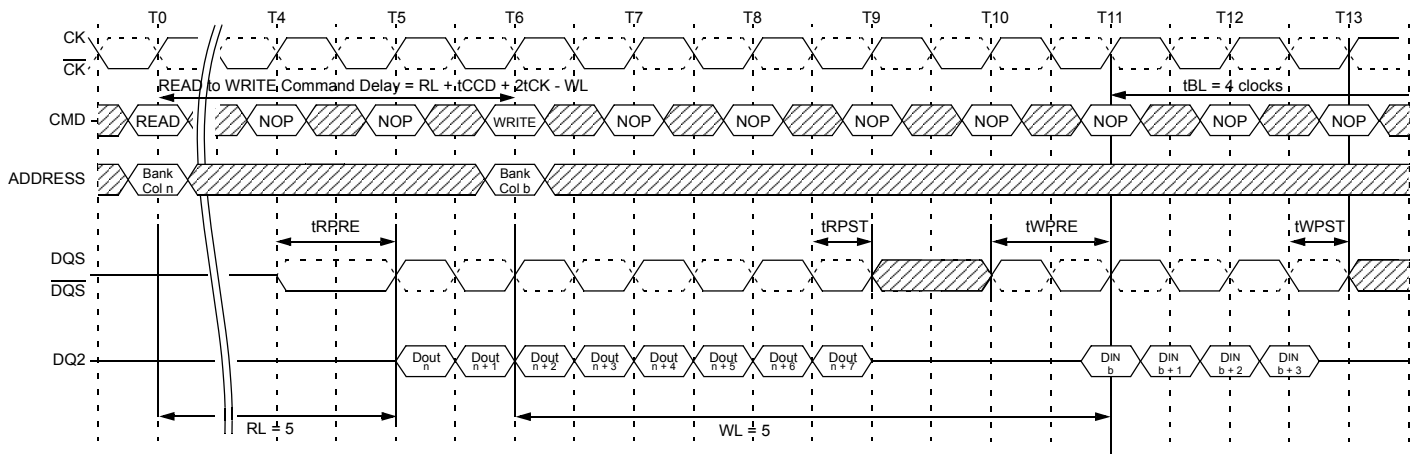
Figure 63. READ (BL8) to READ (BC4) OTF**NOTE :**

1. RL = 5 (CL = 5, AL = 0)
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BC4 setting activated by either MR0[A1:0=00] and A12 = 1 during READ commands at T0.
BL8 setting activated by either MR0[A1:0=01] and A12 = 0 during READ commands at T4.

Figure 64. READ (BC4) to READ (BL8) OTF

**NOTE :**

1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 1, AL = 0)
2. Dout n = data-out from column, DIN b = data-in from column b.
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BC4 setting activated by either MR0[A1:0=00] and A12 = 0 during READ commands at T0.
BL8 setting activated by either MR0[A1:0=01] and A12 = 1 during WRITE commands at T4.

Figure 65. READ (BC4) to WRITE (BL8) OTF**NOTE :**

1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. Dout n = data-out from column, DIN b = data-in from column b.
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] and A12 = 1 during READ commands at T0.
BC4 setting activated by either MR0[A1:0=01] and A12 = 0 during WRITE commands at T6.

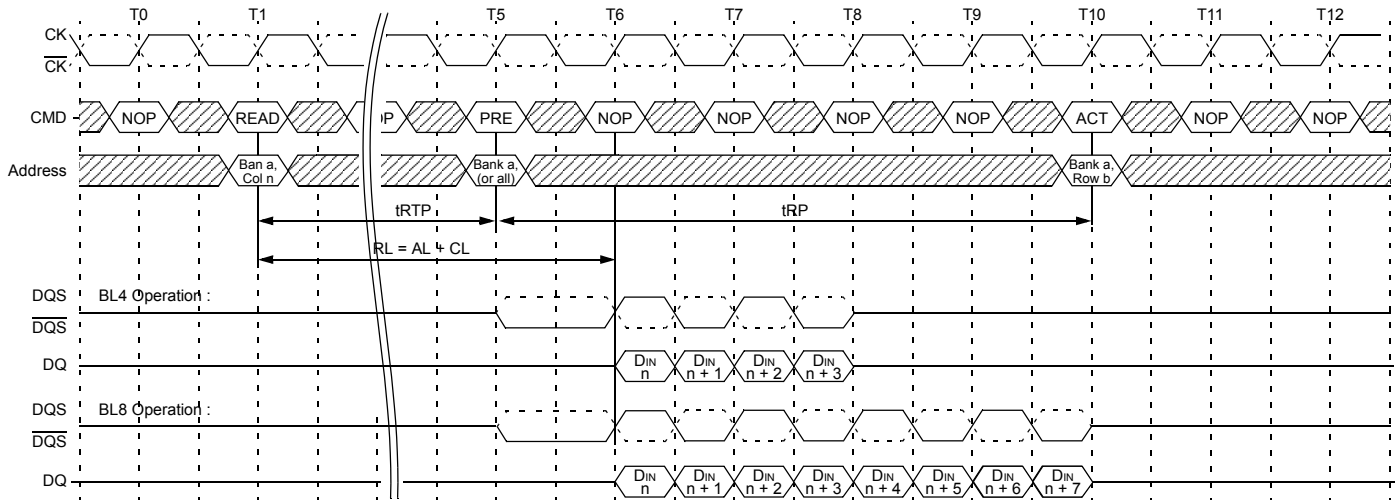
Figure 66. READ (BL8) to WRITE (BC4) OTF

17.13.3 Burst Read Operation followed by a Precharge

The minimum external Read command to Precharge command spacing to the same bank is equal to $AL + tRTP$ with $tRTP$ being the Internal Read Command to Precharge Command Delay. Note that the minimum ACT to PRE timing, $tRAS$, must be satisfied as well. The minimum value for the Internal Read Command to Precharge Command Delay is given by $tRTP.MIN = \max(4 \times nCK, 7.5 \text{ ns})$. A new bank active command may be issued to the same bank if the following two conditions are satisfied simultaneously:

1. The minimum RAS precharge time ($tRP.MIN$) has been satisfied from the clock at which the precharge begins.
2. The minimum RAS cycle time ($tRC.MIN$) from the previous bank activation has been satisfied.

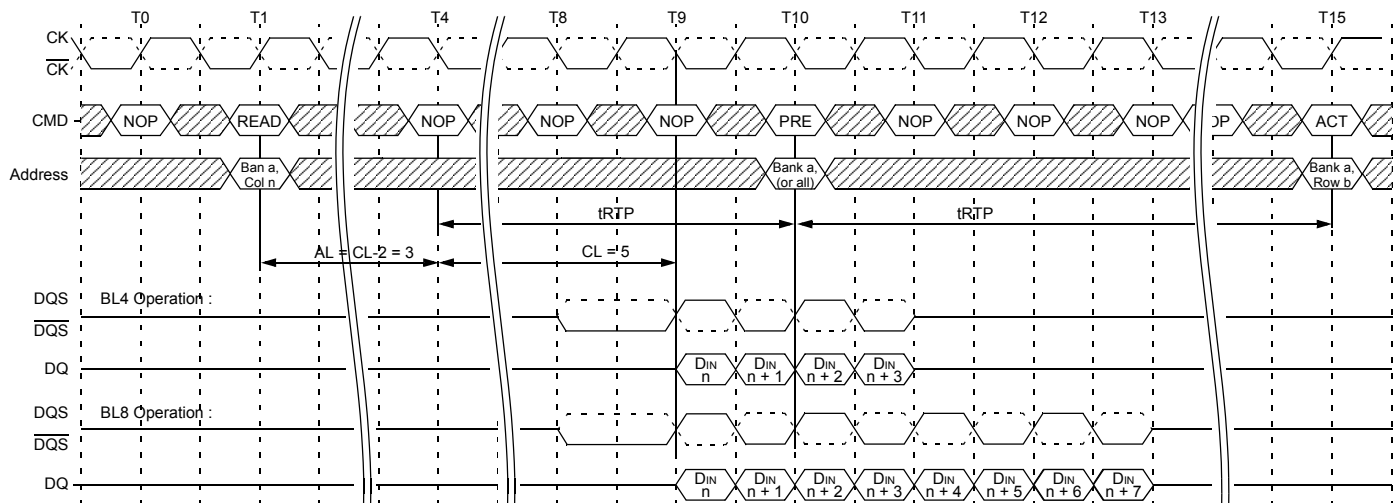
Examples of Read commands followed by Precharge are shown in Figure 67 and Figure 68.



NOTE :

1. $RL = 5$ ($CL = 5$, $AL = 0$)
2. $DOUT\ n$ = data-out from column n .
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes $tRAS.MIN$ is satisfied at Precharge command time ($T5$) and that $tRC.MIN$ is satisfied at the next Active command time ($T10$).

Figure 67. READ to PRECHARGE, $RL=5$, $AL=0$, $CL=5$, $tRTP=4$, $tRP=5$



NOTE :

1. $RL = 8$ ($CL = 5$, $AL = CL - 2$)
2. $DOUT\ n$ = data-out from column n .
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes $tRAS.MIN$ is satisfied at Precharge command time ($T10$) and that $tRC.MIN$ is satisfied at the next Active command time ($T15$).

Figure 68. READ to RRECHARGE, $RL=8$, $AL=CL-2$, $CL=5$, $tRTP=6$, $tRP=5$

17.14 WRITE Operation

17.14.1 gDDR3 Burst Operation

During a READ or WRITE command, gDDR3 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (AUTO PRECHARGE can be enabled or disabled).

A12 = 0, BC4 (BC4 = burst chop, tCCD = 4)

A12 = 1, BL8

A12 is used only for burst length control, not as a column address.

17.14.2 WRITE Timing Violations

17.14.2.1 Motivation

Generally, if timing parameters are violated, a complete reset/initialization procedure has to be initiated to make sure the DRAM works properly. However, it is desirable for certain minor violations that the DRAM is guaranteed not to "hang up" and errors be limited to that particular operation. (for reference: add more motivation here later, or refer to the "Read Synchronization" section if available) For the following, it will be assumed that there are no timing violations w.r.t. to the Write command itself (including ODT, etc.) and that it does satisfy all timing requirements not mentioned below.

17.14.2.2 Data Setup and Hold Violations

Should the data to strobe timing requirements (tDS, tDH) be violated, for any of the strobe edges associated with a write burst, then wrong data might be written to the memory location addressed with this WRITE command. In the example (Figure 69 on page 104), the relevant strobe edges for write burst A are associated with the clock edges: T5, T5.5, T6, T6.5, T7, T7.5, T8, T8.5. Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise.

17.14.2.3 Strobe to Strobe and Strobe to Clock Violations

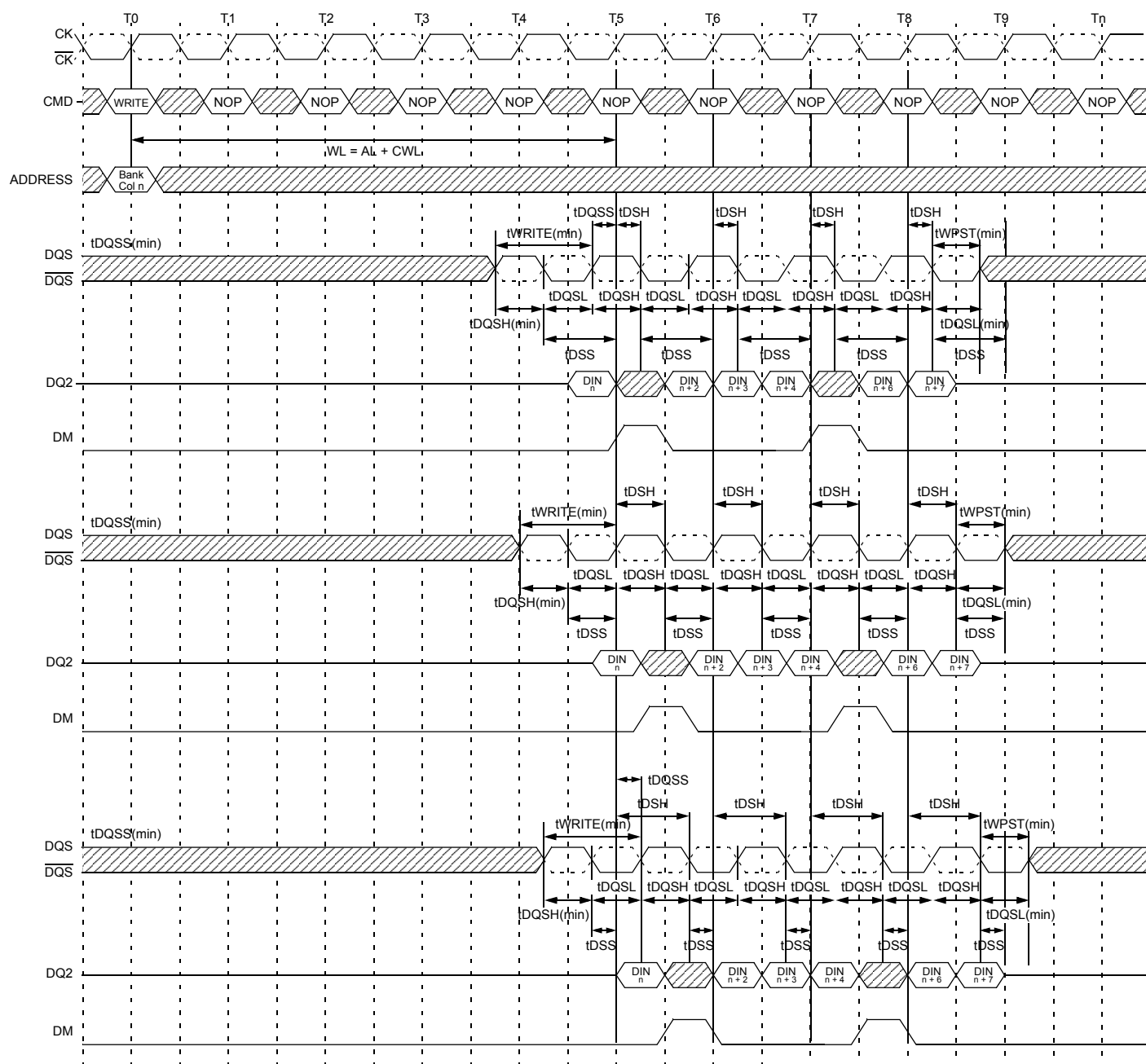
Should the strobe timing requirements (tDQSH, tDQSL, tWPRE, tWPST) or the strobe to clock timing requirements (tDSS, tDSH, tDQSS) be violated, for any of the strobe edges associated with a Write burst, then wrong data might be written to the memory location addressed with the offending WRITE command. Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise.

In the example (Figure 69 on page 104) the relevant strobe edges for Write burst A are associated with the clock edges: T4, T4.5, T5, T5.5, T6, T6.5, T7, T7.5, T8, T8.5 and T9. Any timing requirements starting or ending on one of these strobe edges need to be fulfilled for a valid burst.

For Write burst B the relevant edges are T8, T8.5, T9, T9.5, T10, T10.5, T11, T11.5, T12, T12.5 and T13. Some edges are associated with both bursts.

17.14.2.4 Write Timing Parameters

This drawing is for example only to enumerate the strobe edges that "belong" to a Write burst. No actual timing violations are shown here. For a valid burst all timing parameters for each edge of a burst need to be satisfied (not only for one edge - as shown).



NOTE :

1. BL8, WL = 5 (AL = 0, CWL = 5)
2. DIN n = data-in from column n
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:0=10] or MR0[A1:0 = 01] and A12 = 1 during WRITE commands at T0.
5. tDQSS must be met at each rising clock edge.

Figure 69. gDDR3 Write Timing Definition & Parameters

17.14.3 Write Data Mask

One write data mask (DM) pin for each 8 data bits (DQ) will be supported on gDDR3 SDRAMs, consistent with the implementation on DDR2 SDRAMs. It has identical timings on write operations as the data bits as shown in Figure 69, and though used in a unidirectional manner, is internally loaded identically to data bits to ensure matched system timing. DM is not used during read cycles for any bit organizations including x4, x8, and x16, however, DM of x8 bit organization can be used as TDQS during write cycles if enabled by the MR1[A11] setting. See Figure 16.4.3.7 for more details on TDQS vs. DM operations.

17.14.4 tWPRE Calculation

Method for calculating differential pulse widths for tWPRE is shown in Figure

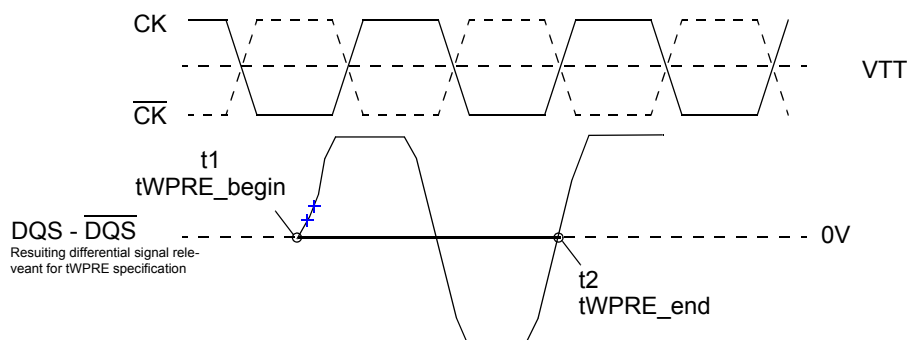


Figure 70. Method for calculating tWPRE transitions and endpoints

17.14.5 tWPST Calculation

Method for calculating differential pulse widths for tWPST is shown in Figure

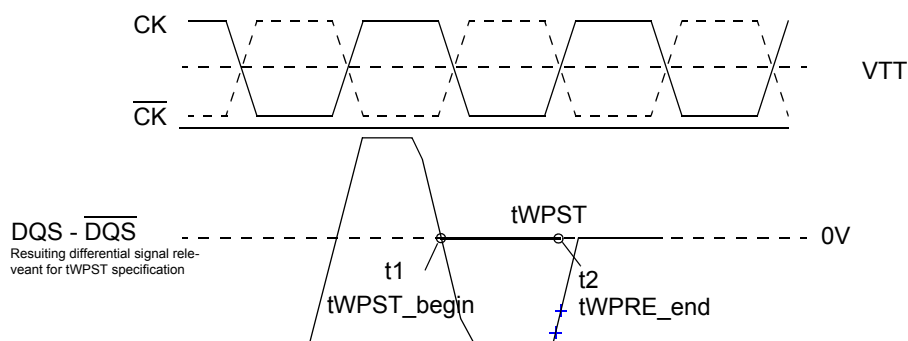
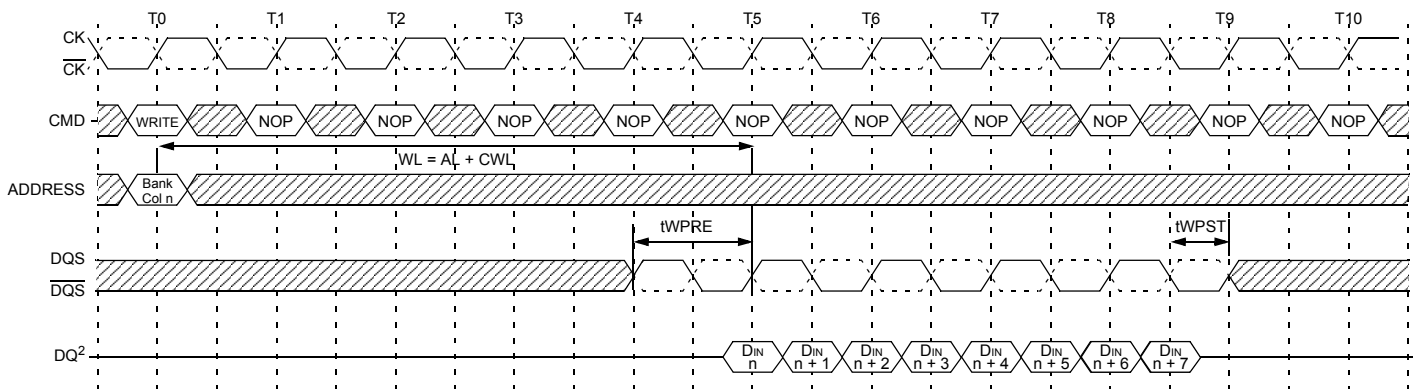
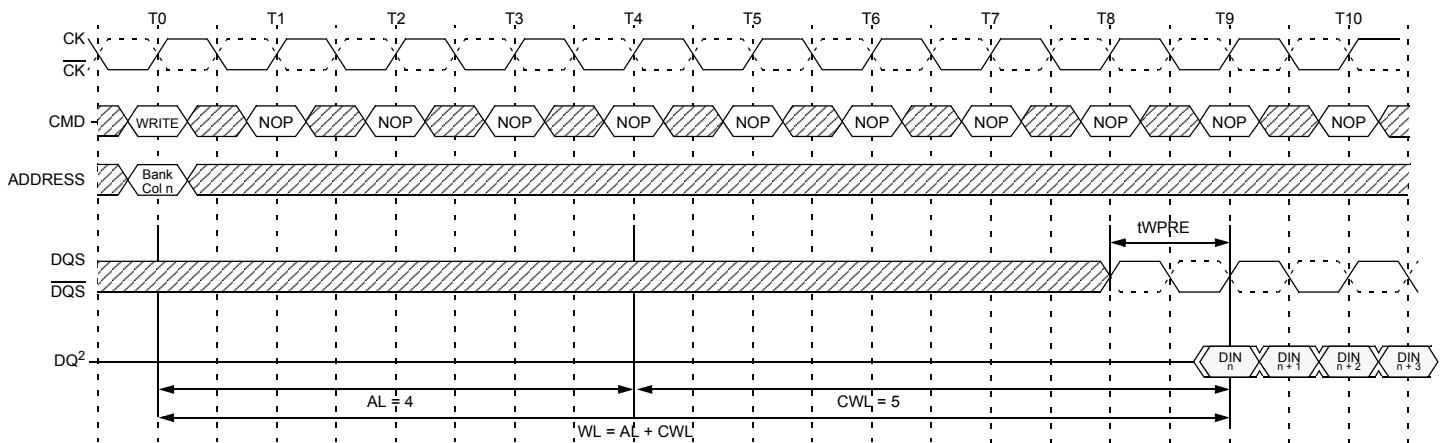


Figure 71. Method for calculating tWPST transitions and endpoints

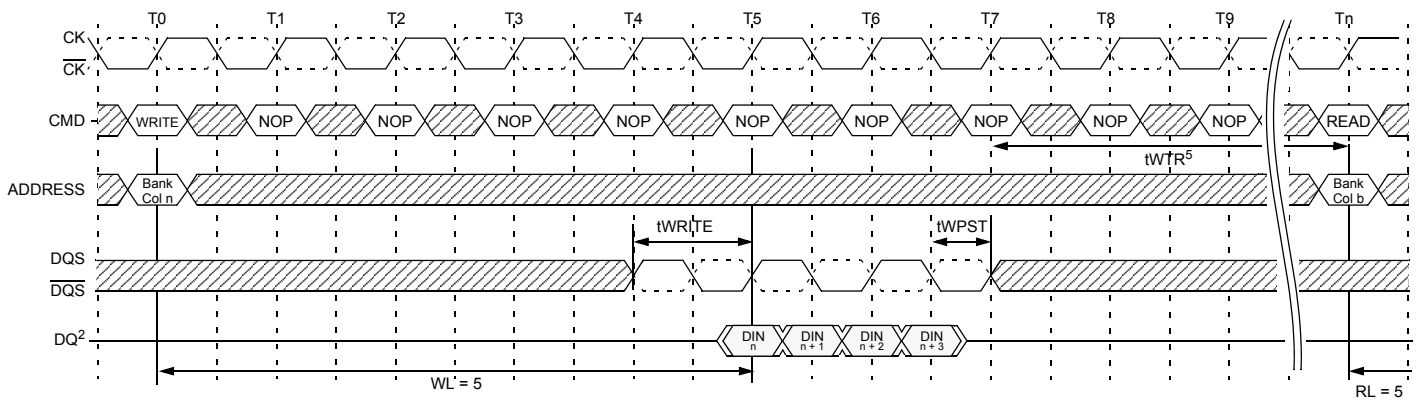
**NOTE :**

1. BL8, WL = 5, AL = 0, CWL = 5
2. DIN n = data-in from column n.
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0=01] and A12 = 1 during WRITE commands at T0.

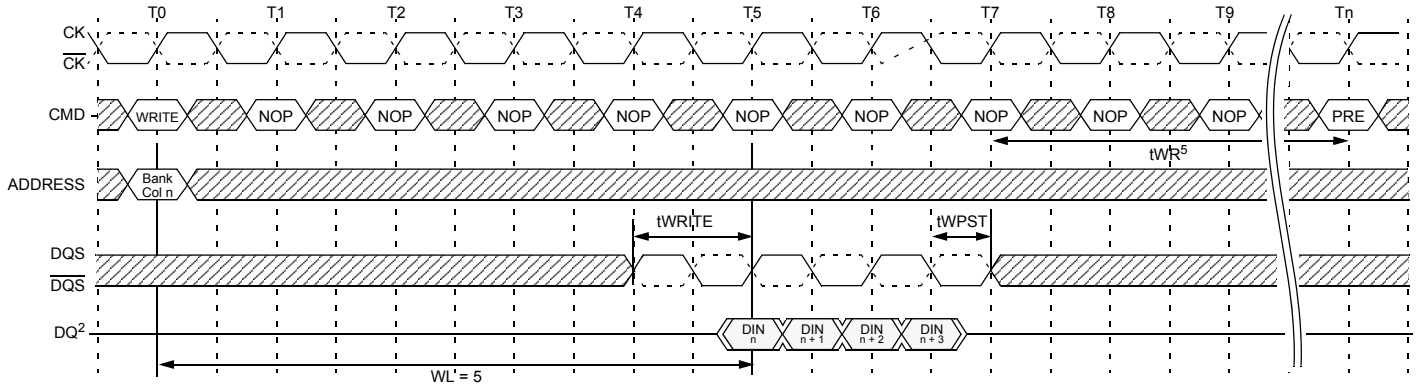
Figure 72. WRITE Burst Operation WL=5 (AL=0, CWL=5, BL8)**NOTE :**

1. BL8, WL = 9, AL = (CL - 1), CL = 5, CWL = 5
2. DIN n = data-in from column n.
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0=01] and A12 = 1 during WRITE commands at T0.

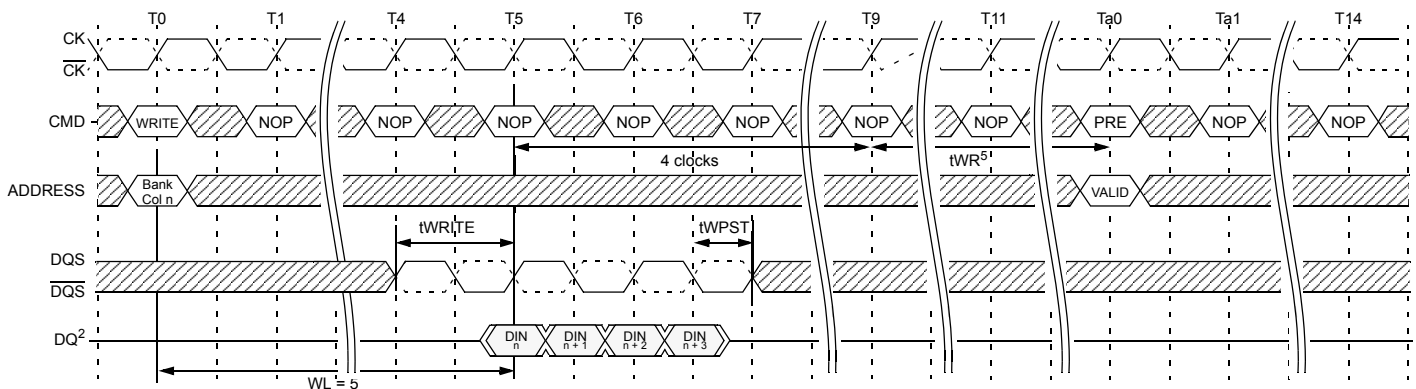
Figure 73. WRITE Burst Operation WL=9 (AL=CL-1, CWL=5, BL8)

**NOTE :**

1. BC4, WL = 5, RL = 0
2. DIN n = data-in from column n ; DOUT b = data-out from column b.
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0=10] during WRITE commands at T0 and READ command at Tn.
5. tWR controls the write to read delay to the same device and starts with the first rising clock edge after the last write data shown at T7.

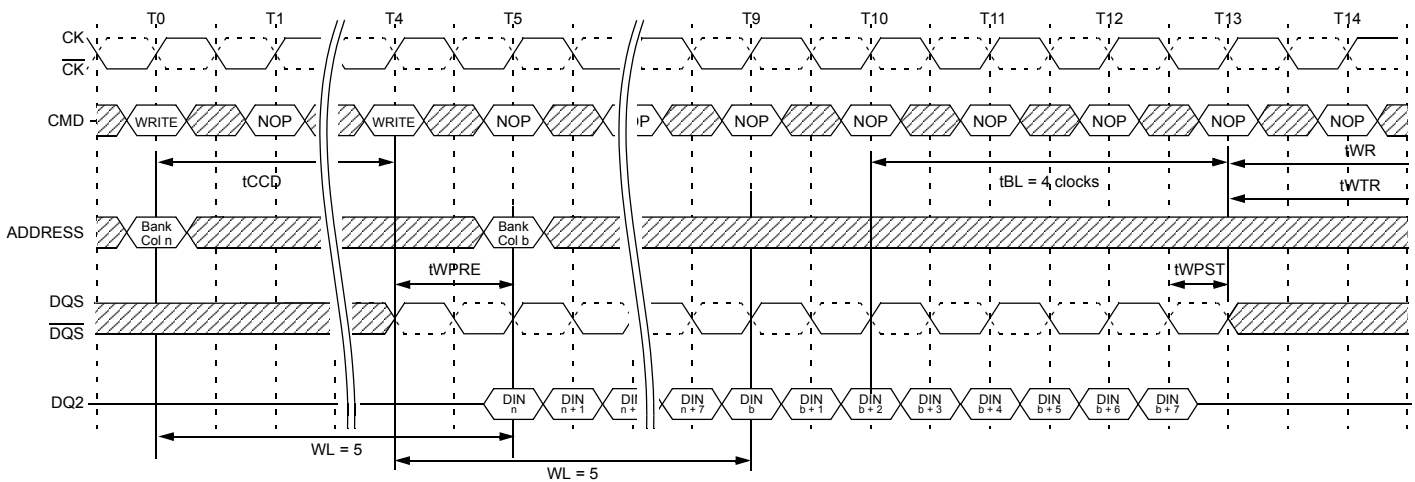
Figure 74. WRITE (BC4) to READ (BC4) Operation**NOTE :**

1. BC4, WL = 5, RL = 5.
2. DIN n = data-in from column n ; DOUT b = data-out from column b.
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 10] during WRITE command at T0.
5. The write recovery time (tWR) referenced from the first rising clock edge after the last write data shown at T7. tWR specifies the last burst write cycle until the precharge command can be issued to the same bank.

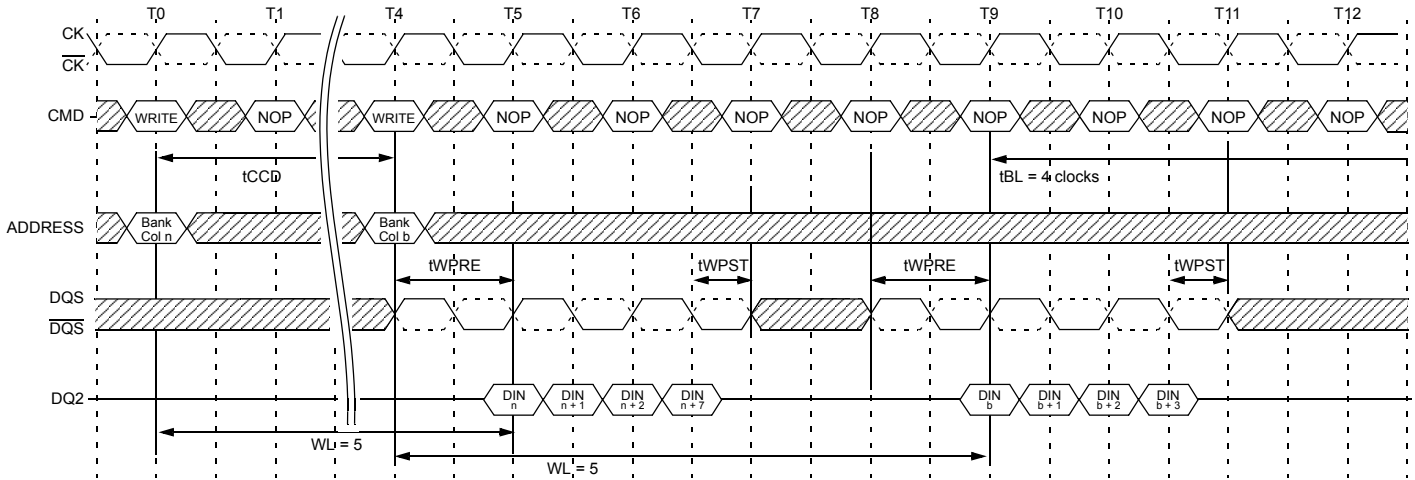
Figure 75. WRITE (BC4) to PRECHARGE Operation**NOTE :**

1. BC4 OTF, WL = 5 (CWL = 5, AL = 0)
2. DIN n (or b) = data-in from column n.
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BC4 OTF setting activated by MR0[A1:0 = 01] and A12 = 0 during WRITE command at T0.
5. The write recovery time (tWR) starts at the rising clock edge T9 (4 clocks from T5).

Figure 76. WRITE (BC4) OTF to PRECHARGE Operation

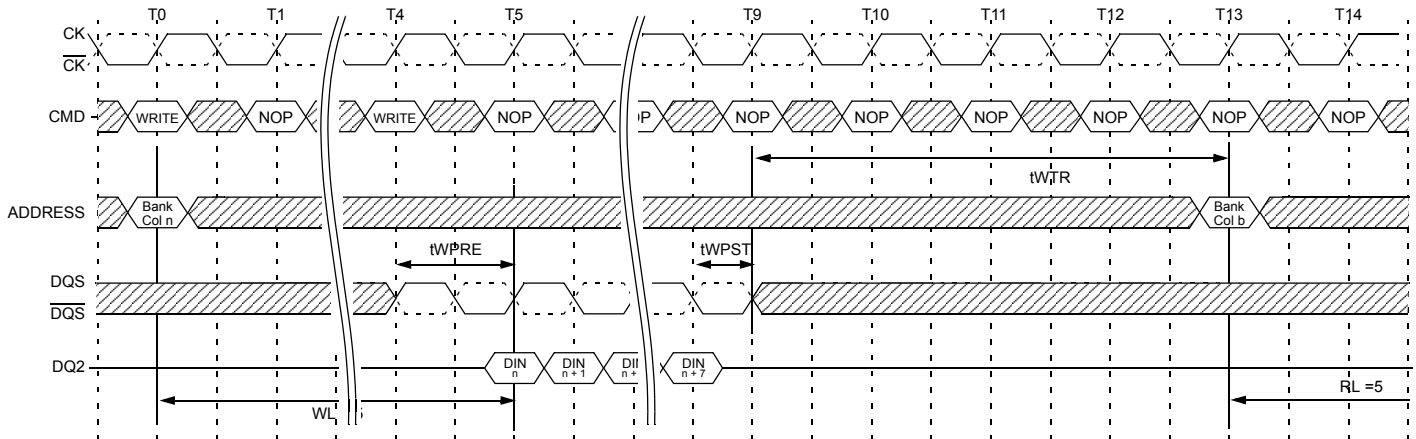
**NOTE :**

1. BL8, WL = 5 (CWL = 5, AL = 0)
2. DIN n (or b) = data-in from column n (or column b.)
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0=01] and A12 = 1 during WRITE commands at T0 and T4
5. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T13.

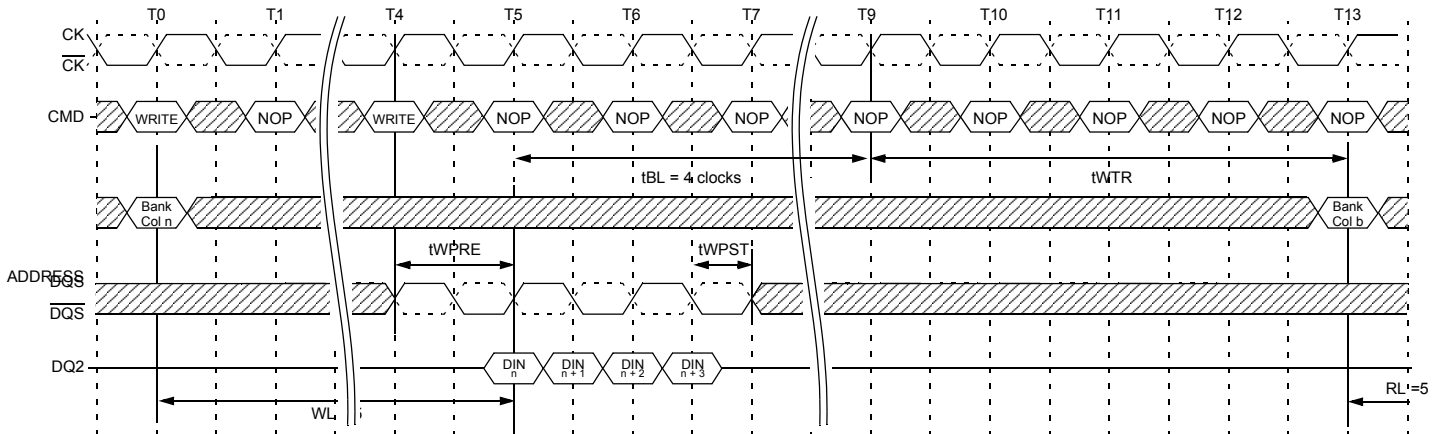
Figure 77. WRITE (BL8) to WRITE (BL8)**NOTE :**

1. BC4, WL = 5 (CWL = 5, AL = 0)
2. DIN n (or b) = data-in from column n (or column b.)
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0=01] and A12 = 0 during WRITE commands at T0 and T4
5. BC4 setting activated by MR0[A1:0=01] and A12 = 0 during WRITE commands at T0 and T4

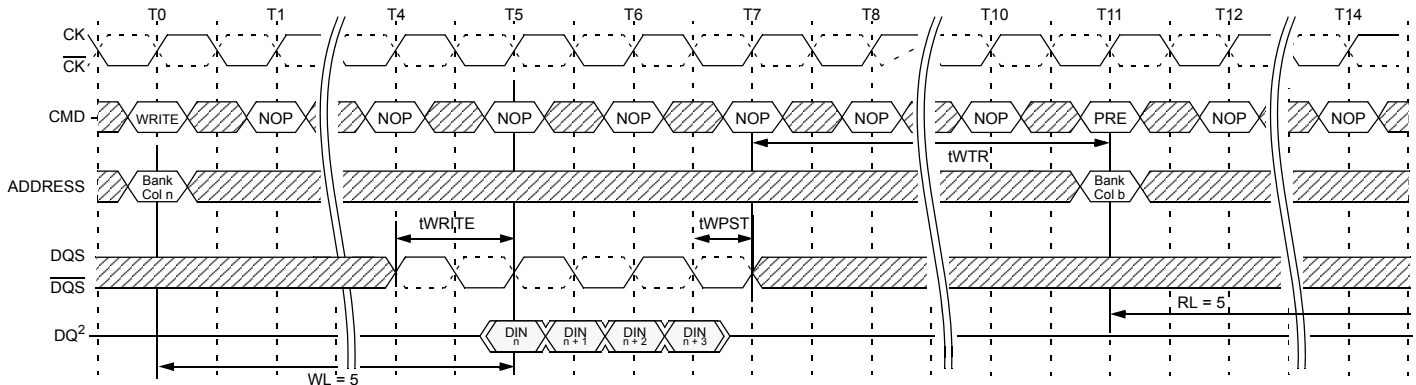
Figure 78. WRITE (BC4) to WRITE (BC4) OTF

**NOTE :**

1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. DIN n = data-in from column n; DOUT b = data-out from column b.
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0=01] and A12 = 1 during WRITE commands at T0.
READ command at T11 can be either BC4 or BL8 depending on MR0[A1 : 0] and A12 status at T13.

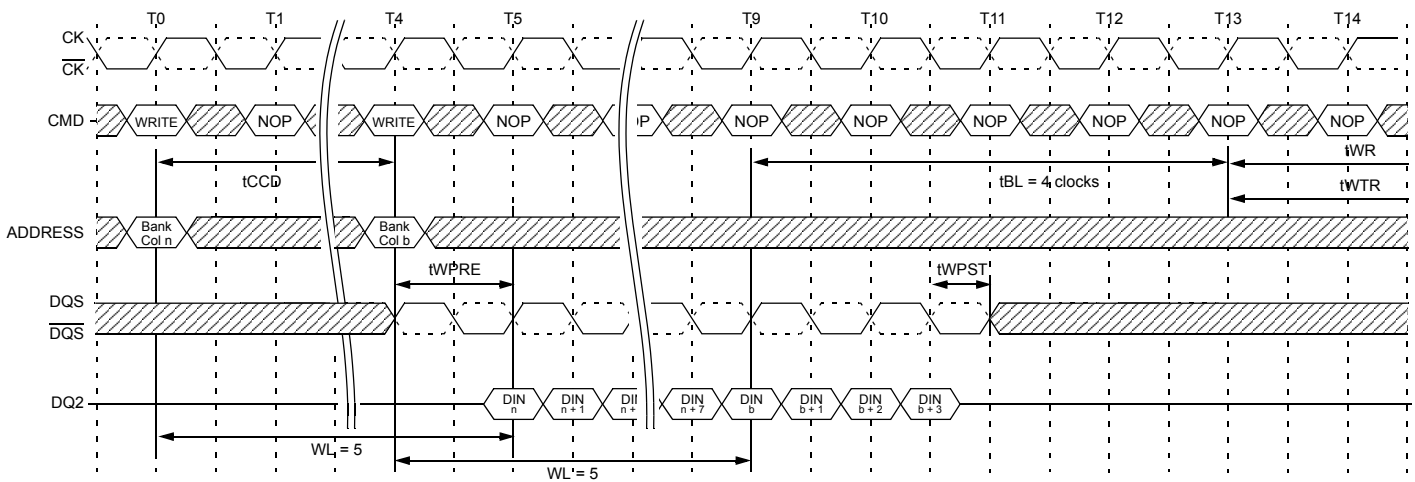
Figure 79. WRITE (BL8) to READ (BC4/BL8)OTF**NOTE :**

1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. DIN n = data-in from column n; DOUT b = data-out from column b.
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during WRITE command at T0.
READ command at T11 can be either BC4 or BL8 depending on A12 status at T13.

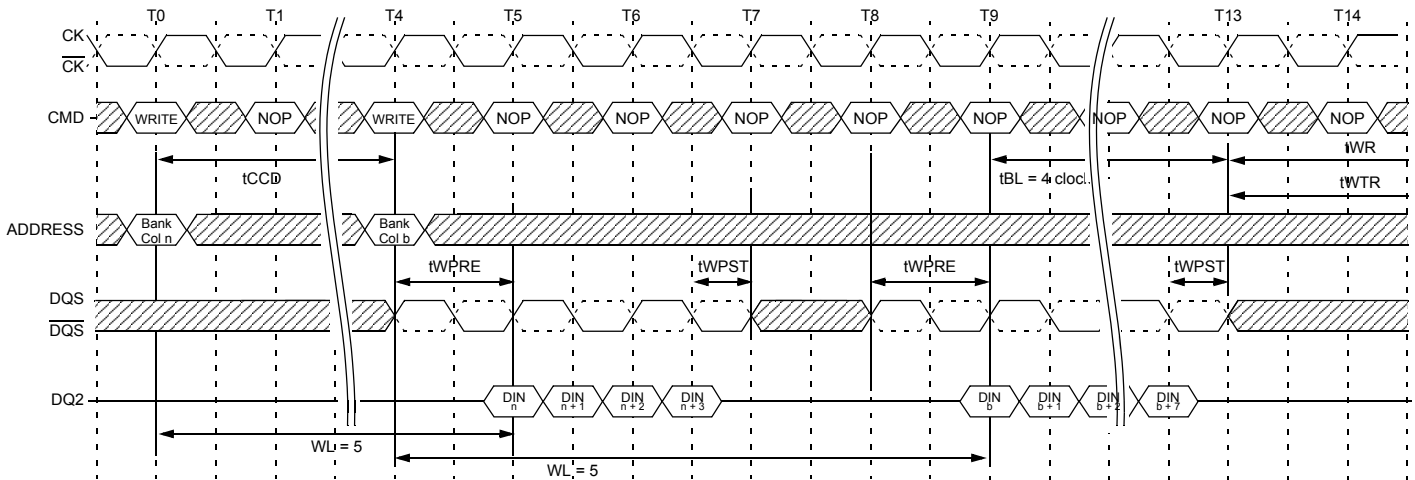
Figure 80. WRITE (BC4) to READ (BC4/BL8) OTF**NOTE :**

1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. DIN n = data-in from column n; DOUT b = data-out from column b.
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 10].

Figure 81. WRITE (BC4) to READ (BC4)

**NOTE :**

1. WL = 5 (CWL = 5, AL = 0)
2. DIN n (or b) = data-in from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0.
BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during WRITE command at T4.

Figure 82. WRITE (BL8) to WRITE (BC4) OTF**NOTE :**

1. WL = 5 (CWL = 5, AL = 0)
2. DIN n (or b) = data-in from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during WRITE command at T0.
BL8 setting activated by MR0[A1:0 = 01] and A12 = 1 during WRITE command at T4.

Figure 83. WRITE (BC4) to WRITE (BL8) OTF

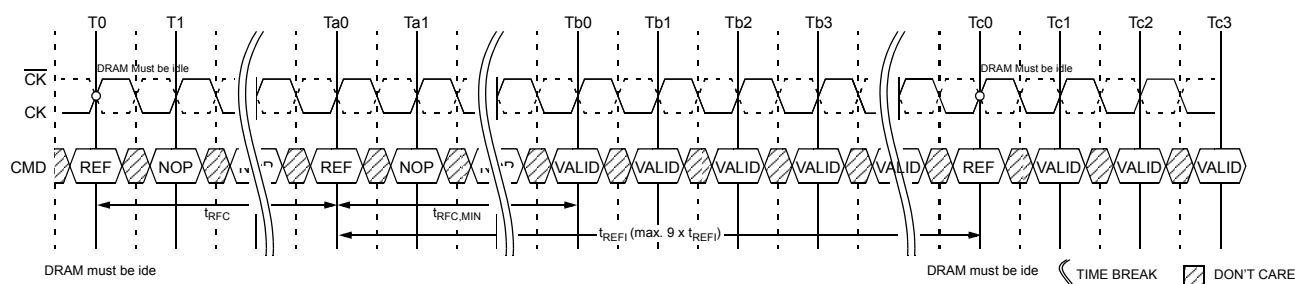
17.15 Refresh Command

The Refresh command (REF) is used during normal operation of the gDDR3 SDRAMs. This command is non persistent, so it must be issued each time a refresh is required. The gDDR3 SDRAM requires Refresh cycles at an average periodic interval of t_{REFI} . When $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ are held Low and $\overline{WE}$ High at the rising edge of the clock, the chip enters a Refresh cycle. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time $t_{RP(min)}$ before the Refresh Command can be applied.

The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during a Refresh command. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started.

When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Refresh Command and the next valid command, except NOP or DES, must be greater than or equal to the minimum Refresh cycle time $t_{RFC(min)}$. Note that the t_{RFC} timing parameter depends on memory density.

In general, a Refresh command needs to be issued to the gDDR3 SDRAM regularly every t_{REFI} interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 Refresh commands can be postponed during operation of the gDDR3 SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to $9 \times t_{REFI}$ (see Figure 85). A maximum of 8 additional Refresh commands can be issued in advance ("pulled in"), with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8 Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to $9 \times t_{REFI}$ (see Figure 86). At any given time, a maximum of 16 REF commands can be issued within $2 \times t_{REFI}$. Self-refresh Mode may be entered with a maximum of eight Refresh commands being postponed. After exiting Self-Refresh Mode with one or more Refresh commands postponed, additional Refresh commands may be postponed to the extent that the total number of postponed Refresh commands (before and after the Self-Refresh) will never exceed eight.



NOTE :

1. Only NOP/DES commands allowed after Refresh command registered until $t_{RFC, Min}$ expires.
2. Time interval between two Refresh commands may be extended to a maximum of $9 \times t_{REFI}$

Figure 84. Refresh Command Timing

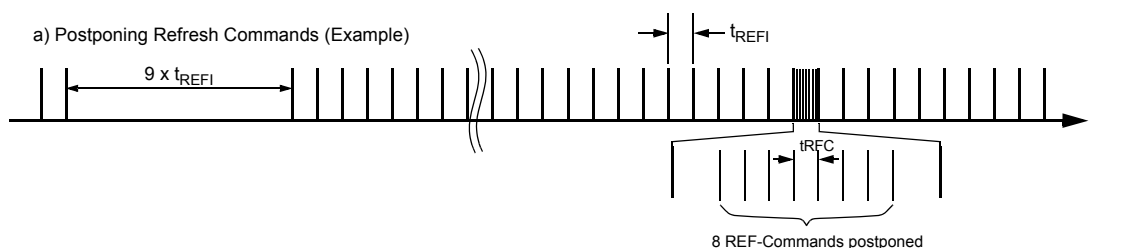


Figure 85. Postponing Refresh - Commands (Example)

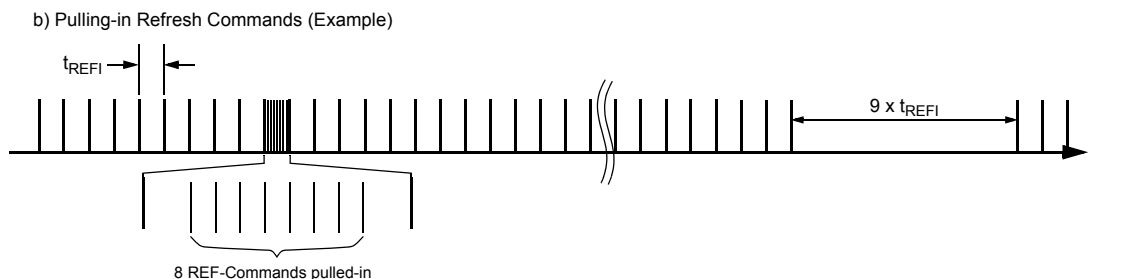


Figure 86. Pulling-in Refresh-Commands (Example)

17.16 Self-Refresh Operation

The Self-Refresh command can be used to retain data in the gDDR3 SDRAM, even if the rest of the system is powered down. When in the Self-Refresh mode, the gDDR3 SDRAM retains data without external clocking. The gDDR3 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh-Entry (SRE) Command is defined by having $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{CKE}}$ held low with $\overline{\text{WE}}$ high at the rising edge of the clock.

Before issuing the Self-Refresh-Entry command, the gDDR3 SDRAM must be idle with all bank precharge state with t_{RP} satisfied. Also, on-die termination must be turned off before issuing Self-Refresh-Entry command, by either registering ODT pin low "ODTL + 0.5tCK" prior to the Self-Refresh Entry command or using MRS to MR1 command. Once the Self-Refresh Entry command is registered, $\overline{\text{CKE}}$ must be held low to keep the device in Self-Refresh mode. During normal operation (DLL on), MR1(A0 = 0), the DLL is automatically disabled upon entering Self-Refresh and is automatically enabled (including a DLL-Reset) upon exiting Self-Refresh.

When the gDDR3 SDRAM has entered Self-Refresh mode, all of the external control signals, except $\overline{\text{CKE}}$ and $\overline{\text{RESET}}$, are "don't care". For proper Self-Refresh operation, all power supply and reference pins (VDD, VDDQ, VSS, VSSQ, VRefCA and VRefDQ) must be at valid levels. VrefDQ supply may be turned OFF in system during Self Refresh operation, provided that VrefDQ is valid and stable prior to $\overline{\text{CKE}}$ going back High and that first Write operation may not occur earlier than 512nCK after exit from Self Refresh.

The DRAM initiates a minimum of one Refresh command internally within tCKE period once it enters Self-Refresh mode.

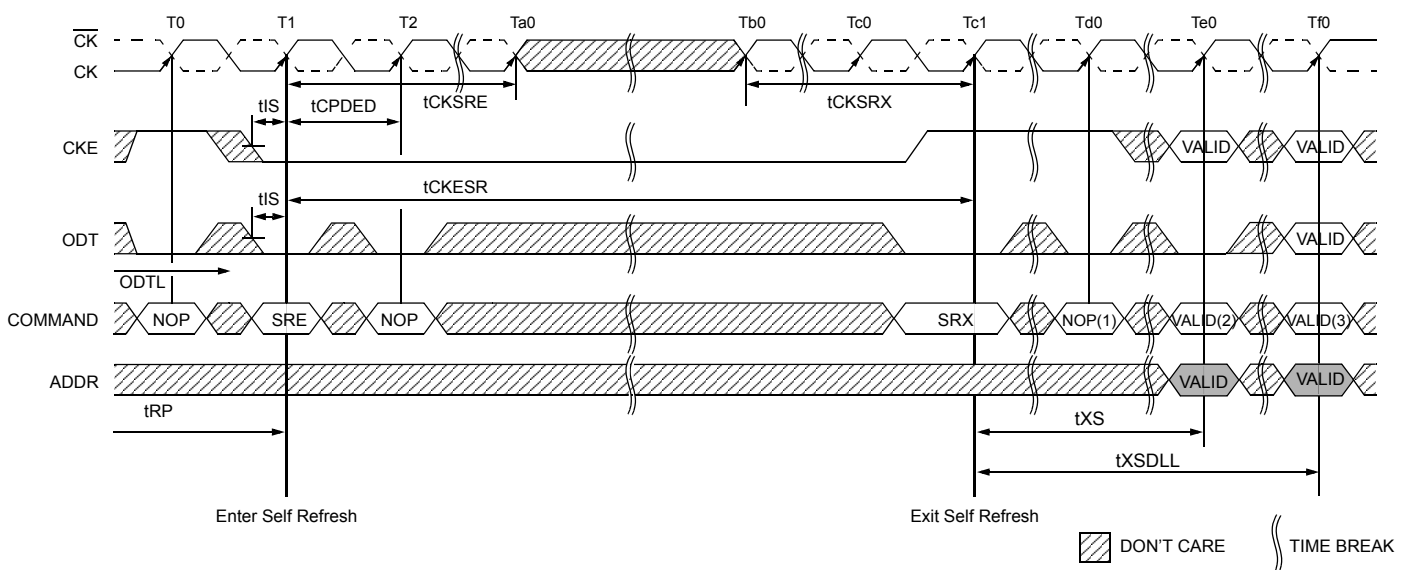
The clock is internally disabled during Self-Refresh Operation to save power. The minimum time that the gDDR3 SDRAM must remain in Self-Refresh mode is tCKE. The user may change the external clock frequency or halt the external clock tCKSRE after Self-Refresh entry is registered, however, the clock must be restarted and stable tCKSRX before the device can exit Self-Refresh operation.

The procedure for exiting Self-Refresh requires a sequence of events. First, the clock must be stable prior to $\overline{\text{CKE}}$ going back HIGH. Once a Self-Refresh Exit command (SRX, combination of $\overline{\text{CKE}}$ going high and either NOP or Deselect on command bus) is registered, a delay of at least tXS must be satisfied before a valid command not requiring a locked DLL can be issued to the device to allow for any internal refresh in progress. Before a command which requires a locked DLL can be applied, a delay of at least tXSDLL and applicable ZQCAL function requirements (TBD) must be satisfied.

Before a command that requires a locked DLL can be applied, a delay of at least tXSDLL must be satisfied. Depending on the system environment and the amount of time spent in Self-Refresh, ZQ calibration commands may be required to compensate for the voltage and temperature drift as described in "ZQ Calibration Commands" on page 119. To issue ZQ calibration commands, applicable timing requirements must be satisfied (See Figure 101, "ZQ Calibration Timing", on page 119)

$\overline{\text{CKE}}$ must remain HIGH for the entire Self-Refresh exit period tXSDLL for proper operation except for Self-Refresh re-entry. Upon exit from Self-Refresh, the gDDR3 SDRAM can be put back into Self-Refresh mode after waiting at least tXS period and issuing one refresh command (refresh period of tRFC). NOP or deselect commands must be registered on each positive clock edge during the Self-Refresh exit interval tXS. ODT must be turned off during tXS-DLL.

The use of Self-Refresh mode introduces the possibility that an internally timed refresh event can be missed when $\overline{\text{CKE}}$ is raised for exit from Self-Refresh mode. Upon exit from Self-Refresh, the gDDR3 SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode.



NOTE :

1. Only NOP or DES commands
2. Valid commands not requiring a locked DLL
3. Valid commands requiring a locked DLL

Figure 87. Self-Refresh Entry/Exit Timing

17.17 Power-Down Modes

17.17.1 Power-Down Entry and Exit

Power-down is synchronously entered when CKE is registered low (along with NOP or Deselect command). CKE is not allowed to go low while mode register set command, MPR operations, ZQCAL operations, DLL locking or read / write operation are in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or auto-precharge and refresh are in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in Figure 88 through Figure 100 with details for entry and exit of Power-Down.

The DLL should be in a locked state when power-down is entered for fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper read operation and synchronous ODT operation. DRAM design provides all AC and DC timing and voltage specification as well proper DLL operation with any CKE intensive operations as long as DRAM controller complies with DRAM specifications.

During Power-Down, if all banks are closed after any in progress commands are completed, the device will be in precharge Power-Down mode; if any bank is open after in progress commands are completed, the device will be in active Power-Down mode.

Entering power-down deactivates the input and output buffers, excluding CK, $\overline{\text{CK}}$, ODT, CKE and $\overline{\text{RESET}}$. To protect DRAM internal delay on CKE line to block the input signals, multiple NOP or Deselect commands are needed during the CKE switch off and cycle(s) after, this timing period are defined as tCPDED. CKE_low will result in deactivation of command and address receivers after tCPDED has expired.

[Table 74] Power-Down Entry Definitions

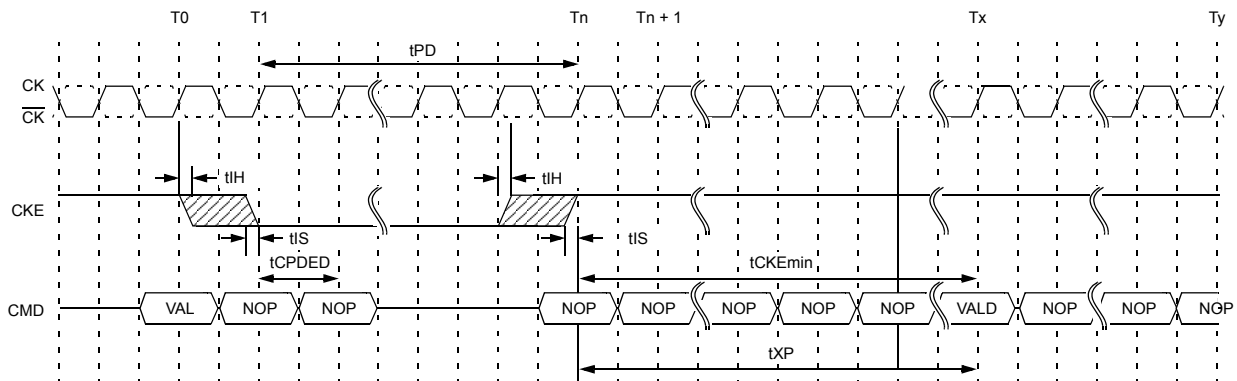
Status of DRAM	MRS bit A12	DLL	PD Exit	Relevant Parameters
Active (A bank or more Open)	Don't Care	On	Fast	tXP to any valid command
Pre Charged (All banks Precharged)	0	Off	Slow	tXP to any valid command. Since it is in precharge state, commands here will be ACT, AR, MRS/EMRS, PR or PRA tXPDLL to commands who need DLL to operate, such as RD, RDA or ODT control line.
Pre Charged (All Banks Precharged)	1	On	Fast	tXP to any valid command

Also, the DLL is disabled upon entering precharge power-down (Slow Exit Mode), but the DLL is kept enabled during precharge power-down (Fast Exit Mode) or active power-down. In power-down mode, CKE low, $\overline{\text{RESET}}$ high and a stable clock signal must be maintained at the inputs of the gDDR3 SDRAM, and ODT should be in a valid state but all other input signals are "Don't Care" (If $\overline{\text{RESET}}$ goes low during Power-Down, the DRAM will be out of PD mode and into reset state.) CKE low must be maintained until tCKE has been satisfied. Power-down duration is limited by 9 times tREFI of the device.

The power-down state is synchronously exited when CKE is registered high (along with a NOP or Deselect command).

CKE high must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP and/or tXP-DLL after CKE goes high. Power-down exit latency is defined at AC spec table of component data sheet.

Active Power Down Entry and Exit timing diagram example is shown in Figure 88. Timing Diagrams for CKE with PD Entry, PD Exit with Read and Read with Auto Precharge, Write, Write with Auto Precharge, Activate, Precharge, Refresh, and MRS are shown in Figure 89 through Figure 97. Additional clarifications are shown in Figure 98 through Figure 100.



NOTE : VAL command at T0 is ACT, NOP, DES or Precharge with still one bank remaining open after completion of precharge command.

Figure 88. Active Power-Down Entry and Exit Timing Diagram

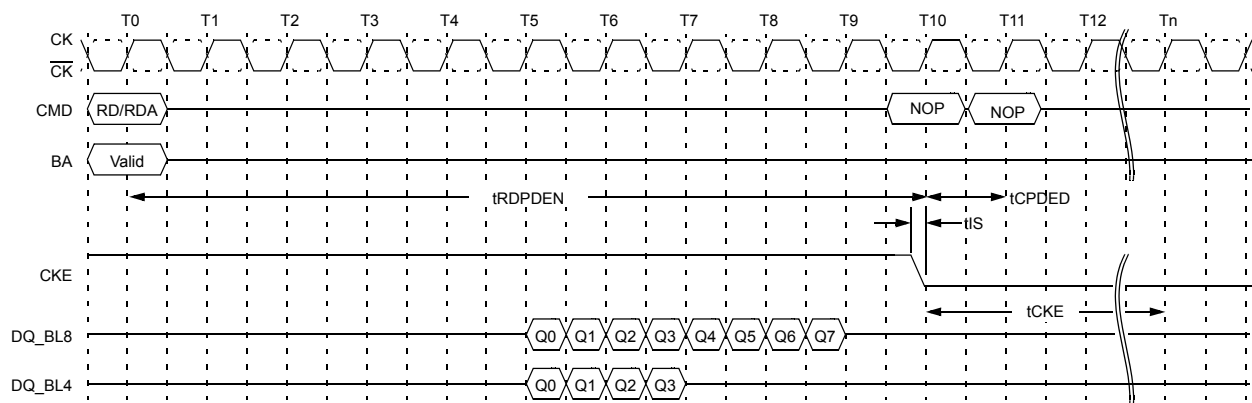


Figure 89. Power-Down Entry after Read and Read with Auto Precharge

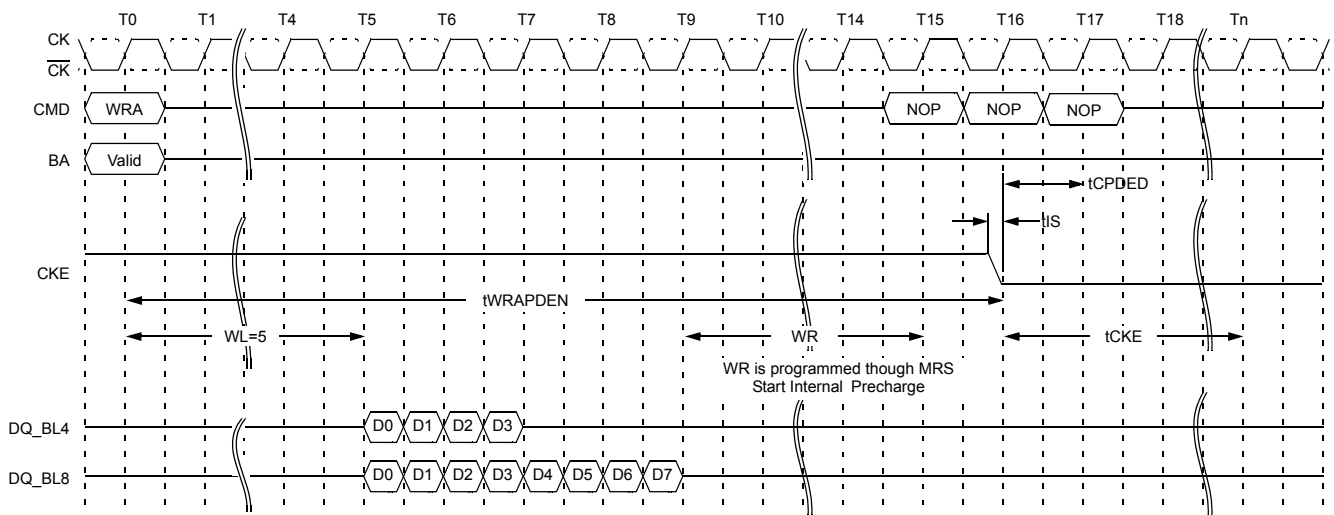


Figure 90. Power-Down Entry After Write with Auto Precharge

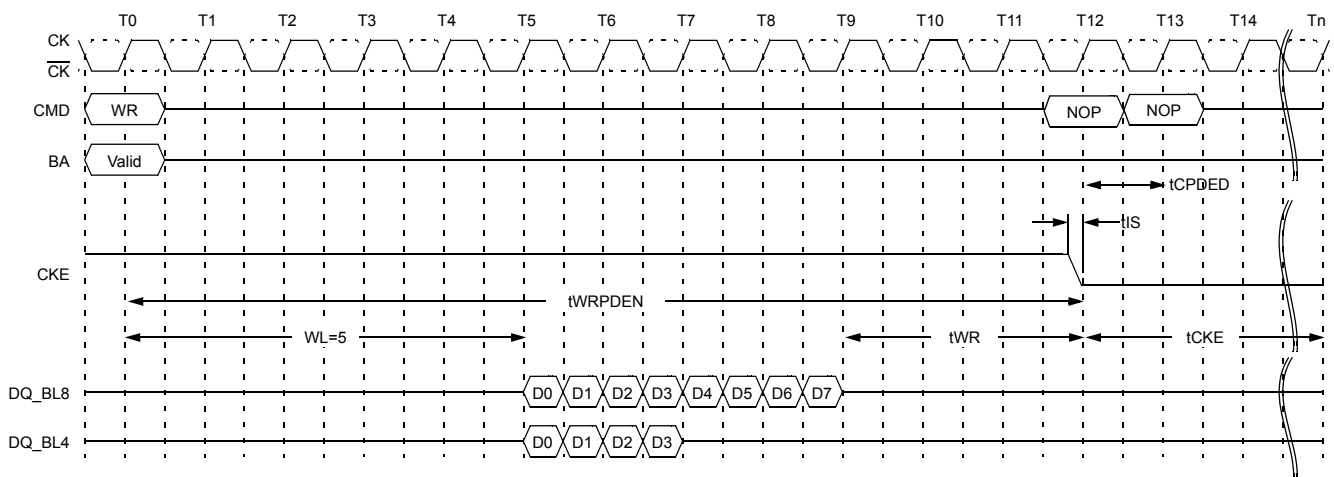


Figure 91. Power-Down Entry after Write

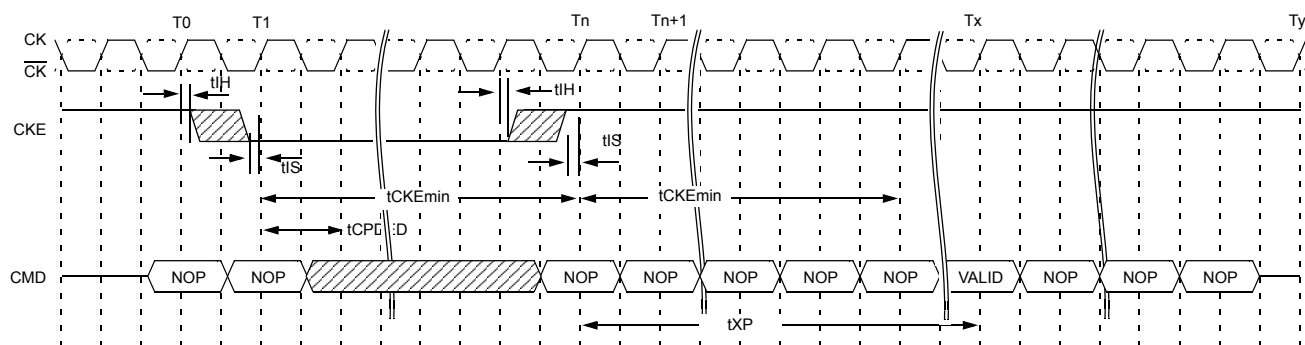


Figure 92. Precharge Power-Down (Fast Exit Mode) Entry and Exit

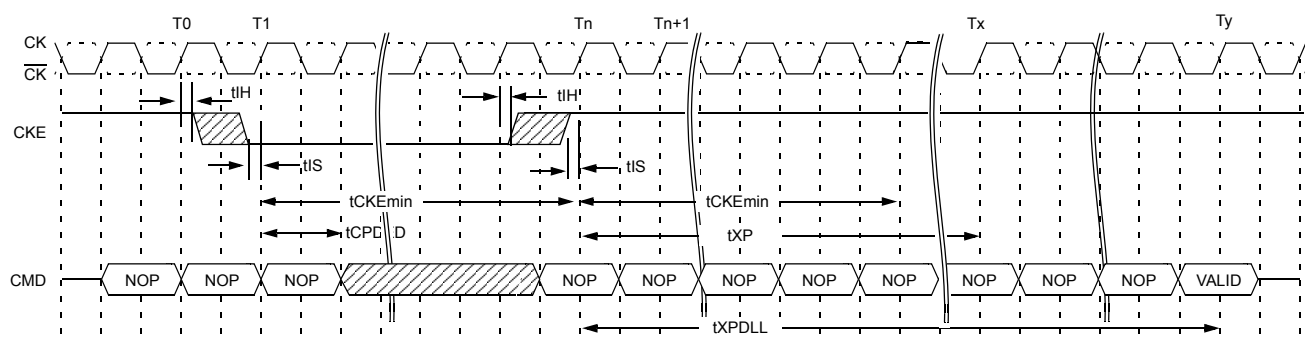


Figure 93. Precharge Power-Down (Slow Exit Mode) Entry and Exit

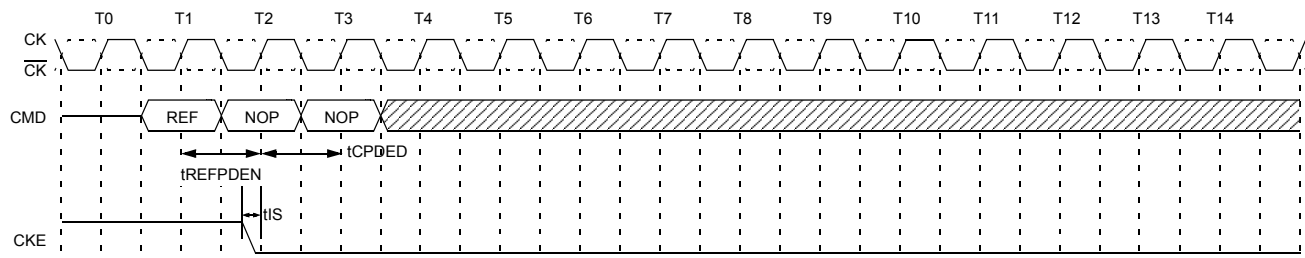


Figure 94. Refresh Command to Power-Down Entry

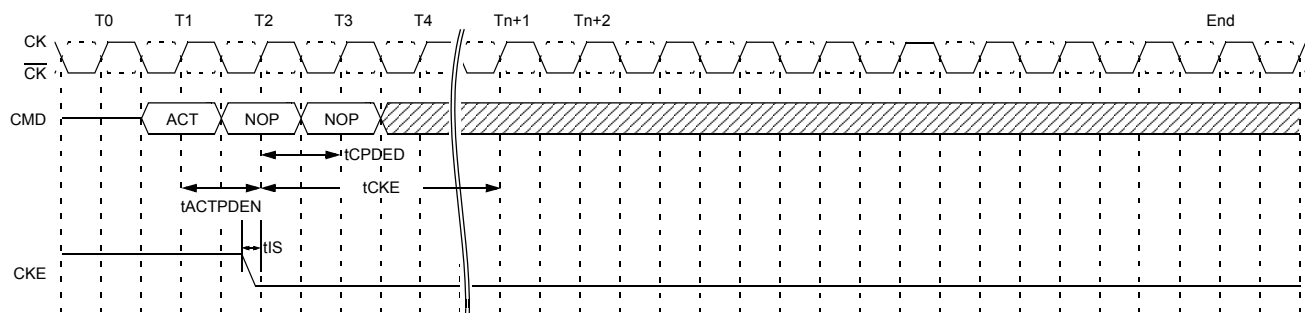


Figure 95. Active Command to Power-Down Entry

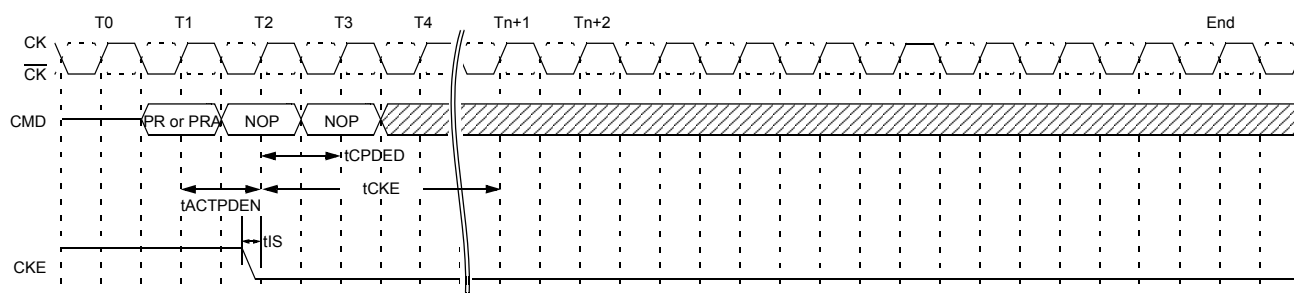


Figure 96. Precharge/Precharge all Command to Power-Down Entry

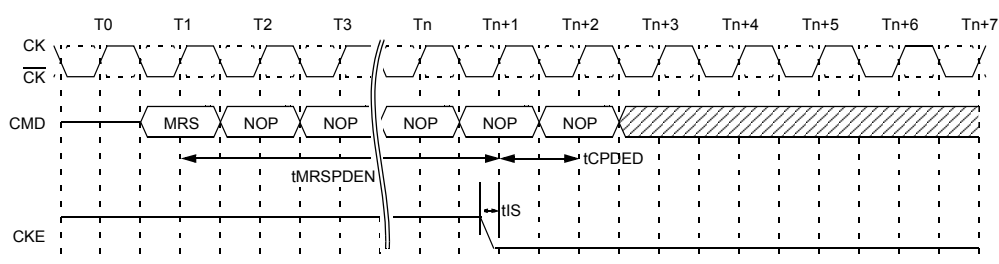
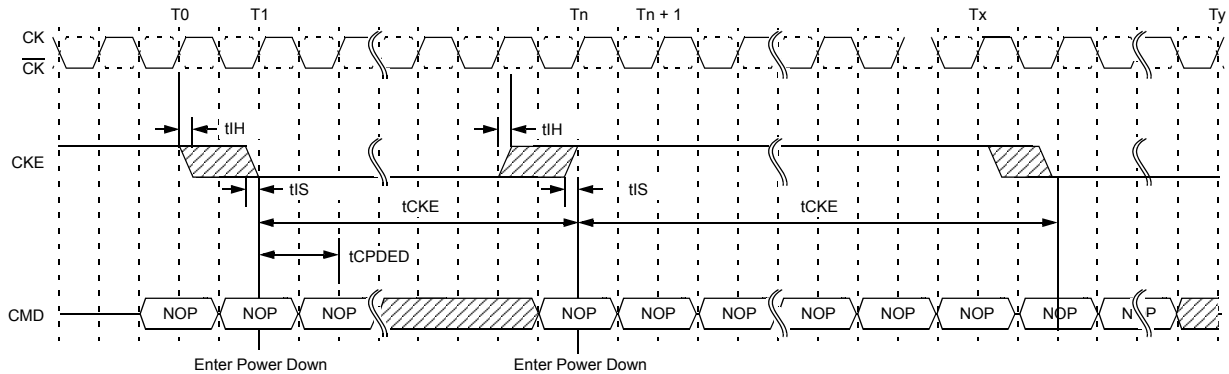


Figure 97. MRS Command to Power-Down Entry

17.17.2 Power-Down clarifications - Case 1

When CKE is registered low for power-down entry, $t_{PD(min)}$ must be satisfied before CKE can be registered high for power-down exit. The minimum value of parameter $t_{PD(min)}$ is equal to the minimum value



CASE 1 :

When CKE registered low for PD Entry, t_{CKE} must be satisfied before CKE can be registered high as PD Exit

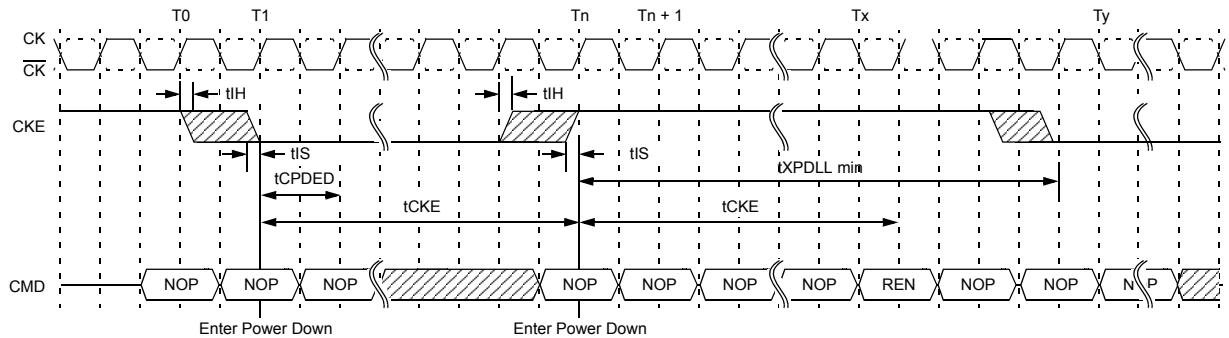
CASE 1a :

After PD Exit, t_{CKE} must be satisfied before CKE can be registered low again.

Figure 98. Power-Down Entry/Exit Clarifications - Case1

17.17.3 Power-Down clarifications - Case 2

For certain CKE intensive operations, for example, repeated 'PD Exit - Refresh - PD Entry' sequence, the number of clock cycles between PD Exit and PD Entry may be insufficient to keep the DLL updated. Therefore the following conditions must be met in addition to t_{CKE} in order to maintain proper DRAM operation when the Refresh command is issued between PD Exit and PD Entry. Power-down mode can be used in conjunction with the Refresh command if the following conditions are met: 1) t_{XP} must be satisfied before issuing the command. 2) t_{XPDLL} must be satisfied (referenced to the registration of PD Exit) before the next power-down can be entered. A detailed example of Case 2 is shown in Figure 99.



CASE 2 :

For certain CKE intensive operations, for example, repeated "PD Exit - Refresh - PD Entry" sequence, the number of clock cycles between PD Exit and PD Entry may be insufficient to keep the DLL updated. Therefore the following conditions must be met in addition to t_{CKE} in order to maintain proper DRAM operation when Refresh command is issued in between PD Exit and PD Entry.

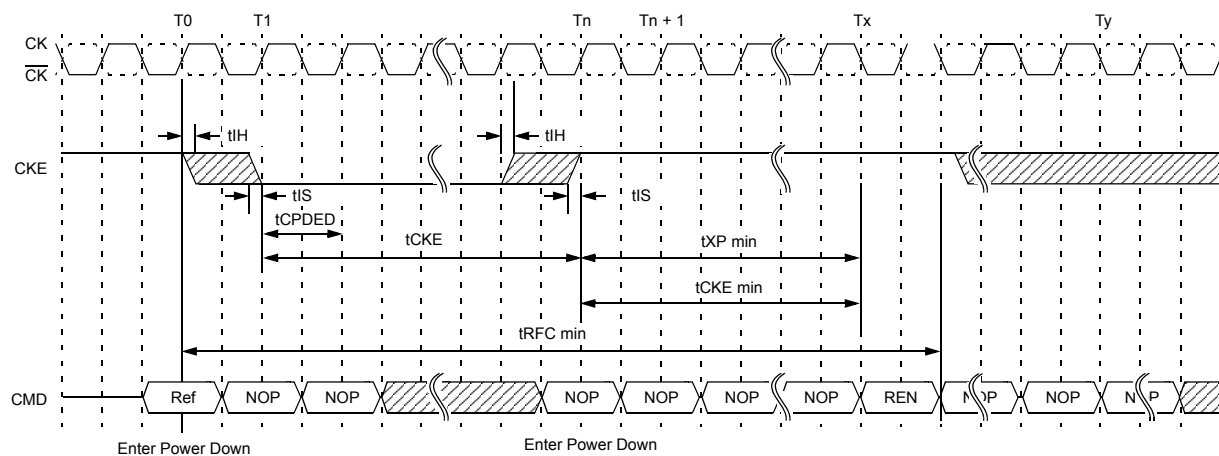
Power down mode can be used in conjunction with Refresh command if the following conditions are met:

1. t_{XP} must be satisfied before issuing the command
2. t_{XPDLL} must be satisfied (referenced to registration of PD exit) before next power down can be entered.

Figure 99. Power-Down Entry/Exit Clarifications - Case2

17.17.4 Power-Down clarifications - Case 3

If an early PD Entry is issued after a Refresh command, once PD Exit is issued, NOP or DES with CKE High must be issued until $t_{RFC}(\min)$ from the Refresh command is satisfied. This means CKE can not be registered low twice within a $t_{RFC}(\min)$ window. A detailed example of Case 3 is shown in Figure 100.

**CASE 3 :**

If an early PD Entry is issued after Refresh command, once PD Exit is issued, NOP or DES with CKE High must be issued until t_{RFC} from the Refresh command is satisfied. This means CKE can not be registered low twice within t_{RFC} window.

Figure 100. Power-Down Entry/Exit Clarifications - Case3

17.18 ZQ Calibration Commands

17.18.1 Calibration Description

ZQ Calibration command is used to calibrate DRAM Ron & ODT values over PVT. gDDR3 SDRAM needs longer time to calibrate Ron & ODT at initialization and relatively smaller time to perform periodic calibrations.

ZQCL command is used to perform the initial calibration during power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. ZQCL command triggers the calibration engine inside the DRAM and once calibration is achieved the calibrated values are transferred from calibration engine to DRAM IO which gets reflected as updated Output Driver and ODT values.

The first ZQCL command issued after reset is allowed a timing period of tZQinit to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after RESET is allowed a timing period of tZQoper.

ZQCS command is used to perform periodic calibrations to account for VT variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter tZQCS. One ZQCS command can effectively correct a minimum of 0.5 % (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdfriftrate) and voltage (Vdfriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{TSens} \times \text{Tdfriftrate}) + (\text{VSens} \times \text{Vdfriftrate})}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5% / °C, VSens = 0.15% / mV, Tdfriftrate = 1 °C / sec and Vdfriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128\text{ms}$$

No other activities should be performed on the DRAM channel by the controller for the duration of tZQinit, tZQoper or tZQCS. The quiet time on the DRAM channel helps in accurate calibration of Ron and ODT. Once DRAM calibration is achieved, the DRAM should disable ZQ current consumption path to reduce power.

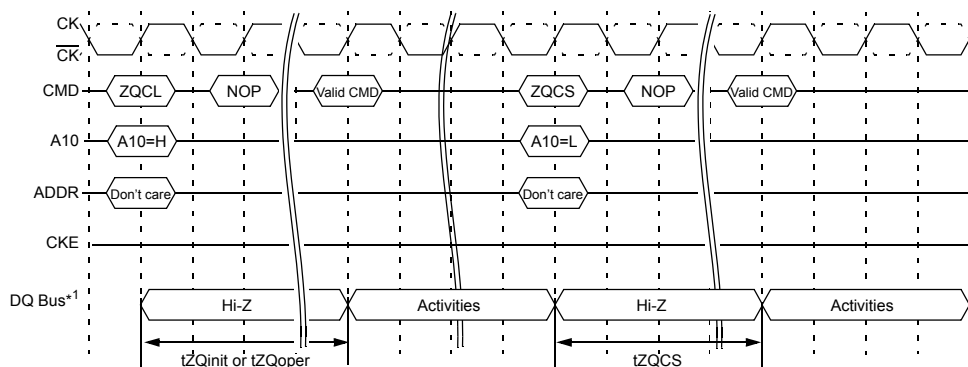
All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller.

See "[BA=Bank Address, RA=Row Address, CA=Column Address, BC#=Burst Chop, X=Don't Care, V=Valid]" on page 78 for a description of the ZQCL and ZQCS commands.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self refresh. Upon Self-Refresh exit, gDDR3 SDRAM will not perform an IO calibration without an explicit ZQ calibration command. The earliest possible time for ZQ Calibration command (short or long) after self refresh exit is tXS.

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of tZQoper or tZQinit or tZQCS between the devices.

17.18.2 ZQ Calibration Timing



NOTE : ODT must be disabled during calibration procedure

*1: All devices connected to DQ bus should be high impedance during calibration

Figure 101. ZQ Calibration Timing

17.18.3 ZQ External Resistor Value and Tolerance and Capacitive loading

In order to use the ZQ Calibration function, a 240 ohm +/- 1% tolerance external resistor must be connected between the ZQ pin and ground. The single resistor can be used for each SDRAM or one resistor can be shared between two SDRAMs if the ZQ calibration timings for each SDRAM do not overlap. The total capacitive loading on the ZQ pin must be limited. (See "Input/Output Capacitance" on component datasheet)

18. On-Die Termination (ODT)

ODT (On-Die Termination) is a feature of the gDDR3 SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS, $\overline{\text{DQS}}$ and DM for x4 and x8 configuration (and TDQS, $\overline{\text{TDQS}}$ for X8 configuration, when enabled via A11=1 in MR1) via the ODT control pin. For x16 configuration, ODT is applied to each DQU, DQL, DQSU, $\overline{\text{DQSU}}$, DQSL, $\overline{\text{DQSL}}$, DMU and DML signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices. More details about ODT control modes and ODT timing modes can be found further down in this document :

- The ODT control modes are described in 3.1.
- The ODT synchronous mode is described in 3.2
- The dynamic ODT feature is described in 3.3
- The ODT asynchronous mode is described in 3.4
- The transitions between ODT synchronous and asynchronous are described in 3.4.1 through 3.4.4

The ODT feature is turned off and not supported in Self-Refresh mode.

A simple functional representation of the DRAM ODT feature is shown in Figure 102.

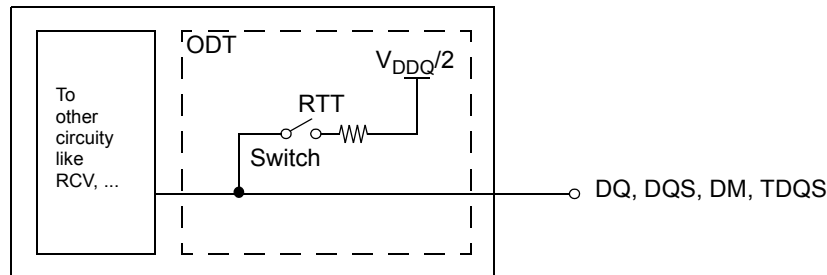


Figure 102. Functional Representation of ODT

The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other control information, see below. The value of RTT is determined by the settings of Mode Register bits (see Figure 35 on page 73 and Figure 36 on page 76). The ODT pin will be ignored if the Mode Registers MR1 and MR2 are programmed to disable ODT and in self-refresh mode.

18.1 ODT Mode Register and ODT Truth Table

The ODT Mode is enabled if either of MR1 bits A2 or A6 or A9 are non zero. In this case, the value of RTT is determined by the settings of those bits (see Figure 35 on page 73).

Application: Controller sends WR command together with ODT asserted.

- One possible application: The rank that is being written to provides termination.
- DRAM turns ON termination if it sees ODT asserted (except ODT is disabled by MR).
- DRAM does not use any write or read command decode information.
- The Termination Truth Table is shown in Table 75.

[Table 75] Termination Truth Table

ODT pin	DRAM Termination State
0	OFF
1	ON, (OFF, if disabled by MR1 {A9, A6, A2} and MR2 {A10, A9} in general)

18.2 Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the power-down definition, these modes are:

- Any bank active with CKE high
- Refresh with CKE high
- Idle mode with CKE high
- Active power down mode (regardless of MR0 bit A12)
- Precharge power down mode if DLL is enabled during precharge power down by MR0 bit A12.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

In synchronous ODT mode, RTT will be turned on ODTLon clock cycles after ODT is sampled high by a rising clock edge and turned off ODTLoff clock cycles after ODT is registered low by a rising clock edge. The ODT latency is tied to the write latency (WL) by: $ODTLon = WL - 2$; $ODTLoff = WL - 2$.

18.2.1 ODT Latency and Posted ODT

In Synchronous ODT Mode, the Additive Latency (AL) programmed into the Mode Register (MR1) also applies to the ODT signal. The DRAM internal ODT signal is delayed for a number of clock cycles defined by the Additive Latency (AL) relative to the external ODT signal. $ODTLon = CWL + AL - 2$; $ODTLoff = CWL + AL - 2$. For details, refer to gDDR3 SDRAM latency definitions.

[Table 76] ODT Latency

Symbol	Parameter	gDDR-1066	gDDR3-1333	gDDR3-1600	gDDR3-1866	gDDR3-2133	gDDR3-2400	Unit
ODTLon	ODT turn on Latency	WL - 2.0 = CWL + AL - 2.0						tCK
ODTLoff	ODT turn on Latency	WL - 2.0 = CWL + AL - 2.0						

18.2.2 Timing Parameters

In synchronous ODT mode, the following timing parameters apply (see Figure 103 on page 122):

ODTLon, ODTLoff, tAON,min,max, tAOF,min,max.

Minimum RTT turn-on time (tAONmin) is the point in time when the device leaves high impedance and ODT resistance begins to turn on. Maximum RTT turn on time (tAONmax) is the point in time when the ODT resistance is fully on. Both are measured from ODTLon.

Minimum RTT turn-off time (tAOFmin) is the point in time when the device starts to turn off the ODT resistance.

Maximum RTT turn off time (tAOFmax) is the point in time when the on-die termination has reached high impedance.

Both are measured from ODTLoff.

When ODT is asserted, it must remain high until ODT4 is satisfied. If a Write command is registered by the SDRAM with ODT high, then ODT must remain high until ODT4 (BL = 4) or ODT8 (BL = 8) after the Write command (see Figure 104 on page 122). ODT4 and ODT8 are measured from ODT registered high to ODT registered low or from the registration of a Write command until ODT is registered low.

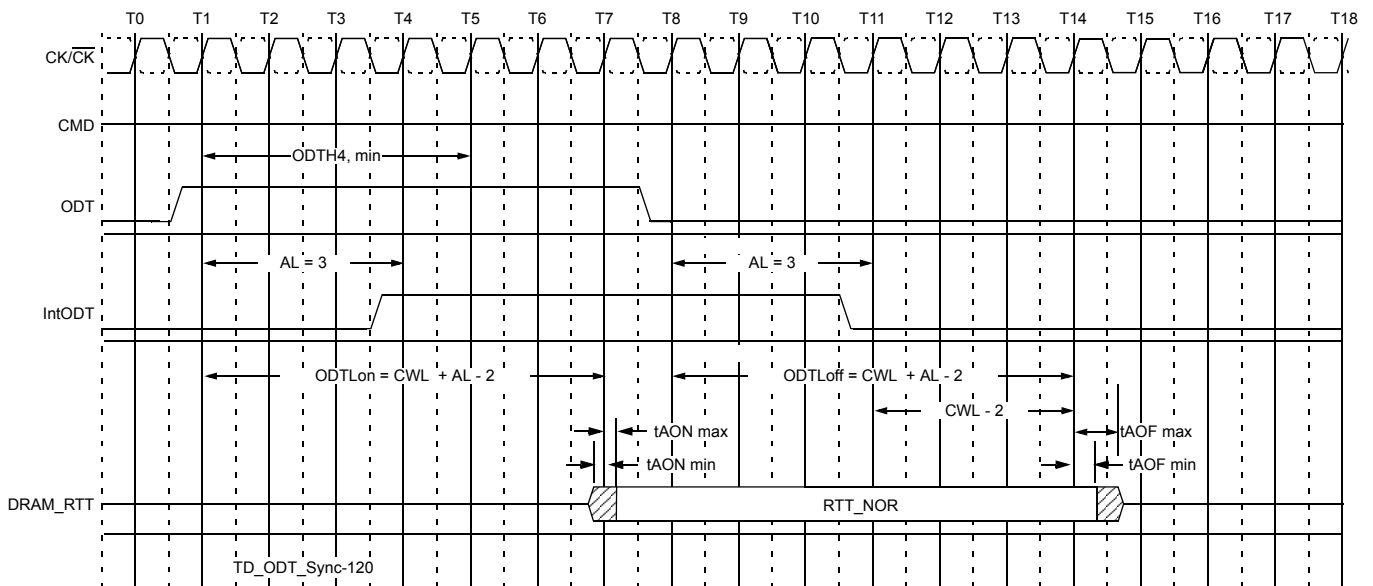


Figure 103. Synchronous ODT Timing Example for AL=3; CWL=5; ODTLon=AL+CWL-2=6.0; ODTLoff=AL+CWL-2=6

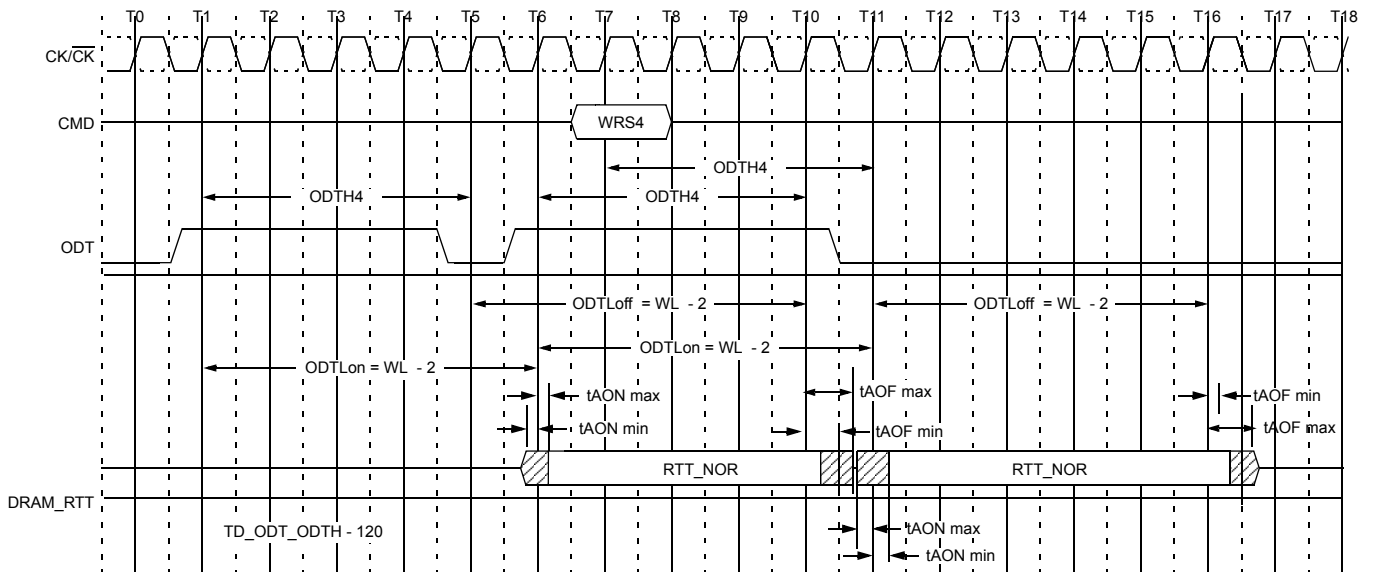


Figure 104. Synchronous ODT example with BL=4, WL=7

ODT must be held high for at least ODT_{H4} after assertion (T1); ODT must be kept high ODT_{H4} (BL = 4) or ODT_{H8} (BL = 8) after Write command (T7). ODT_H is measured from ODT first registered high to ODT first registered low, or from registration of Write command with ODT high to ODT registered low. Note that although ODT_{H4} is satisfied from ODT registered high at T6 ODT must not go low before T11 as ODT_{H4} must also be satisfied from the registration of the Write command at T7.

18.2.3 ODT during Reads:

As the gDDR3 SDRAM can not terminate and drive at the same time, RTT must be disabled at least half a clock cycle before the read preamble by driving the ODT pin low appropriately. RTT may nominally not be enabled until one clock cycle after the end of the post-amble as shown in the example below. As shown in Figure 105 below at cycle T15, DRAM turns on the termination when it stops driving which is determined by t_{HZ}. If DRAM stops driving early (i.e t_{HZ} is early) than t_{AONmin} timing may apply. If DRAM stops driving late (i.e t_{HZ} is late) than DRAM complies with t_{AONmax} timing. Note that ODT may be disabled earlier before the Read and enabled later after the Read than shown in this example in Figure 105.

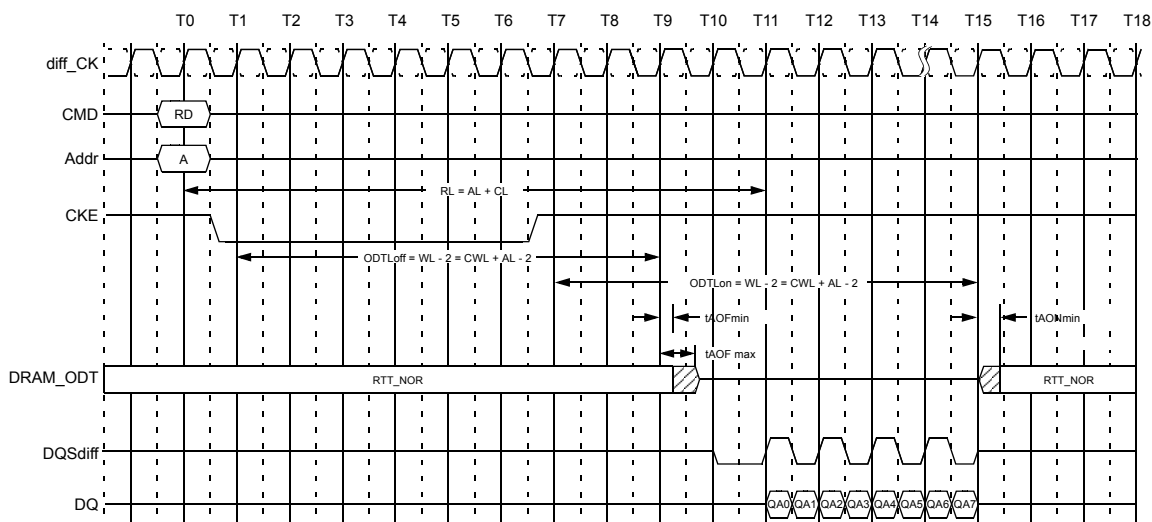


Figure 105. ODT must be disabled externally during Reads by driving ODT low.
(example: CL=6; AL=CL-1=5; RL=AL+CL=11; CWL=5; ODTLon=CWL+AL-2=8; ODTLoff=CWL+AL-2=8)

18.3 Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the gDDR3 SDRAM can be changed without issuing an MRS command. This requirement is supported by the "Dynamic ODT" feature as described as follows:

18.3.1 Functional Description:

The Dynamic ODT Mode is enabled if bit (A9) or (A10) of MR2 is set to '1'. The function is described as follows:

- Two RTT values are available: RTT_Nom and RTT_WR.
 - The value for RTT_Nom is preselected via bits A[9,6,2] in MR1
 - The value for RTT_WR is preselected via bits A[10,9] in MR2
- During operation without commands, the termination is controlled as follows;
 - Nominal termination strength RTT_Nom is selected.
 - Termination on/off timing is controlled via ODT pin and latencies ODTLon and ODTLoff.
- When a write command (WR, WRA, WRS4, WRS8, WRAS4, WRAS8) is registered, and if Dynamic ODT is enabled, the termination is controlled as follows:
 - A latency ODTLcnw after the write command, termination strength RTT_WR is selected.
 - A latency ODTLcwn8 (for BL8, fixed by MRS or selected OTF) or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) after the write command, termination strength RTT_Nom is selected.
 - Termination on/off timing is controlled via ODT pin and ODTLon, ODTLoff.

Table 77 shows latencies and timing parameters which are relevant for the on-die termination control in Dynamic ODT mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2{A10,A9}={0,0}, to disable Dynamic ODT externally.

When ODT is asserted, it must remain high until ODT_H4 is satisfied. If a Write command is registered by the SDRAM with ODT high, then ODT must remain high until ODT_H4 (BL = 4) or ODT_H8 (BL = 8) after the Write command (see Figure 104) ODT_H4 and ODT_H8 are measured from ODT registered high to ODT registered low or from the registration of a Write command until ODT is registered low.

[Table 77] Latencies and timing parameters relevant for Dynamic ODT

Name and Description	Abbr.	Defined from	Define to	Definition for all gDDR3 speed bins	Unit
ODT turn-on Latency	ODTLon	registering external ODT signal high	turning termination on	ODTLon = WL - 2	tCK
ODT turn-off Latency	ODTLoff	registering external ODT signal low	turning termination off	ODTLoff = WL - 2	tCK
ODT Latency for changing from RTT_Nom to RTT_WR	ODTLcnw	registering external write command	change RTT strength from RTT_Nom to RTT_WR	ODTLcnw = WL - 2	tCK
ODT Latency for change from RTT_WR to RTT_Nom (BL = 4)	ODTLcwn4	registering external write command	change RTT strength from RTT_WR to RTT_Nom	ODTLcwn4 = 4 + ODTLoff	tCK
ODT Latency for change from RTT_WR to RTT_Nom (BL = 8)	ODTLcwn8	registering external write command	change RTT strength from RTT_WR to RTT_Nom	ODTLcwn8 = 6 + ODTLoff	tCK(avg)
minimum ODT hold time after ODT assertion	ODTH4	registering ODT high	ODT registered low	ODTH4 = 4	tCK(avg)
minimum ODT hold time after Write (BL = 4)	ODTH4	registering Write with ODT high	ODT registered low	ODTH4 = 4	tCK(avg)
minimum ODT hold time after Write (BL = 8)	ODTH8	registering Write with ODT high	ODT registered low	ODTH8 = 6	tCK(avg)
RTT change skew	tADC	ODTLcnw ODTLcwn	RTT valid	tADC(min) = 0.3 * tCK(avg) tADC(max) = 0.7 * tCK(avg)	tCK(avg)

NOTE : tAOF,nom and tADC,nom are 0.5 tCK (effectively adding half a clock cycle to ODTLoff, ODTcnw and ODTLcwn)

18.3.2 ODT Timing Diagrams

The following pages provide exemplary timing diagrams as described in Table 78:

[Table 78] Timing Diagrams for "Dynamic ODT"

Figure	Description
Figure 106	Dynamic ODT: Behavior with ODT being asserted before and after the write.
Figure 107	Dynamic ODT: Behavior without write command, AL = 0, CWL = 5.
Figure 108	Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles.
Figure 109	Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles, example for BC4 (via MRS or OTF), AL = 0, CWL = 5.
Figure 110	Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 4 clock cycles.

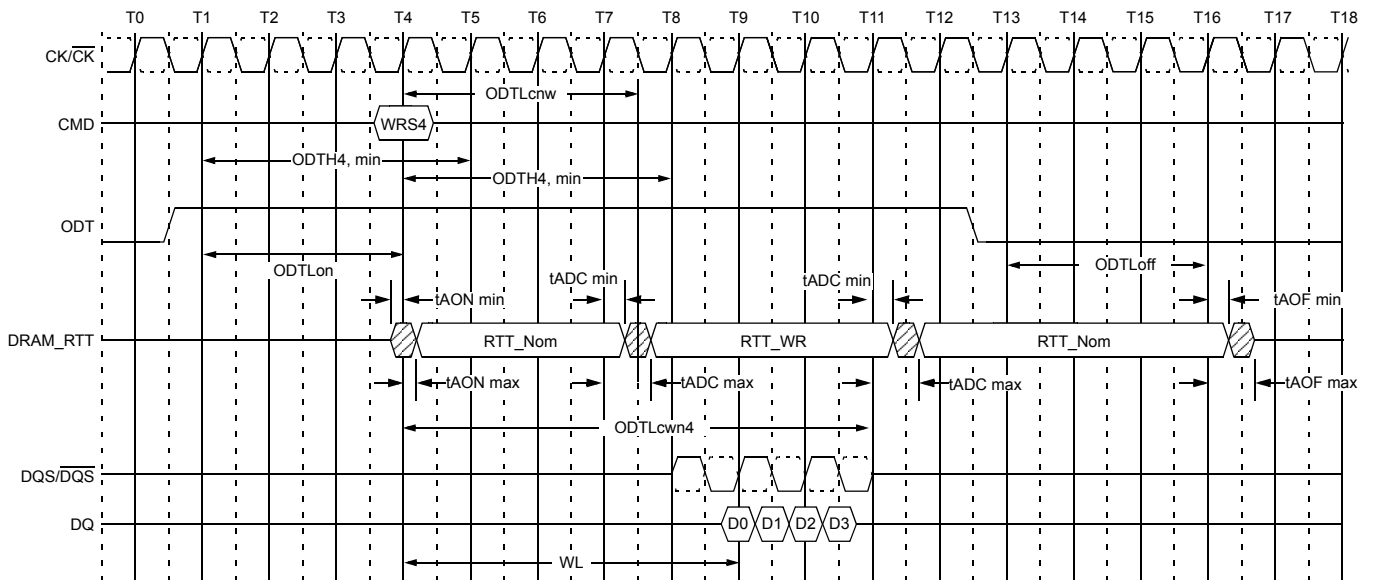


Figure 106. Dynamic ODT : Behavior with ODT being asserted before and after the write, example for BC4(via MRS or OTF), AL=0, CWL=5

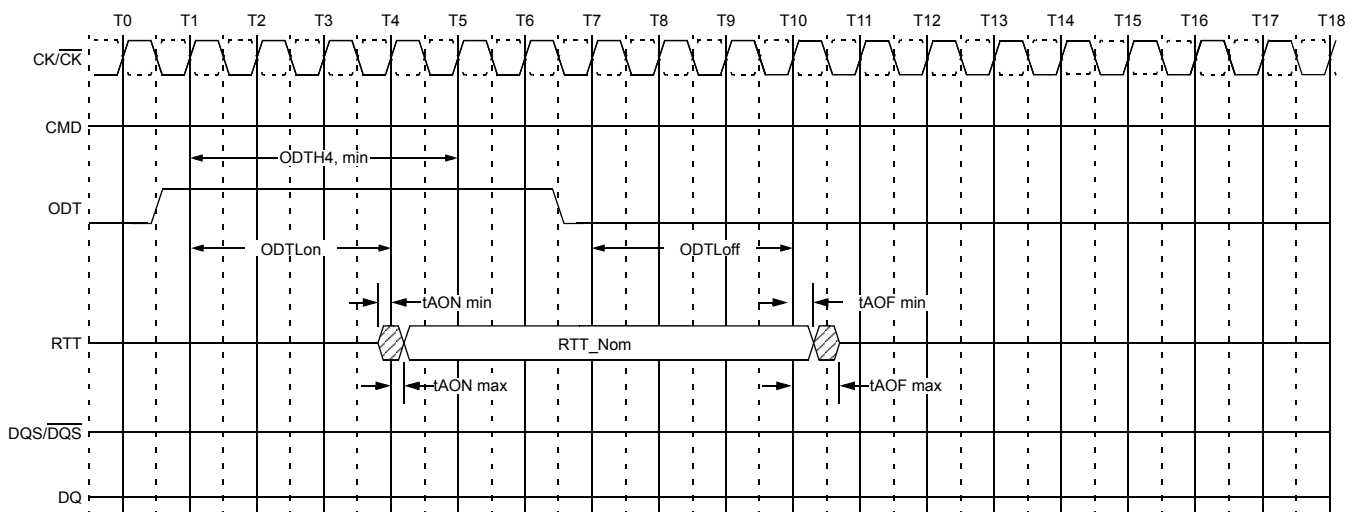


Figure 107. Dynamic ODT : Behavior without write command, AL=0, CWL=5

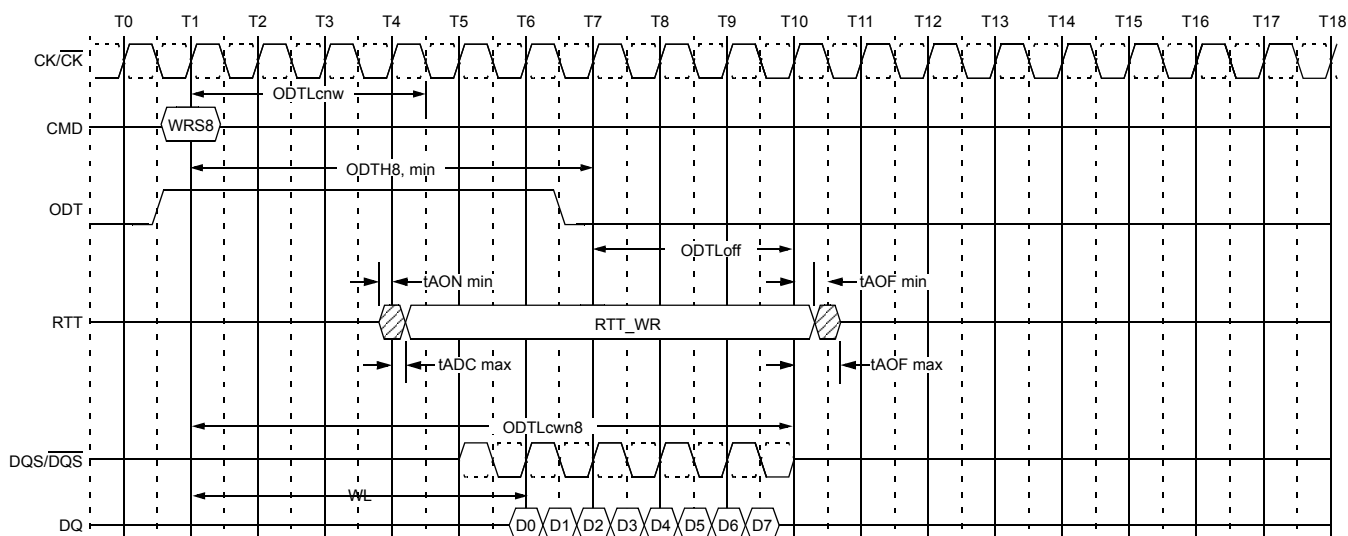


Figure 108. Dynamic ODT : Behavior with ODT pin being asserted together with write command for a duration of 6clock cycles, example for BL8 (via MRS or OTF). AL=0, CWL=5

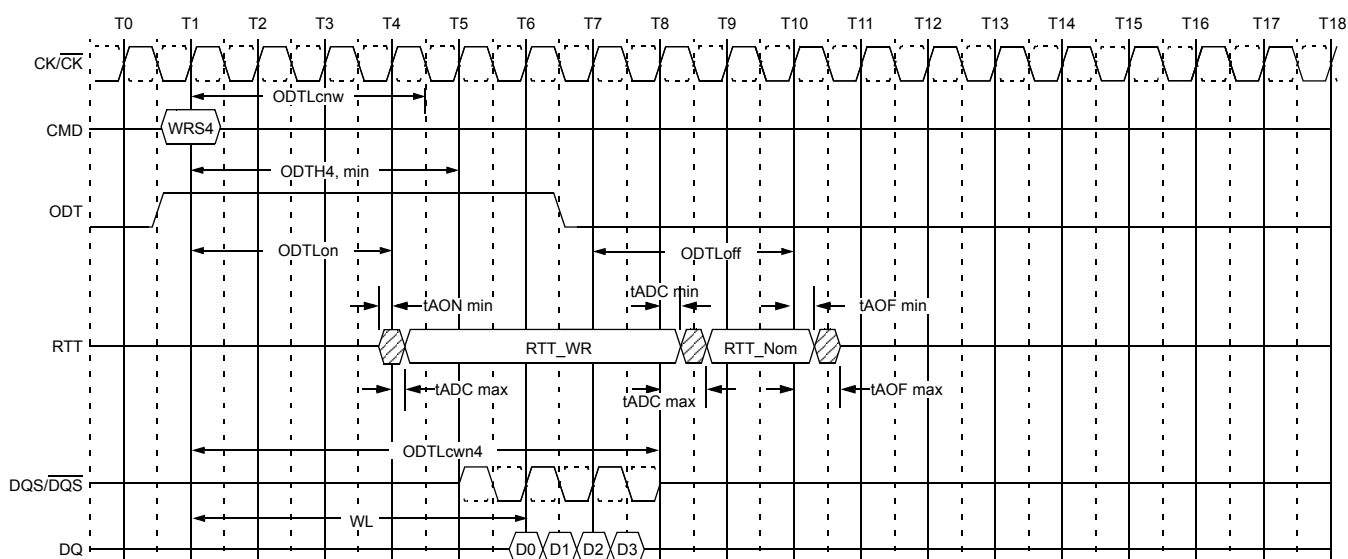


Figure 109. Dynamic ODT : Behavior with ODT pin being asserted together with write command for a duration of 6clock cycles, example for BC4 (via MRS or OTF), AL=0, CWL=5

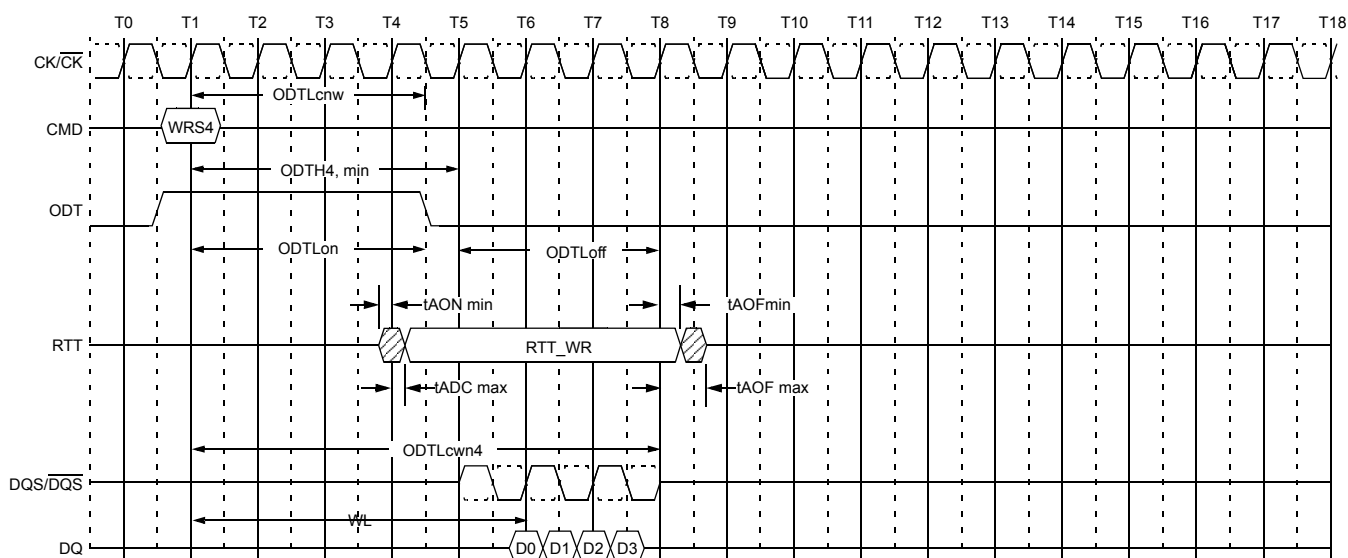


Figure 110. Dynamic ODT : Behavior with ODT pin being asserted together with write command for a duration of 4clock cycles, example for BC4 (via MRS or OTF), AL=0, CWL=5

18.4 Asynchronous ODT mode

Asynchronous ODT mode is selected when DRAM runs in DLLon mode, but DLL is temporarily disabled (i.e. frozen) in precharge power-down (by MR0 bit A12). Based on the power down mode definitions, this is currently Precharge power down mode if DLL is disabled during precharge power down by MR0 bit A12.

In asynchronous ODT timing mode, internal ODT command is NOT delayed by Additive Latency (AL) relative to the external ODT command.

In asynchronous ODT mode, the following timing parameters apply

$t_{AONPD,min,max}$, $t_{AOFPD,min,max}$

Minimum RTT turn-on time ($t_{AONPDmin}$) is the point in time when the device termination circuit leaves high impedance and ODT resistance begins to turn on. Maximum RTT turn on time ($t_{AONPDmax}$) is the point in time when the ODT resistance is fully on.

$t_{AONPDmin}$ and $t_{AONPDmax}$ are measured from ODT being sampled high.

Minimum RTT turn-off time ($t_{AOFPDmin}$) is the point in time when the device's termination circuit starts to turn off the ODT resistance. Maximum ODT turn off time ($t_{AOFPDmax}$) is the point in time when the on-die termination has reached high impedance. $t_{AOFPDmin}$ and $t_{AOFPDmax}$ are measured from ODT being sampled low.

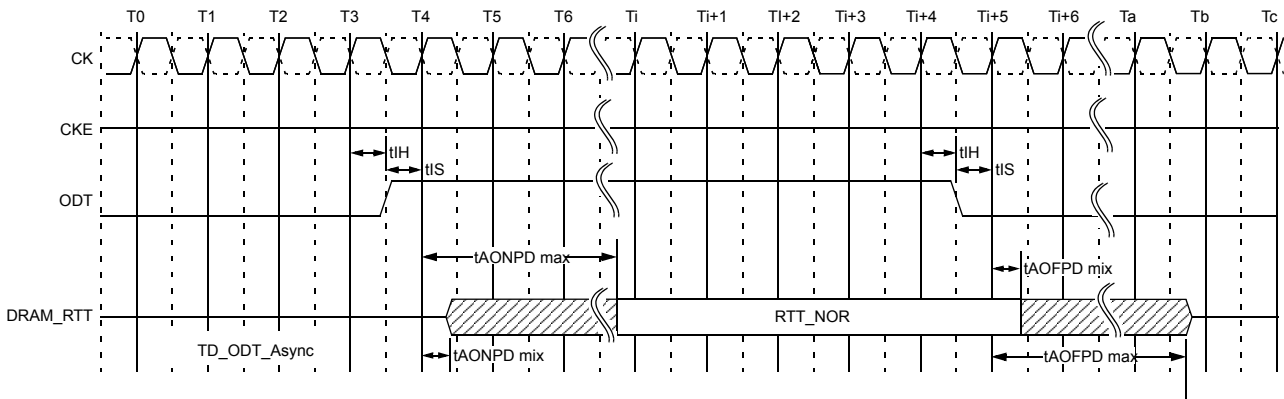


Figure 111. Asynchronous ODT Timing on gDDR3 SDRAM with fast ODT transition: AL is ignored

In Precharge Power Down, ODT receiver remains active, however no Read or Write command can be issued, as the respective ADD/CMD receivers may be disabled.

[Table 79] Asynchronous ODT Timing Parameters for all Speed Bins

Symbol	Description	min	max	Unit
t_{AONPD}	Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	2	8.5	ns
t_{AOFPD}	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	2	8.5	ns

18.4.1 Synchronous to Asynchronous ODT Mode Transition

[Table 80] ODT timing parameters for Power Down (with DLL frozen) entry and exit transition period

Description	min	max
ODT to RTT turn-on delay	$\min\{\text{ODTLon} * t_{CK} + t_{AONmin}; t_{AONPDmin}\}$	$\max\{\text{ODTLon} * t_{CK} + t_{AONmax}; t_{AONPDmax}\}$
	$\min\{(WL - 2.0) * t_{CK} + t_{AONmin}; t_{AONPDmin}\}$	$\max\{(WL - 2.0) * t_{CK} + t_{AONmax}; t_{AONPDmax}\}$
ODT to RTT turn-off delay	$\min\{\text{ODTLoff} * t_{CK} + t_{AOFmin}; t_{AOFPDmin}\}$	$\max\{\text{ODTLoff} * t_{CK} + t_{AOFmax}; t_{AOFPDmax}\}$
	$\min\{(WL - 2.0) * t_{CK} + t_{AOFmin}; t_{AOFPDmin}\}$	$\max\{(WL - 2.0) * t_{CK} + t_{AOFmax}; t_{AOFPDmax}\}$
t_{ANPD}	WL - 1	

18.4.2 Synchronous to Asynchronous ODT Mode Transition during Powerdown Entry

if DLL is selected to be frozen in Precharge Power Down Mode by the setting of bit A12 in MR0 to "0" there is a transition period around power down entry, where the gDDR3 SDRAM may show either synchronous or asynchronous ODT behavior.

This transition period ends when CKE is first registered low and starts t_{ANPD} before that. If there is a Refresh command in progress while CKE goes low, then the transition period ends t_{RFC} after the Refresh command. t_{ANPD} is equal to $(WL-1)$ and is counted (backwards) from the clock cycle where CKE is first registered low. The transition period begins with the starting point of t_{ANPD} and terminates at the end point of $t_{CPDED(min)}$ as shown in Figure 112. If there is a Refresh command in progress while CKE goes low, then the transition period ends at the later one of $t_{RFC(min)}$ after the Refresh command and the end point of $t_{CPDED(min)}$ as shown in Figure 113. Please note that the actual starting point at t_{ANPD} is excluded from the transition period, and the actual end point at $t_{CPDED(min)}$ and $t_{RFC(min)}$, respectively, are included in the transition period.

ODT assertion during the transition period may result in an RTT change as early as the smaller of $t_{AONPD min}$ and $(ODTLon * t_{CK} + t_{AON min})$ and as late as the larger of $t_{AONPD max}$ and $(ODTLoff * t_{CK} + t_{AON max})$. ODT de-assertion during the transition period may late as the larger of $t_{AOFPD max}$ and $(ODTLoff * t_{CK} + t_{AOF max})$. Note that, if AL has a large Value, the range where RTT is uncertain becomes quite large. it shows the three different cases: ODT_A, synchronous behavior before t_{ANPD} ; ODT_B has a state change during the transition period; ODT_C shows a state change after the transition period.

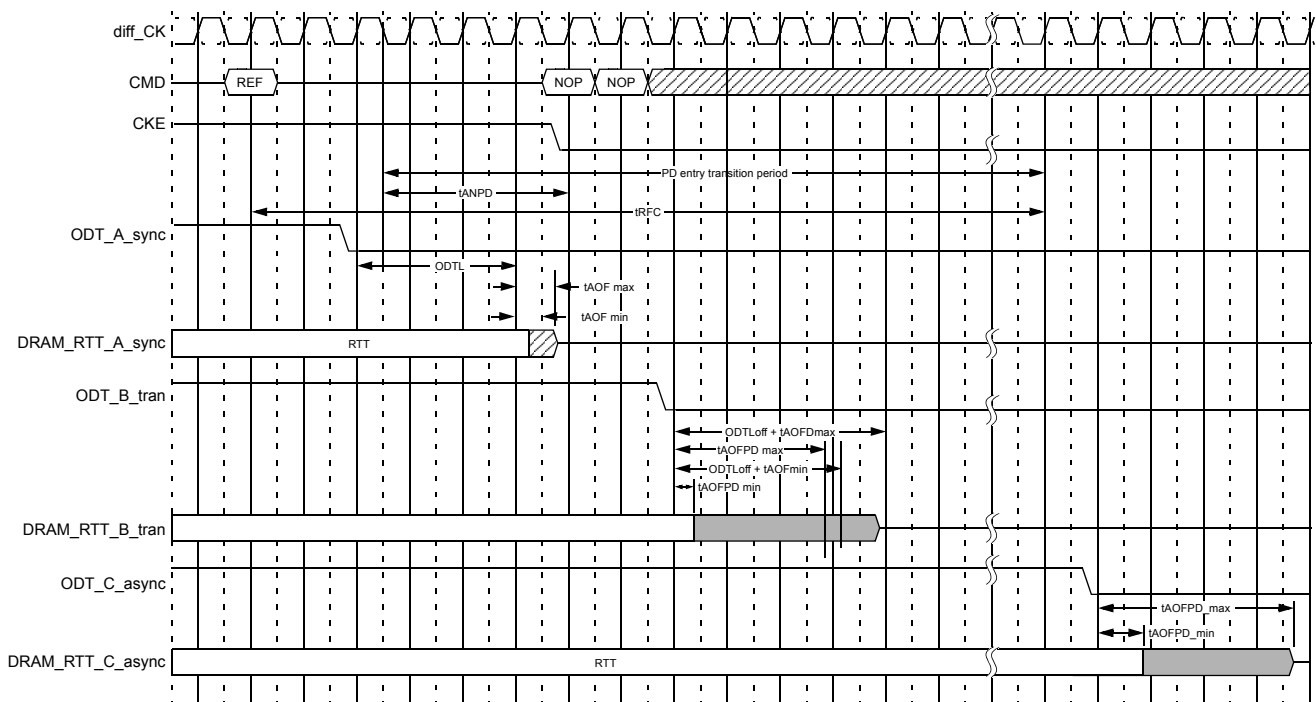


Figure 112. Synchronous to asynchronous transition after Refresh command (AL=0; CWL=5; $t_{ANPD}=WL-1=4$)

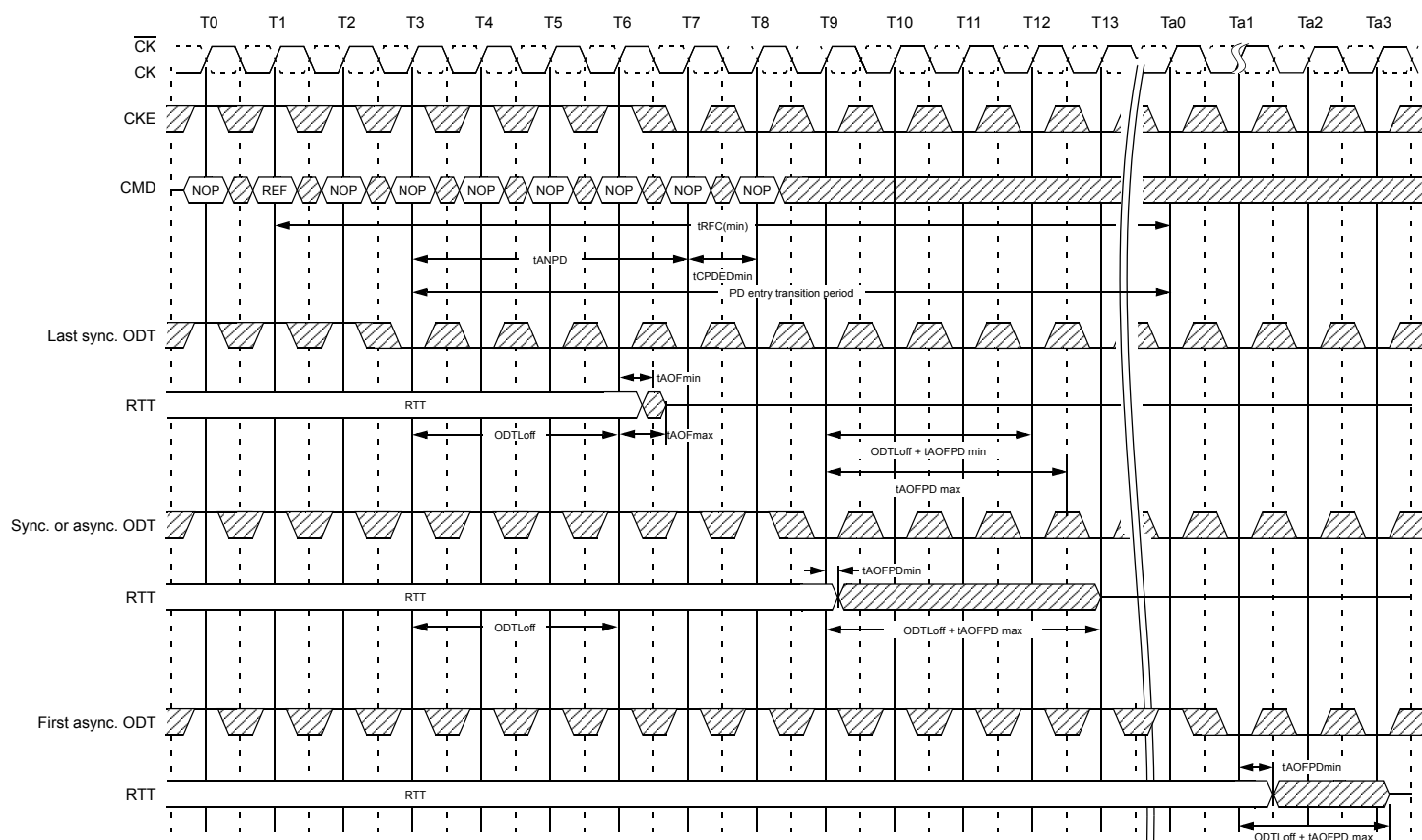


Figure 113. Synchronous to asynchronous transition after Refresh command (AL=0; CWL=5; tANPD=WL-1=4)

18.4.3 Asynchronous to Synchronous ODT Mode Transition during Power-Down Exit

If DLL is selected to be frozen in Precharge Power Down Mode by the setting of bit A12 in MR0 to "0", there is also a transition period around power down exit, where either synchronous or asynchronous response to a change in ODT must be expected from the gDDR3 SDRAM.

This transition period starts t_{ANPD} before CKE is first registered high, and ends t_{XPDLL} after CKE is first registered high. t_{ANPD} is equal to $\max\{ODT_{Loff}, ODT_{Lon}\}$ and is counted from the clock cycle where CKE is first registered high.

ODT assertion during the transition period may result in an RTT change as early as the smaller of t_{AONPD} min and $(ODT_{Lon} * t_{CK} + t_{AON} \min)$ and as late as the larger of t_{AOFPD} max and $(ODT_{Lon} * t_{CK} + t_{AON} \max)$. ODT de-assertion during the transition period may result in an RTT change as early as the smaller of t_{AOFPD} min and $(ODT_{Loff} * t_{CK} + t_{AOF} \min)$ and as late as the larger of t_{AOFPD} max and $(ODT_{Loff} * t_{CK} + t_{AOF} \max)$.

Note that, if AL has a large Value, the range where RTT is uncertain becomes quite large. Figure 114 shows the three different cases: ODT_C, asynchronous response before t_{ANPD} ; ODT_B has a state change of ODT during the transition period; ODT_A shows a state change of ODT after the transition period with synchronous response.

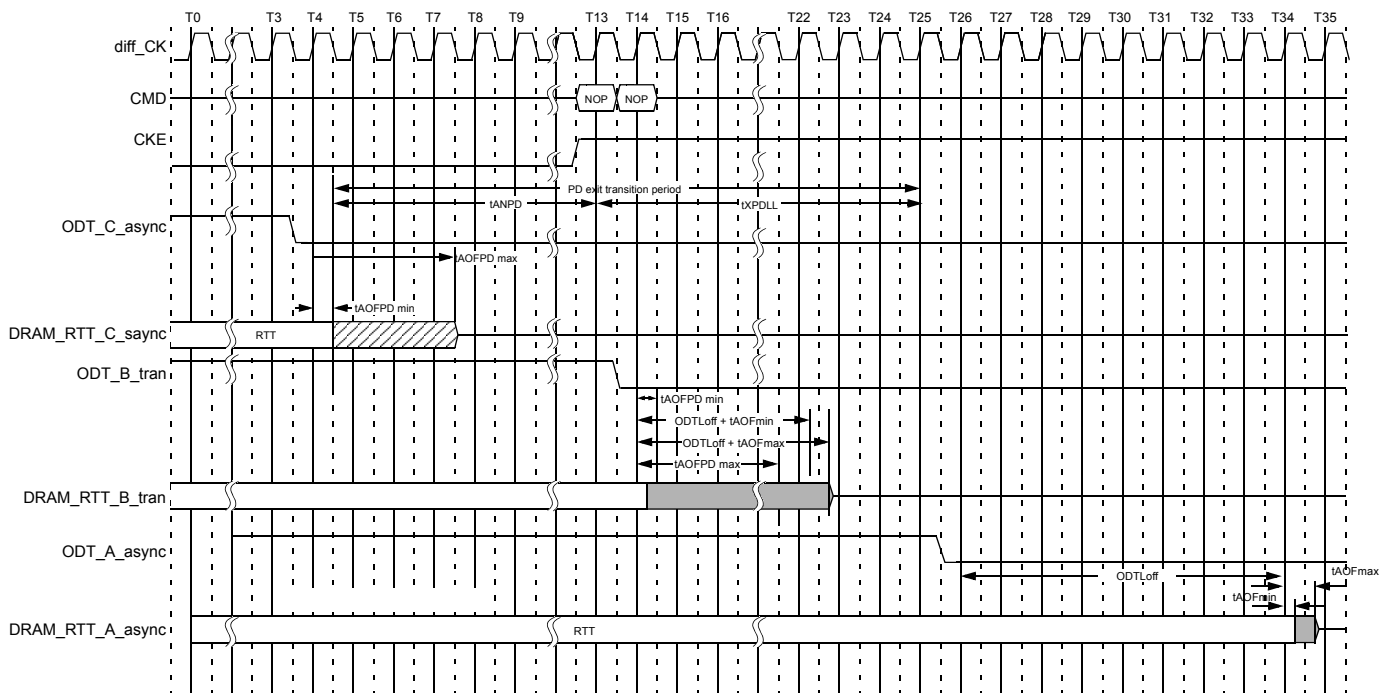


Figure 114. Asynchronous to synchronous transition during Precharge Power Down (with DLL frozen) exit (CL=6; AL=CL-1; CWL=5; $t_{ANPD}=WL-1=9$)

18.4.4 Asynchronous to Synchronous ODT Mode during short CKE high and short CKE low periods

If the total time in Precharge Power Down state or Idle state is very short, the transition periods for PD entry and PD exit may overlap. In this case the response of the gDDR3 SDRAMs RTT to a change in ODT state at the input may be synchronous OR asynchronous from the start of the PD entry transition period to the end of the PD exit transition period (even if the entry period ends later than the exit period).

If the total time in Idle state is very short, the transition periods for PD exit and PD exit and PD entry may overlap. In this case the response of the gDDR3 SDRAMs RTT to a change in ODT state at the input may be synchronous OR asynchronous from the start of the PD exit transition period to the end of the PD entry transition period. Note that, it is assumed that there was no Refresh command in progress when Idle state was entered.

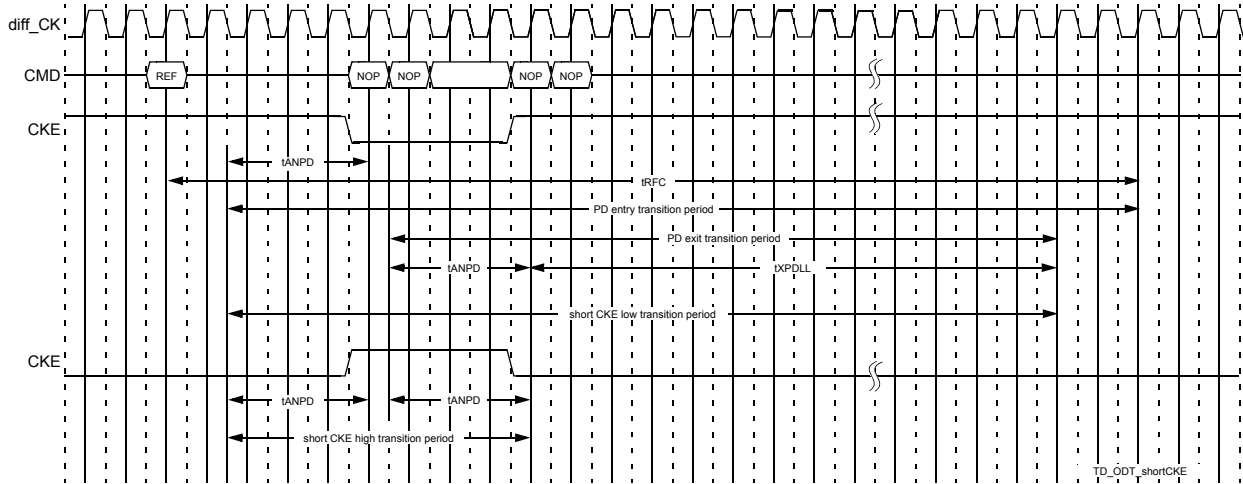


Figure 115. Transition period for short CKE cycles with entry and exit period overlapping
(AL=0, WL=5, tANPD=WL-1=4)