Surface Mount Quartz Crystal Oscillator LGF, PGF and XGF Series

CONNOR WINFIELD

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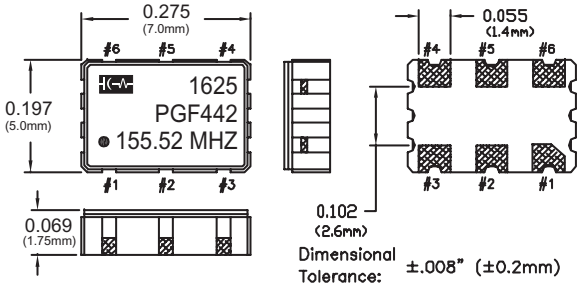
Description:

The Connor-Winfield's LGFxxx Series, PGFxxx Series and XGFxxx Series are 5.0x7.0 mm Surface Mount, LVDS, LVPECL or LVCMOS, Fixed Frequency Crystal Controlled Oscillators (XO). These oscillators are designed for applications requiring high frequency, tight frequency stability, wide temperature range and low jitter. Operating at 2.5 or 3.3 Vdc supply voltage, the LGFxxx series provides LVDS output logic, the PGFxxx series provides LVPECL and XGFxxx series provides LVCMOS. The Enable / disable (OE) function is available on pad 1 or 2. The surface mount package is designed for high-density mounting and is optimum for mass production.

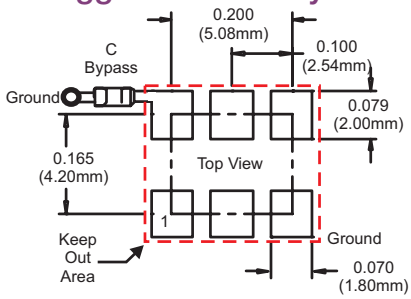
Features:

- Frequency Range
  LGF-PGF Series: 10 MHz to 1.5 GHz
  XGF Series: 10 MHz to 200 MHz
- 3.3 or 2.5 Vdc Operation
- 5x7 mm SMT Package
- Frequency Stabilities Available:
  ±20 ppm, ±25 ppm, ±50 ppm
  or ±100 ppm
- Temperature Ranges Available:
  0 to 70°C, -40 to 85°C, 0 to 85°C
  or -20 to 70°C
- Jitter: <1.5 ps RMS
- LGF Series: Differential LVDS Outputs
- PGF Series: Differential LVPECL Outputs
- XGF Series: LVCMOS Output
- Tri-State Enable/Disable on Pad 1 or 2
- Tape and Reel Packaging
- RoHS Compliant / Lead Free
- Factory Programed Output Frequency
- Fast Delivery of any Output Frequency

Package Outline



Suggested Pad Layout



Keep Out Area: Do not route any traces in the keep out area. It is recommended the next layer under the keep out area is to be ground plane.

Pad Connections

Models: LGFxx2, LGFxx3, PGFxx2, PGFxx3
XGFxx2, XGFxx3

1: Enable / Disable (OE)
2: N/C
3 Ground:
4: Output Q
5: Complementary Output $\overline{Q}$, XGF Series = N/C
6: Supply Voltage (Vcc)

Pad Connections

Models: LGFxx4, LGFxx5, PGFxx4, PGFxx5
XGFxx4, XGFxx5

1: N/C
2: Enable / Disable (OE)
3 Ground:
4: Output Q
5: Complementary Output $\overline{Q}$, XGF Series = N/C
6: Supply Voltage (Vcc)

Ordering Information

PGF	4	4	2	-155.52M
Oscillator Type LGF = LVDS PGF = LVPECL XGF = LVCMOS Clock Series 5x7 mm	Temperature Range 1 = 0 to 70°C 2 = -40 to 85°C 3 = 0 to 85°C 4 = -20 to 70°C	Frequency Tolerance 4 = ±20 ppm 1 = ±25 ppm 2 = ±50 ppm 3 = ±100 ppm	Supply Voltage E/D Function 2 = 2.5 Vdc, E/D Pad 1 3 = 3.3 Vdc, E/D Pad 1 4 = 2.5 Vdc, E/D Pad 2 5 = 3.3 Vdc, E/D Pad 2	Output Frequency Frequency Format -xxx.xM Min.* -xxx.xxxxxxM Max*

*Amount of numbers after the decimal point.
M = MHz
G = GHz

Part Number Examples

PGF442-155.52M = 5x7 mm package, ±20 ppm, -20 to 70°C, 2.5 Vdc, LVPECL Output, E/D Pad 1, Output Frequency 155.52 MHz'
PGF123-311.04M = 5x7 mm package, ±50 ppm, 0 to 70°C, 3.3 Vdc, LVPECL Output, E/D Pad 1, Output Frequency 311.04 MHz
LGF214-622.08M = 5x7 mm package, ±25 ppm, -40 to 85°C, 2.5 Vdc, LVDS Output, E/D Pad 2, Output Frequency 622.08 MHz
LGF325-074.25M = 5x7 mm package, ±50 ppm, 0 to 85°C, 2.5 Vdc, LVDS Output, E/D Pad 2, Output Frequency 74.25 MHz
XGF244-074.25M = 5x7 mm package, ±20 ppm, -40 to 85°C, 2.5 Vdc, LVDS Output, E/D Pad 2, Output Frequency 74.25 MHz
XGF425-038.88M = 5x7 mm package, ±50 ppm, -20 to 70°C, 2.5 Vdc, LVDS Output, E/D Pad 2, Output Frequency 38.88 MHz

RoHS COMPLIANT

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Absolute Maximum Ratings

Parameter	Minimum	Nominal	Maximum	Units	Notes
Storage Temperature	-55	-	125	°C	
Supply Voltage (Vcc)	-0.5	-	4.2	Vdc	
Input Voltage	-0.5	-	Vcc+0.5	Vdc	

Absolute Ratings: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only. The functional operation of the device at those or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to conditions outside the "recommended operating conditions" for any extended period of time may adversely impact device reliability and result in failures not covered by warranty.

Model Series

LGFxxx Series	LVDS Output Series
PGFxxx Series	LVPECL Output Series
XGFxxx Series	LVCMOS Output Series

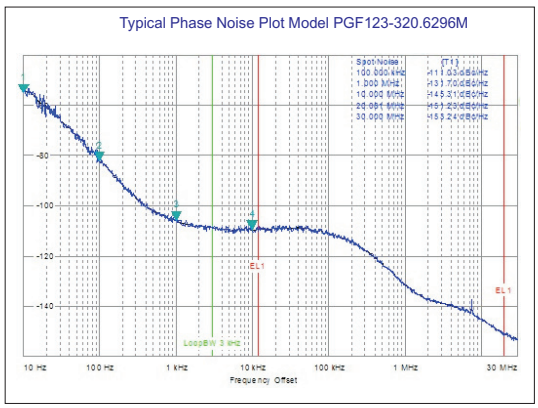
Operating Specifications

Parameter		Minimum	Nominal	Maximum	Units	Notes
Frequencies Available: (Fo)	LVDS or LVPECL	10	-	1500	MHz	
	LVCMOS	10	-	200	MHz	
Operating Temperature Range: (See Ordering Information)						
Temperature Code 1		0	-	70	°C	
Temperature Code 2		-40	-	85	°C	
Temperature Code 3		0	-	85	°C	
Temperature Code 4		-20	-	70	°C	
Total Frequency Tolerance: (See Ordering Information)						
Tolerance Code 4		-20.0	-	20.0	ppm	1
Tolerance Code 1		-25.0	-	25.0	ppm	1
Tolerance Code 2		-50.0	-	50.0	ppm	1
Tolerance Code 3		-100.0	-	100.0	ppm	1
Supply Voltage: (Vcc)						
Supply Voltage Code 2 or 4		2.375	2.5	2.625	Vdc	±5%
Supply Voltage Code 3 or 5		3.135	3.3	3.465	Vdc	±5%
Supply Current		-	30	50	mA	
Start-Up Time:		-	-	10	ms	

Jitter / Phase Noise Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Jitter					
Period Jitter	-	6.0	8.0	ps RMS	
Integrated Phase Jitter (BW = 12 KHz to 20 MHz)	-	1.1	1.5	ps RMS	
SSB Phase Noise for Fo = 320.6296 MHz					
@ 10 Hz offset	-	-55	-	dBC/Hz	
@ 100 Hz offset	-	-82	-	dBC/Hz	
@ 1 KHz offset	-	-106	-	dBC/Hz	
@ 10 KHz offset	-	-110	-	dBC/Hz	
@ 100 KHz offset	-	-111	-	dBC/Hz	
@ 1 MHz offset	-	-132	-	dBC/Hz	
@ 10 MHz offset	-	-145	-	dBC/Hz	

Phase Noise Plot



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OE Input Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Enable / Disable Function Option:					
Models LGFxx2, LGFxx3, PGFxx2, PGFxx3, XGFxx2, XPGFxx3 - OE Pad 1, N/C Pad 2					
Models LGFxx4, LGFxx5, PGFxx4, PGFxx5, XGFxx4, XGFxx5 - OE Pad 2, N/C Pad 1					
Enable Voltage (V_{IH})	70% Vcc	-	-	Vdc	
Disable Voltage (V_{IL})	-	-	30% Vcc	Vdc	2
Enable Time	-	-	200	ns	
Disable Time	-	-	50	ns	

Enable / Disable Function

Function: (Pad 1 or 2)	Output
Low or Open:	Disabled (High Impedance)
High	Enabled

LVDS Output Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Load	-	100	-	Ohm	
Output Differential Voltage (Vod)	250	-	450	mV	3
Output Swing (Differential Output Pk to Pk)	500	700	900	mV	
Duty Cycle at 50% of output voltage swing	45	50	55	%	4
Differential Rise / Fall Time: -	-	0.15	0.35	ns	5

LVPECL Output Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Load	-	50	-	pF	6
Output Voltage: Vcc = 2.5 Vdc					
High (V_{OH})	1.475	-	-	V	
Low (V_{OL})	-	-	0.880	V	
Output Voltage: Vcc = 3.3 Vdc					
High (V_{OH})	2.275	-	-	V	
Low (V_{OL})	-	-	1.680	V	
Duty Cycle at 50% of output voltage swing	45	50	55	%	4
Rise / Fall Time: 20% to 80%	-	350	500	ps	

LVCMOS Output Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Load	-	15	-	pF	
Output Voltage:					
High (V_{OH})	90%Vcc	-	-	V	
Low (V_{OL})	-	-	10%Vcc	V	
Duty Cycle at 50% of output voltage swing	45	50	55	%	4
Rise / Fall Time: 10% to 90%	-	300	600	ps	

Package Characteristics

Package	Hermetically sealed ceramic package and metal cover

Environmental Characteristics

Vibration:	Vibration per Mil Std 883E Method 2007.3 Test Condition A.
Shock:	Mechanical Shock per Mil Std 883E Method 2002.4 Test Condition B.
Soldering Process;	RoHS compliant lead free. See soldering profile on page 4.

Notes:

1. *Includes calibration @ 25°C, frequency stability vs. change in temperature, supply voltage and load variations, shock and vibration and 20 years aging.*
2. *When the oscillator is disabled the outputs go to tri-state level (high impedance) which floats to VOL. Outputs are enabled with no connection on E/D pad.*
3. *Vod is measured with a 100 ohm resistor between the true and the complementary outputs.*
4. *Duty cycle measured at 50% of output voltage swing.*
5. *Rise and fall times measured from 10% to 90%*
6. *Outputs must be terminated into 50 ohms to Vcc – 2V or Thevenin equivalent.*

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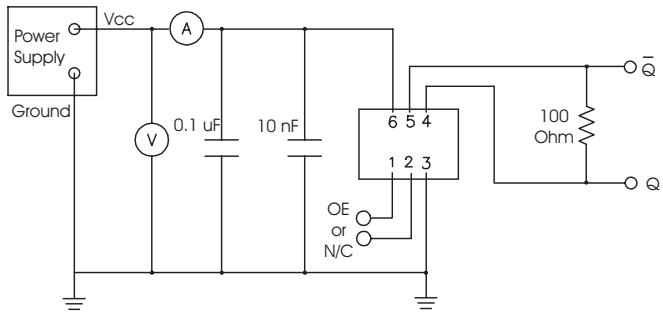
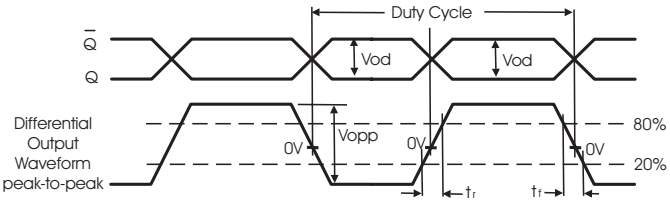
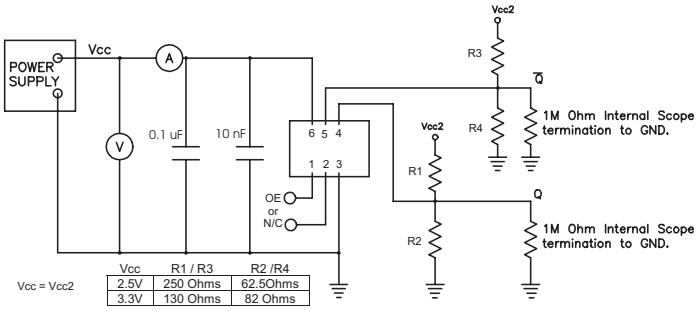
LVDS Test Circuit



LVDS Output Waveform



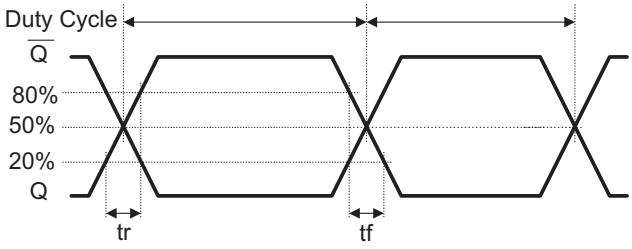
LVPECL Test Circuit



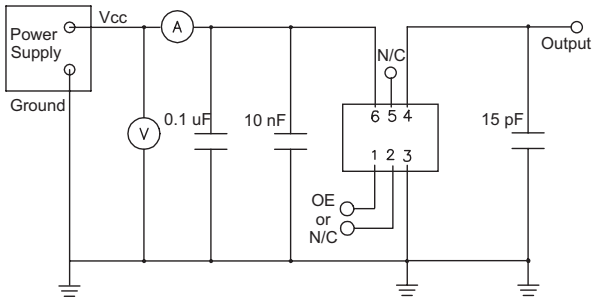
Vcc = Vcc2

Vcc	R1 / R3	R2 /R4
2.5V	250 Ohms	62.5Ohms
3.3V	130 Ohms	82 Ohms

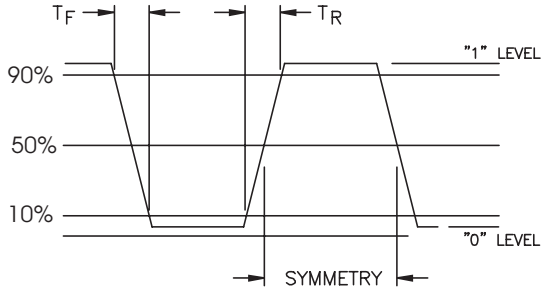
LVPECL Output Waveform



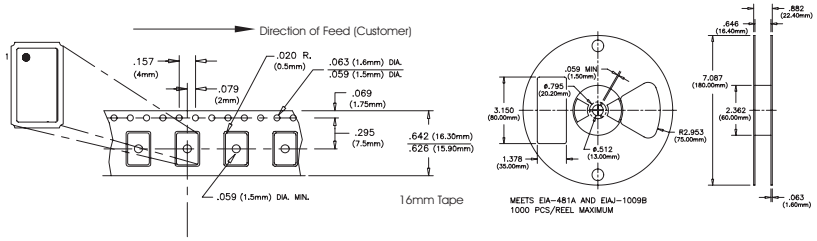
LVCMOS Test Circuit



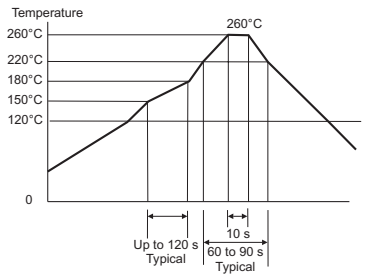
LVCMOS Output Waveform



Tape and Reel Dimensions



RoHS Solder Profile



Meets IPC/JEDEC J-STD-020C

Revision History

Revision	Date	Note
00	07/09/13	Data sheet released
01	07/10/13	Corrected supply voltage code, page 2.
02	08/23/13	Added LVDS series to the data sheet.
03	12/06/13	Updated phase noise.
04	12/18/13	Added LVCMOS series to data sheet.
05	06/16/16	Updated period jitter and rise/fall times.