## *HYUNDAI 4 Banks X 4/2/1M X 4/8/16 bits DDR SDRAM*

** The contents of this document are subject to change without notice*

# *DATA SHEET*

# HY5DV654022-75/80/10
# HY5DV658022-75/80/10
# HY5DV651622-75/80/10

# *HYUNDAI 4 Banks X 4/2/1M X 4/8/16 bits DDR SDRAM*

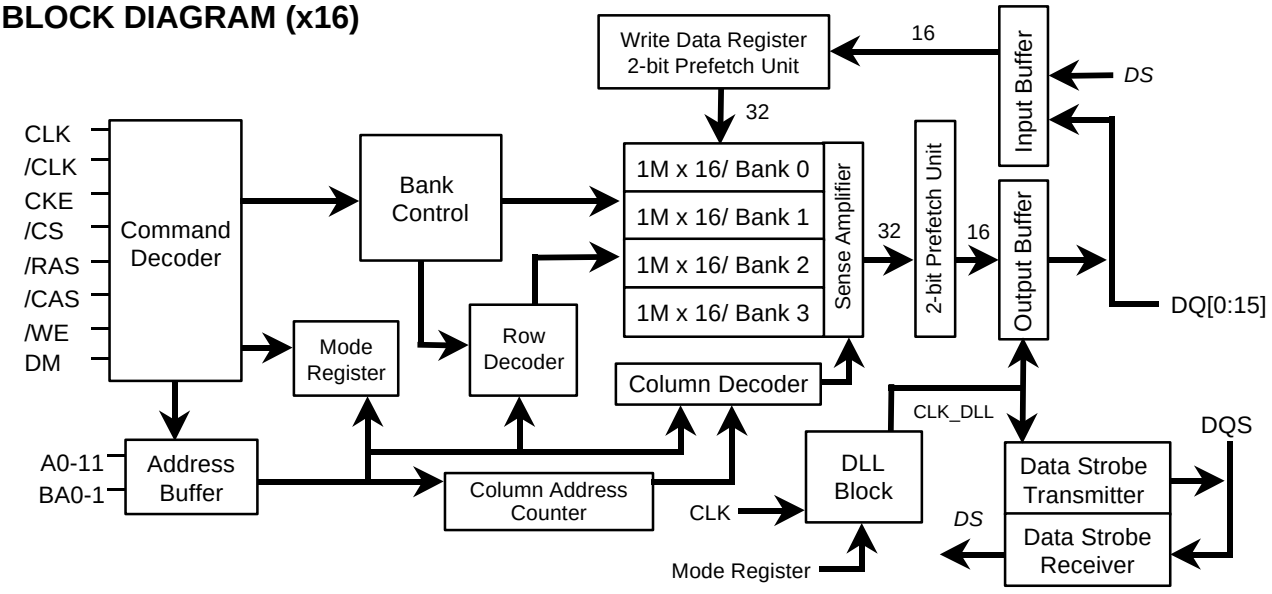
## DESCRIPTION

HY5DV654022-75/80/10, HY5DV658022-75/80/10 and HY5DV651623-75/80/10 are high speed 3.3 V(I/O= 2.5V) 64M Double Data Rate(DDR) Synchronous DRAM fabricated with the Hyundai high performance CMOS process. While all address and control inputs are latched on the rising edge of the clock(falling edge of the /clock), data, data strobe and data mask inputs are sampled on both rising and falling edge of the clock. The data path is internally pipelined and 2-bit prefetched to achieve higher bandwidth. Because data rate is doubled through reading and writing at both rising and falling edge of the clock, 2X higher data bandwidth can be achieved.

## FEATURES

- 3.3V VDD and 2.5V VDDQ power supply
- Internal 4 banks with single pulsed RAS
- Fully differential clock operation with clock frequency 100MHz/125MHz/133MHz
- Data output on data strobe(DQS) edge when read (edged DQ)
- Data input on data strobe(DQS) center when write (centered DQ)
- Data strobe synchronized with output data for read and input data for write
- Programmable CAS latency 1.5/2.0/2.5 supported
- Programmable burst length 2/4/8 with both sequential and interleave mode
- Delay Locked Loop(DLL) installed with DLL reset mode
- SSTL_2 interface for all inputs and outputs
- Write mask byte control with LDM and UDM
- Bytewide data strobe with LDQS and UDQS
- Auto refresh and self refresh supported
- 4K/64ms refresh cycle
- 400mil 66 pin 0.65mm pin pitch TSOP-II package

## BLOCK DIAGRAM (x16)



# *HYUNDAI 4 Banks X 4/2/1M X 4/8/16 bits DDR SDRAM*

## ORDERING INFORMATION

**HY 5D V 65 40 2 2 _ L TC - 10**

**HYUNDAI**

Memory Products

**PRODUCT GROUP**

55 - FP DRAM
56 - EDO DRAM
57 - SDRAM
5D - DDR SDRAM

**PROCESS & POWER SUPPLY**

BLANK - CMOS 5.0V VDD
V - CMOS 3.3V VDD
U - CMOS 2.5V VDD

**DENSITY & REFRESH CYCLE**

64 - 64M bits, 8K refresh
65 - 64M bits, 4K refresh

**DATA WIDTH**

40 - x4
80 - x8
16 - x16
32 - x32

**NUMBER OF BANKS**

1 - 2 banks
2 - 4 banks

**INTERFACE**

0 - LVTTL
1 - SSTL-3
2 - SSTL-2
3 - Mixed Interface

**DIE GENERATION**

BLANK - 1st Gen.
A - 2nd Gen.
B - 3rd Gen.
C - 4th Gen.

**POWER CONSUMPTION**

BLANK - Normal
L - Low power

**PACKAGE**

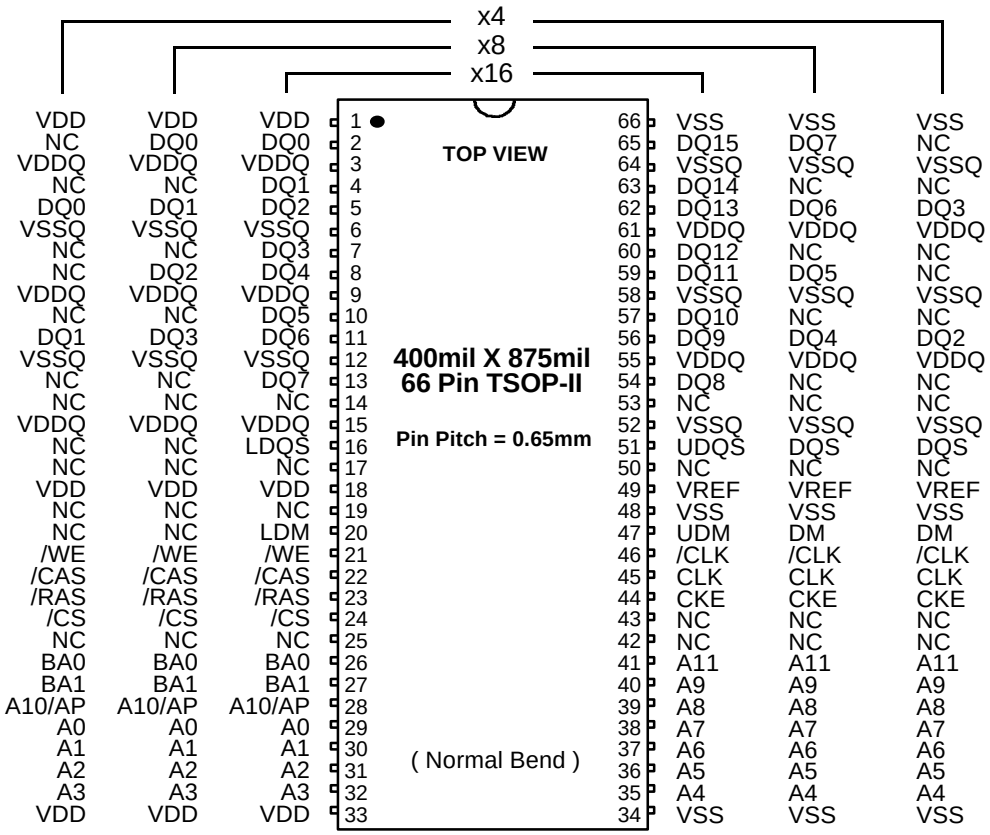
JC - 400mil SOJ
TC - 400mil TSOP-II

**SPEED**

75 - 7.5ns(133MHz)
80 - 8ns(125MHz)
10 - 10ns(100MHz)
12 - 12ns(83MHz)
15 - 15ns(66MHz)
10P - PC/100, CL=2/3
10S - PC/100, CL=2

# *HYUNDAI 4 Banks X 4/2/1M X 4/8/16 bits DDR SDRAM*

## PIN CONFIGURATION & DESCRIPTION




| Pin | Description |
|---|---|
| A0 - A11 | Row / Column Address |
| BA0, BA1 | Bank Select Address |
| DQ0 - DQ15 | Data Input/Output |
| /CS | Chip Select |
| /RAS | Row Address Strobe |
| /CAS | Column Address Strobe |
| /WE | Write Enable |
| LDM, UDM | Write Mask(Lower/Upper Byte) |
| CLK, /CLK | Clock Input |
| CKE | Clock Enable |
| LDQS, UDQS | Data Strobe(Lower/Upper Byte) |
| VREF | Reference Voltage |
| VDD, VSS | Power, Ground |
| VDDQ, VSSQ | I/O Power, I/O Ground |
| NC | No Connection |

# *HYUNDAI 4 Banks X 4/2/1M X 4/8/16 bits DDR SDRAM*

## ADDRESS MAPPING TABLE

| Organization | Bank Select | Row Address | Column Address | Autoprecharge |
|---|---|---|---|---|
| x4 | BA0, BA1 | A0 ~ A11 | A0~A9 | A10 |
| x8 | BA0, BA1 | A0 ~ A11 | A0~A8 | A10 |
| x16 | BA0, BA1 | A0 ~ A11 | A0~A7 | A10 |

## COMMAND TRUTH TABLE

| Function | Symbol | $CKE_{n-1}$ | $CKE_n$ | /CS | /RAS | /CAS | /WE | A11 | A10 | BA | A9-0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Device Deselect | DSEL | H | X | H | X | X | X | X | X | X | X |
| No Operation | NOP | H | X | L | H | H | H | X | X | X | X |
| Read | READ | H | X | L | H | L | H | X | L | V | V |
| Read w/ Autoprecharge | READAP | H | X | L | H | L | H | X | H | V | V |
| Write | WRITE | H | X | L | H | L | L | X | L | V | V |
| Write w/ Autoprecharge | WRITEAP | H | X | L | H | L | L | X | H | V | V |
| Bank Activate | ACT | H | X | L | L | H | H | V | V | V | V |
| Precharge Selected Bank | PRE | H | X | L | L | H | L | X | L | V | X |
| Precharge All Banks | PALL | H | X | L | L | H | L | X | H | X | X |
| Read Burst Stop | BST | H | X | L | H | H | L | X | X | X | X |
| Auto Refresh | AREF | H | H | L | L | L | H | X | X | X | X |
| Self Refresh Entry | SREF | H | L | L | L | L | H | X | X | X | X |
| Self Refresh Exit | SREX | L | H | H | X | X | X | X | X | X | X |
| Power Down Entry | PDEN | H | L | X | X | X | X | X | X | X | X |
| Power Down Exit | PDEX | L | H | H | X | X | X | X | X | X | X |
| Mode Register Set | MRS | H | X | L | L | L | L | L | L | V | V |

## WRITE DATA MASK TRUTH TABLE

| Function | $CKE_{n-1}$ | $CKE_n$ | UDM | LDM |
|---|---|---|---|---|
| Data Write/Output Enable | H | X | L | L |
| Data Mask/Output Disable | H | X | H | H |
| Upper Byte Write Enable / Lower Byte Mask | H | X | L | H |
| Lower Byte Write Enable / Upper Byte Mask | H | X | H | L |

*Notes : 'H' - Logic High Level, 'L' - Logic Low Level, 'X' - Don't Care, 'V' - Valid Data Input*

# *HYUNDAI 4 Banks X 4/2/1M X 4/8/16 bits DDR SDRAM*

## OPERATION COMMAND TRUTH TABLE

| Current State | /CS | /RAS | /CAS | /WE | Address | Command | Action |
|---|---|---|---|---|---|---|---|
| **IDLE** | H | X | X | X | X | DSEL | NOP or power down [3] |
| | L | H | H | H | X | NOP | NOP or power down [3] |
| | L | H | H | L | X | BST | ILLEGAL[4] |
| | L | H | L | H | BA, CA, A10 | READ/READAP | ILLEGAL[4] |
| | L | H | L | L | BA, CA, A10 | WRITE/WRITEAP | ILLEGAL[4] |
| | L | L | H | H | BA, RA | ACT | Row Activation |
| | L | L | H | L | BA, A10 | PRE/PALL | NOP |
| | L | L | L | H | X | AREF/SREF | Auto Refresh or Self Refresh [5] |
| | L | L | L | L | OPCODE | MRS | Mode Register Set |
| **ROW ACTIVE** | H | X | X | X | X | DSEL | NOP |
| | L | H | H | H | X | NOP | NOP |
| | L | H | H | L | X | BST | ILLEGAL[4] |
| | L | H | L | H | BA, CA, A10 | READ/READAP | Begin read : optional AP [6] |
| | L | H | L | L | BA, CA, A10 | WRITE/WRITEAP | Begin write : optional AP [6] |
| | L | L | H | H | BA, RA | ACT | ILLEGAL[4] |
| | L | L | H | L | BA, A10 | PRE/PALL | Precharge [7] |
| | L | L | L | H | X | AREF/SREF | ILLEGAL[11] |
| | L | L | L | L | OPCODE | MRS | ILLEGAL[11] |
| **READ** | H | X | X | X | X | DSEL | Continue burst to end |
| | L | H | H | H | X | NOP | Continue burst to end |
| | L | H | H | L | X | BST | Terminate burst |
| | L | H | L | H | BA, CA, A10 | READ/READAP | Term burst, new read:optional AP [8] |
| | L | H | L | L | BA, CA, A10 | WRITE/WRITEAP | ILLEGAL |
| | L | L | H | H | BA, RA | ACT | ILLEGAL[4] |
| | L | L | H | L | BA, A10 | PRE/PALL | Term burst, precharge |
| | L | L | L | H | X | AREF/SREF | ILLEGAL[11] |
| | L | L | L | L | OPCODE | MRS | ILLEGAL[11] |
| **WRITE** | H | X | X | X | X | DSEL | Continue burst to end |
| | L | H | H | H | X | NOP | Continue burst to end |
| | L | H | H | L | X | BST | ILLEGAL[4] |
| | L | H | L | H | BA, CA, A10 | READ/READAP | Term burst, new read:optional AP [8] |
| | L | H | L | L | BA, CA, A10 | WRITE/WRITEAP | Term burst, new write:optional AP |

# *HYUNDAI 4 Banks X 4/2/1M X 4/8/16 bits DDR SDRAM*

## OPERATION COMMAND TRUTH TABLE

| Current State | /CS | /RAS | /CAS | /WE | Address | Command | Action |
|---|---|---|---|---|---|---|---|
| **WRITE** | L | L | H | H | BA, RA | ACT | ILLEGAL[4] |
| | L | L | H | L | BA, A10 | PRE/PALL | Term burst, precharge |
| | L | L | L | H | X | AREF/SREF | ILLEGAL[11] |
| | L | L | L | L | OPCODE | MRS | ILLEGAL[11] |
| **READ WITH AUTOPRE-CHARGE** | H | X | X | X | X | DSEL | Continue burst to end |
| | L | H | H | H | X | NOP | Continue burst to end |
| | L | H | H | L | X | BST | ILLEGAL |
| | L | H | L | H | BA, CA, A10 | READ/READAP | ILLEGAL[10] |
| | L | H | L | L | BA, CA, A10 | WRITE/WRITEAP | ILLEGAL[10] |
| | L | L | H | H | BA, RA | ACT | ILLEGAL[4,10] |
| | L | L | H | L | BA, A10 | PRE/PALL | ILLEGAL[4,10] |
| | L | L | L | H | X | AREF/SREF | ILLEGAL[11] |
| | L | L | L | L | OPCODE | MRS | ILLEGAL[11] |
| **WRITE WITH AUTOPRE-CHARGE** | H | X | X | X | X | DSEL | Continue burst to end |
| | L | H | H | H | X | NOP | Continue burst to end |
| | L | H | H | L | X | BST | ILLEGAL |
| | L | H | L | H | BA, CA, A10 | READ/READAP | ILLEGAL[10] |
| | L | H | L | L | BA, CA, A10 | WRITE/WRITEAP | ILLEGAL[10] |
| | L | L | H | H | BA, RA | ACT | ILLEGAL[4,10] |
| | L | L | H | L | BA, A10 | PRE/PALL | ILLEGAL[4,10] |
| | L | L | L | H | X | AREF/SREF | ILLEGAL[11] |
| | L | L | L | L | OPCODE | MRS | ILLEGAL[11] |
| **PRE-CHARGE** | H | X | X | X | X | DSEL | NOP - Enter IDLE after tRP |
| | L | H | H | H | X | NOP | NOP - Enter IDLE after tRP |
| | L | H | H | L | X | BST | ILLEGAL[4] |
| | L | H | L | H | BA, CA, A10 | READ/READAP | ILLEGAL[4,10] |
| | L | H | L | L | BA, CA, A10 | WRITE/WRITEAP | ILLEGAL[4,10] |
| | L | L | H | H | BA, RA | ACT | ILLEGAL[4,10] |
| | L | L | H | L | BA, A10 | PRE/PALL | NOP - Enter IDLE after tRP |
| | L | L | L | H | X | AREF/SREF | ILLEGAL[11] |
| | L | L | L | L | OPCODE | MRS | ILLEGAL[11] |

# *HYUNDAI 4 Banks X 4/2/1M X 4/8/16 bits DDR SDRAM*

## OPERATION COMMAND TRUTH TABLE

| Current State | /CS | /RAS | /CAS | /WE | Address | Command | Action |
|---|---|---|---|---|---|---|---|
| **ROW ACTIVATING** | H | X | X | X | X | DSEL | NOP - Enter ROW ACT after tRCD |
| | L | H | H | H | X | NOP | NOP - Enter ROW ACT after tRCD |
| | L | H | H | L | X | BST | ILLEGAL[4] |
| | L | H | L | H | BA, CA, A10 | READ/READAP | ILLEGAL[4,10] |
| | L | H | L | L | BA, CA, A10 | WRITE/WRITEAP | ILLEGAL[4,10] |
| | L | L | H | H | BA, RA | ACT | ILLEGAL[4,9,10] |
| | L | L | H | L | BA, A10 | PRE/PALL | ILLEGAL[4,10] |
| | L | L | L | H | X | AREF/SREF | ILLEGAL[11] |
| | L | L | L | L | OPCODE | MRS | ILLEGAL[11] |
| **WRITE RECOVERING** | H | X | X | X | X | DSEL | NOP - Enter ROW ACT after tDPL |
| | L | H | H | H | X | NOP | NOP - Enter ROW ACT after tDPL |
| | L | H | H | L | X | BST | ILLEGAL[4] |
| | L | H | L | H | BA, CA, A10 | READ/READAP | ILLEGAL |
| | L | H | L | L | BA, CA, A10 | WRITE/WRITEAP | ILLEGAL |
| | L | L | H | H | BA, RA | ACT | ILLEGAL[4,10] |
| | L | L | H | L | BA, A10 | PRE/PALL | ILLEGAL[4,11] |
| | L | L | L | H | X | AREF/SREF | ILLEGAL[11] |
| | L | L | L | L | OPCODE | MRS | ILLEGAL[11] |
| **WRITE RECOVERING WITH AUTOPRECHARGE** | H | X | X | X | X | DSEL | NOP - Enter precharge after tDPL |
| | L | H | H | H | X | NOP | NOP - Enter precharge after tDPL |
| | L | H | H | L | X | BST | ILLEGAL[4] |
| | L | H | L | H | BA, CA, A10 | READ/READAP | ILLEGAL[4,8,10] |
| | L | H | L | L | BA, CA, A10 | WRITE/WRITEAP | ILLEGAL[4,10] |
| | L | L | H | H | BA, RA | ACT | ILLEGAL[4,10] |
| | L | L | H | L | BA, A10 | PRE/PALL | ILLEGAL[4,11] |
| | L | L | L | H | X | AREF/SREF | ILLEGAL[11] |
| | L | L | L | L | OPCODE | MRS | ILLEGAL[11] |
| **REFRESHING** | H | X | X | X | X | DSEL | NOP - Enter IDLE after tRC |
| | L | H | H | H | X | NOP | NOP - Enter IDLE after tRC |
| | L | H | H | L | X | BST | ILLEGAL[11] |
| | L | H | L | H | BA, CA, A10 | READ/READAP | ILLEGAL[11] |

# *HYUNDAI 4 Banks X 4/2/1M X 4/8/16 bits DDR SDRAM*

## OPERATION COMMAND TRUTH TABLE

| Current State | /CS | /RAS | /CAS | /WE | Address | Command | Action |
|---|---|---|---|---|---|---|---|
| REFRESH-ING | L | H | L | L | BA, CA, A10 | WRITE/WRITEAP | ILLEGAL[11] |
| | L | L | H | H | BA, RA | ACT | ILLEGAL[11] |
| | L | L | H | L | BA, A10 | PRE/PALL | ILLEGAL[11] |
| | L | L | L | H | X | AREF/SREF | ILLEGAL[11] |
| | L | L | L | L | OPCODE | MRS | ILLEGAL[11] |
| MODE REGISTER ACCESSING | H | X | X | X | X | DSEL | NOP - Enter IDLE after tMRD |
| | L | H | H | H | X | NOP | NOP - Enter IDLE after tMRD |
| | L | H | H | L | X | BST | ILLEGAL[11] |
| | L | H | L | H | BA, CA, A10 | READ/READAP | ILLEGAL[11] |
| | L | H | L | L | BA, CA, A10 | WRITE/WRITEAP | ILLEGAL[11] |
| | L | L | H | H | BA, RA | ACT | ILLEGAL[11] |
| | L | L | H | L | BA, A10 | PRE/PALL | ILLEGAL[11] |
| | L | L | L | H | X | AREF/SREF | ILLEGAL[11] |
| | L | L | L | L | OPCODE | MRS | ILLEGAL[11] |

*Notes :*

*1. 'H' - Logic High Level, 'L' - Logic Low Level, 'X' - Don't Care, 'V' - Valid Data Input, BA - Bank Address AP - Auto Precharge, CA - Column Address, RA - Row Address, NOP - NO Operation*

*2. All entries assume that CKE was active(high level) during the preceding clock cycle.*

*3. If both banks are idle and CKE is inactive(low level), then in power down mode.*

*4. Illegal to bank in specified state. Function may be legal in the bank indicated by Bank Address(BA), depending on the state of that bank.*

*5. If both banks are idle and CKE is inactive(low level), then self refresh mode.*

*6. Illegal if tRCD is not met*

*7. Illegal if tRAS is not met.*

*8. Must satisfy bus contention, bus turn around, and/or write recovery requirements*

*9. Illegal if tRRD is not met.*

*10. Illegal for single bank, but legal for other banks in multi-bank devices.*

*11. Illegal for all banks.*

# *HYUNDAI 4 Banks X 4/2/1M X 4/8/16 bits DDR SDRAM*

## CKE FUNCTION TRUTH TABLE

| Current State | $CKE_{n-1}$ | $CKE_n$ | /CS | /RAS | /CAS | /WE | ADD | Action |
|---|---|---|---|---|---|---|---|---|
| **SELF[1] REFRESH** | H | X | X | X | X | X | X | INVALID |
| | L | H | H | X | X | X | X | Exit self refresh, enter idle after tSREX |
| | L | H | L | H | H | H | X | Exit self refresh, enter idle after tSREX [3] |
| | L | H | L | H | H | L | X | ILLEGAL |
| | L | H | L | H | L | X | X | ILLEGAL |
| | L | H | L | L | X | X | X | ILLEGAL |
| | L | L | X | X | X | X | X | NOP, continue self refresh |
| **POWER[2] DOWN** | H | X | X | X | X | X | X | INVALID |
| | L | H | H | X | X | X | X | Exit power down, enter idle |
| | L | H | L | H | H | H | X | Exit power down, enter idle |
| | L | H | L | H | H | L | X | ILLEGAL |
| | L | H | L | H | L | X | X | ILLEGAL |
| | L | H | L | L | X | X | X | ILLEGAL |
| | L | L | X | X | X | X | X | NOP, continue power down mode |
| **ALL[4] BANKS IDLE** | H | H | X | X | X | X | X | See operation command truth table |
| | H | L | L | L | L | H | X | Enter self refresh |
| | H | L | H | X | X | X | X | Enter power down |
| | H | L | L | H | H | H | X | Enter power down |
| | H | L | L | H | H | L | X | ILLEGAL |
| | H | L | L | H | L | X | X | ILLEGAL |
| | H | L | L | L | H | X | X | ILLEGAL |
| | H | L | L | L | L | L | X | ILLEGAL |
| | L | L | X | X | X | X | X | NOP |
| **Any State other than above** | H | H | X | X | X | X | X | See operation command truth table |
| | H | L | X | X | X | X | X | ILLEGAL[5] |
| | L | H | X | X | X | X | X | INVALID |
| | L | L | X | X | X | X | X | INVALID |

*Notes :*

*When CKE=L, all DQ and DQS must be in Hi-Z state*

*1. CKE and /CS must be kept high for a minimum of 200 stable input clocks before issuing any command*

*2. All command can be stored after 2 clocks from low to high transition of CKE*

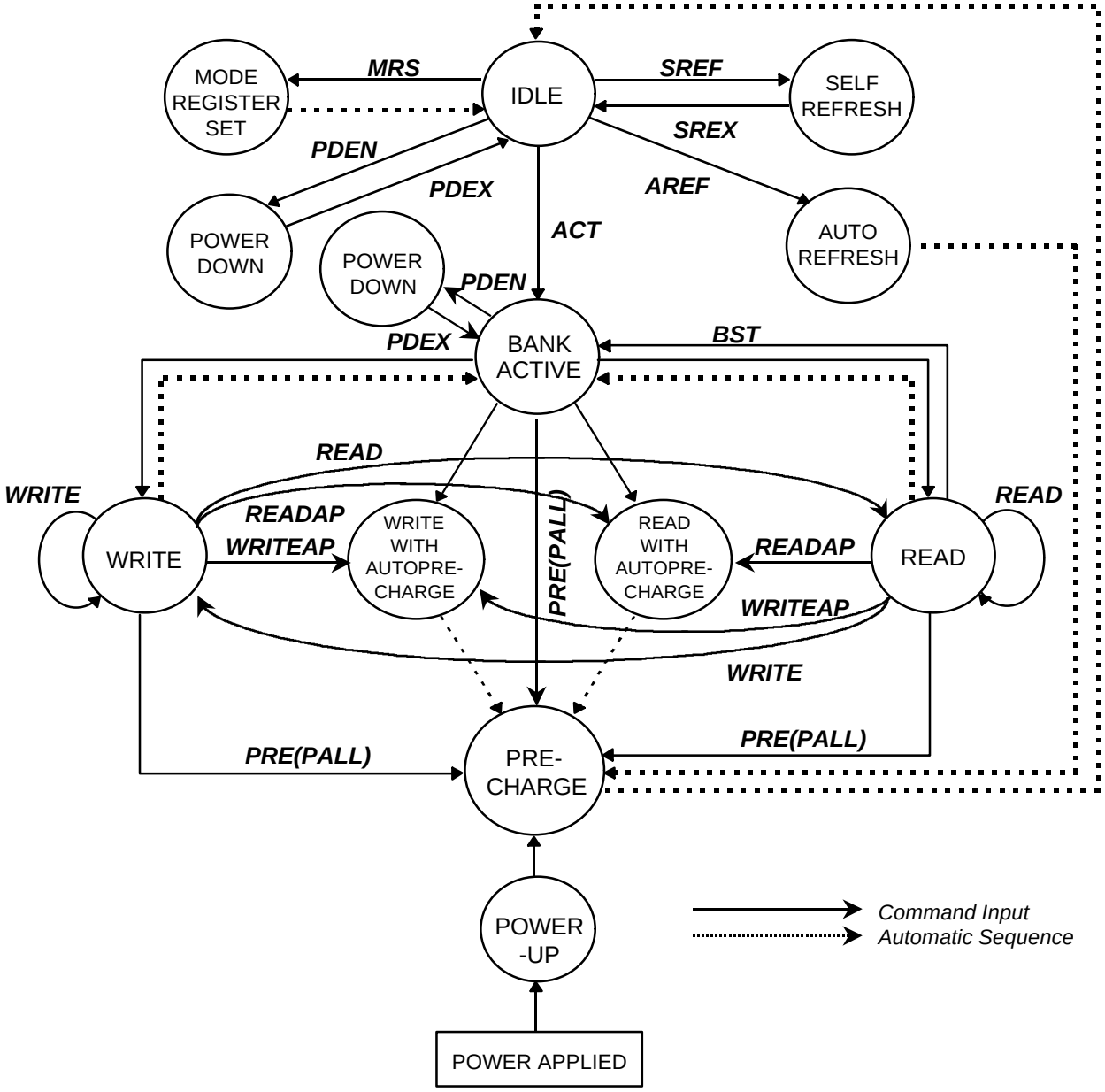
*3. Illegal if CLK is suspended or stopped during the power down mode*

*4. Self refresh can be entered only from the all banks idle state*

*5. Disabling CLK may cause malfunction if any bank is in active state*

# *HYUNDAI 4 Banks X 4/2/1M X 4/8/16 bits DDR SDRAM*

## SIMPLIFIED STATE DIAGRAM



# *HYUNDAI 4 Banks X 4/2/1M X 4/8/16 bits DDR SDRAM*

## MODE REGISTER TABLE

The mode register of DDR SDRAM provides a variety of different options. The mode register can be programmed by the Mode Register Set(MRS) command. Once mode register field is determined, the information will be held until resetted by another MRS command.

| BA0 | BA1 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | RFU* | | | DR* | TM* | CAS Latency(CL) | | | BT* | Burst Length(BL) | | |

**BT=Burst Type, TM=Test Mode, DR=DLL Reset, RFU=Reserved for Future Use*
***RFU Address fields (A11,A10, A9) must be "0" during MRS entry***

| A8 | DLL Reset |
|---|---|
| 0 | No |
| 1 | Yes |

| A7 | Test Mode |
|---|---|
| 0 | Normal Operation |
| 1 | Test Mode Entry |

| A3 | Burst Type |
|---|---|
| 0 | Sequential |
| 1 | Interleave |

| A6 | A5 | A4 | CAS Latency |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | 2.0 |
| 0 | 1 | 1 | Reserved |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | 1.5 |
| 1 | 1 | 0 | 2.5 |
| 1 | 1 | 1 | Reserved |

| A2 | A1 | A0 | Sequential | Interleave |
|---|---|---|---|---|
| 0 | 0 | 0 | Reserved | Reserved |
| 0 | 0 | 1 | 2 | 2 |
| 0 | 1 | 0 | 4 | 4 |
| 0 | 1 | 1 | 8 | 8 |
| 1 | 0 | 0 | Reserved | Reserved |
| 1 | 0 | 1 | Reserved | Reserved |
| 1 | 1 | 0 | Reserved | Reserved |
| 1 | 1 | 1 | Reserved | Reserved |

## EXTENDED MODE REGISTER TABLE

| BA0 | BA1 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | RFU* | | | | | | | | | | | DLL* |

** DLL=DLL Enable/Disable, A0=0(DLL Enable), A0=1(DLL Disable) - refer to page 17 for details, field for BA=1 is still reserved*

## BURST SEQUENCE TABLE

The burst type can be determined either sequential or interleave by MRS command. DDR SDRAM provides any starting address for bursting read and write data as SDR SDRAM.

| Start Address | Sequential | Interleave |
|---|---|---|
| A0=0 | 0,1 | 0, 1 |
| A0=1 | 1,0 | 1, 0 |
| A1=0, A0=0 | 0, 1, 2, 3 | 0, 1, 2, 3 |
| A1=0, A0=1 | 1, 2, 3, 0 | 1, 0, 3, 2 |
| A1=1, A0=0 | 2, 3, 0, 1 | 2, 3, 0, 1 |
| A1=1, A0=1 | 3, 0, 1, 2 | 3, 2, 1, 0 |
| A2=0, A1=0, A0=0 | 0, 1, 2, 3, 4, 5, 6, 7 | 0, 1, 2, 3, 4, 5, 6, 7 |
| A2=0, A1=0, A0=1 | 1, 2, 3, 4, 5, 6, 7, 0 | 1, 0, 3, 2, 5, 4, 7, 6 |
| A2=0, A1=1, A0=0 | 2, 3, 4, 5, 6, 7, 0, 1 | 2, 3, 0, 1, 6, 7, 4, 5 |
| A2=0, A1=1, A0=1 | 3, 4, 5, 6, 7, 0, 1, 2 | 3, 2, 1, 0, 7, 6, 5, 4 |
| A2=1, A1=0, A0=0 | 4, 5, 6, 7, 0, 1, 2, 3 | 4, 5, 6, 7, 0, 1, 2, 3 |
| A2=1, A1=0, A0=1 | 5, 6, 7, 0, 1, 2, 3, 4 | 5, 4, 7, 6, 1, 0, 3, 2 |
| A2=1, A1=1, A0=0 | 6, 7, 0, 1, 2, 3, 4, 5 | 6, 7, 4, 5, 2, 3, 0, 1 |
| A2=1, A1=1, A0=1 | 7, 0, 1, 2, 3, 4, 5, 6 | 7, 6, 5, 4, 3, 2, 1, 0 |

# *HYUNDAI 4 Banks X 4/2/1M X 4/8/16 bits DDR SDRAM*

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $T_A$ | Ambient temperature | 0 ~ 70 | °C |
| $T_{STG}$ | Storage temperature | -55 ~ 125 | °C |
| $V_{IN}$, $V_{OUT}$ | Voltage on any pin relative to $V_{SS}$ | -0.5 ~ 3.6 | Volts |
| $V_{DD}$ | Voltage on $V_{DD}$ relative to $V_{SS}$ | -1.0 ~ 4.6 | Volts |
| $V_{DDQ}$ | Voltage on $V_{DDQ}$ relative to $V_{SS}$ | -0.5 ~ 3.6 | Volts |
| $I_{OS}$ | Output short circuit current | 50 | mA |
| $P_D$ | Power dissipation | 1 | W |
| $T_{SOLDER}$ | Soldering temperature X time | 260 X10 | °C X sec |

*Notes : Operation other than above table can adversely affect the device reliability*

## RECOMMENDED DC OPERATING CONDITIONS

( $T_A$ = 0 to 70 °C)

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Power supply voltage | 3.0 | 3.3 | 3.6 | Volts |
| $V_{DDQ}$[1] | Power supply voltage | 2.3 | 2.5 | 2.7 | Volts |
| $V_{SS}$, $V_{SSQ}$ | Power supply voltage | 0 | 0 | 0 | Volts |
| $V_{IL}$(DC)[2] | Input DC low voltage | -0.3 | - | $V_{REF}$ - 0.18 | Volts |
| $V_{IH}$(DC) | Input DC high voltage | $V_{REF}$ + 0.18 | - | $V_{DDQ}$ + 0.3 | Volts |
| $V_{IL}$(AC) | Input AC low voltage | - | - | $V_{REF}$ - 0.35 | Volts |
| $V_{IH}$(AC) | Input AC high voltage | $V_{REF}$ + 0.35 | - | - | Volts |
| $V_{OL}$[3] | Output low voltage | - | - | $V_{TT}$ - 0.76 | Volts |
| $V_{OH}$[4] | Output high voltage | $V_{TT}$ + 0.76 | - | - | Volts |
| $V_{TT}$ | Termination voltage | $V_{REF}$ - 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 | Volts |
| $V_{REF}$[5] | Reference voltage | 1.15 | 1.25 | 1.35 | Volts |
| $R_T$ | Termination resistor | - | 50 | - | Ohms |
| $R_S$ | Series resistor | - | 25 | - | Ohms |

*Notes : 1. $V_{DDQ}$ must not exceed the level of $V_{DD}$*
*2. $V_{IL,min}$ (AC) = -1.5V (pulse width < 5ns)*
*3. $I_{OL}$ =15.2mA, 4. $I_{OH}$ = -15.2mA*
*5. The value of $V_{REF}$ is approximately equal to 0.5$V_{DDQ}$*

## CAPACITANCE

( $T_A$ = 25 °C, f = 1MHz)

| Symbol | Parameter | Pin | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | Addresses, all inputs | 2.5 | 3.5 | pF |
| $C_{CLK}$ | Clock capacitance | CLK, /CLK | 2.5 | 3.5 | pF |
| $C_{IO}$ | I/O capacitance | DQ0 - DQ15, DQS, DM | 4.0 | 5.5 | pF |

# *HYUNDAI 4 Banks X 4/2/1M X 4/8/16 bits DDR SDRAM*

## DC CHARACTERISTICS

| Symbol | Parameter | Test Condition | Maximum | Unit |
|---|---|---|---|---|
| $I_{LI}$ | Input leakage current | $V_{applied}$=0 to 3.6V w/ all other pins=0V | 5 | uA |
| $I_{LO}$ | Output leakage current | $V_{applied}$=0 to 2.7V w/ $D_{OUT}$ is disabled | 5 | uA |
| $I_{CC1}$ | Operating current | No CAS activity, 1 bank active<br>$t_{RC}$=minimum cycle | 120 | mA |
| $I_{CC2N}$ | Precharge standby current<br>( Non-power down mode ) | CKE ≥ $V_{IH(min)}$ in all banks idle state<br>$t_{CK}$=minimum cycle | 40 | mA |
| $I_{CC2P}$ | Precharge standby current<br>( Power down mode ) | CKE ≤ $V_{IL(max)}$ in all banks idle state<br>$t_{CK}$=minimum cycle | 20 | mA |
| $I_{CC3N}$ | Active standby current<br>( Non-power down mode ) | CKE ≥ $V_{IH(min)}$ in all banks active state<br>$t_{CK}$=minimum cycle | 50 | mA |
| $I_{CC3P}$ | Active standby current<br>( Power down mode ) | CKE ≤ $V_{IL(max)}$ in all banks active state<br>$t_{CK}$=minimum cycle | 25 | mA |
| $I_{CC4}$ | Burst operating current | With CAS activity, $t_{CK}$=minimum cycle | 180 | mA |
| $I_{CC5}$ | Refresh current | $t_{RC}$=minimum cycle<br>with auto refresh mode | 200 | mA |
| $I_{CC6}$ | Self refresh current | CKE ≤ 0.2V at self refresh mode | 2 | mA |

## AC CHARACTERISTICS I - TIMING

| Symbol | Parameter | | - 7.5 | | - 8 | | - 10 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{CK}$ | Clock cycle time | CL=1.5 | - | - | - | - | 12 | 15 | ns |
| | | CL=2.0 | 8 | 15 | 10 | 15 | 10 | 15 | ns |
| | | CL=2.5 | 7.5 | 15 | 7.5 | 15 | 8 | 15 | ns |
| $r_D$ | Maximum data rate | | - | 266 | - | 250 | - | 200 | Mb/s |
| $t_{CH}$ | Clock high level width | | 0.45 | - | 0.45 | - | 0.45 | - | $t_{CK}$ |
| $t_{CL}$ | Clock low level width | | 0.45 | - | 0.45 | - | 0.45 | - | $t_{CK}$ |
| $t_{AC}$ | DQ edge to clock edge skew | | - 0.1 | 0.1 | - 0.1 | 0.1 | - 0.1 | 0.1 | $t_{CK}$ |
| $t_{DQSCK}$ | DQS edge to clock edge skew | | - 0.1 | 0.1 | - 0.1 | 0.1 | - 0.1 | 0.1 | $t_{CK}$ |
| $t_{DQCK}$ | DQ edge to clock edge skew | | - 0.1 | 0.1 | - 0.1 | 0.1 | - 0.1 | 0.1 | $t_{CK}$ |
| $t_{DQSQ}$ | DQS edge to DQ edge skew | | - 0.075 | 0.075 | - 0.075 | 0.075 | - 0.075 | 0.075 | $t_{CK}$ |
| $t_{HZQ}$ | DQ output Lo-Z to Hi-Z delay | | - | 3 | - | 3 | - | 4 | ns |

# *HYUNDAI 4 Banks X 4/2/1M X 4/8/16 bits DDR SDRAM*

## AC CHARACTERISTICS I - TIMING

| Symbol | Parameter | - 7.5 | | - 8 | | - 10 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{DV}$ | Data valid window | 0.35 | - | 0.35 | - | 0.35 | - | $t_{CK}$ |
| $t_{DQSV}$ | Data strobe valid window | 0.35 | - | 0.35 | - | 0.35 | - | $t_{CK}$ |
| $t_{RPRE}$ | Read DQS preamble time | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | $t_{CK}$ |
| $t_{RPST}$ | Read DQS postamble time | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | $t_{CK}$ |
| $t_{WPRES}$ | Write DQS preamble setup time | 0 | - | 0 | - | 0 | - | $t_{CK}$ |
| $t_{WPREH}$ | Write DQS preamble hold time | 0.25 | - | 0.25 | - | 0.25 | - | $t_{CK}$ |
| $t_{WPST}$ | DQS last falling edge to Hi-Z | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | $t_{CK}$ |
| $t_{DQSS}$ | CLK to first rising edge of DQS | 0.75 | 1.25 | 0.75 | 1.25 | 0.75 | 1.25 | $t_{CK}$ |
| $t_{IS}$[1] | Input setup time to clock | 0.15 | - | 0.15 | - | 0.15 | - | $t_{CK}$ |
| $t_{IH}$[1] | Input hold time to clock | 0.15 | - | 0.15 | - | 0.15 | - | $t_{CK}$ |
| $t_{DDQSS}$[2] | DQ setup time to DQS | 0.075 | - | 0.075 | - | 0.075 | - | $t_{CK}$ |
| $t_{DDQSH}$[2] | DQ hold time to DQS | 0.075 | - | 0.075 | - | 0.075 | - | $t_{CK}$ |
| $t_{DMDQSS}$[2] | DM setup time to DQS | 0.075 | - | 0.075 | - | 0.075 | - | $t_{CK}$ |
| $t_{DMDQSH}$[2] | DM hold time to DQS | 0.075 | - | 0.075 | - | 0.075 | - | $t_{CK}$ |
| $t_{DRL}$ | Last data-in to read command | 1 | - | 1 | - | 1 | - | $t_{CK}$ |
| $t_{DPL}$ | Last data-in to precharge | 10 | - | 10 | - | 10 | - | ns |
| $t_{RAS}$ | RAS active time | 45 | 100K | 48 | 100K | 50 | 100K | ns |
| $t_{RP}$ | RAS precharge time | 15 | - | 15 | - | 20 | - | ns |
| $t_{RC}$ | RAS cycle time | 60 | - | 63 | - | 70 | - | ns |
| $t_{RFC}$ | Auto-refresh command cycle | 75 | - | 80 | - | 80 | - | ns |
| $t_{RCD}$ | RAS to CAS delay | 15/20 | - | 15/20 | - | 20 | - | ns |
| $t_{RRD}$ | RAS to RAS delay | 2 | - | 2 | - | 2 | - | $t_{CK}$ |
| $t_{CCD}$ | CAS to CAS delay | 1 | - | 1 | - | 1 | - | $t_{CK}$ |
| $t_{MRD}$ | Mode register set delay | 2 | - | 2 | - | 2 | - | $t_{CK}$ |
| $t_{PDEX}$ | Power down exit time | 10 | - | 10 | - | 10 | - | ns |
| $t_{SREX}$ | Self-refresh exit time | 200 | - | 200 | - | 200 | - | ns |
| $t_{T}$ | Input transition time | 0.5 | - | 0.5 | - | 0.5 | - | ns |
| $t_{REF}$ | Refresh time | - | 64 | - | 64 | - | 64 | ms |

*Notes :*
*1. Data sampled at the rising edge of the clock : Addresses, CKE, /CS, /RAS, /CAS, /WE*
*2. Data sampled at both the rising edge and falling edge of data strobe : DQ, DM*
*3. tRCD=15ns/20ns each one represents different parts*

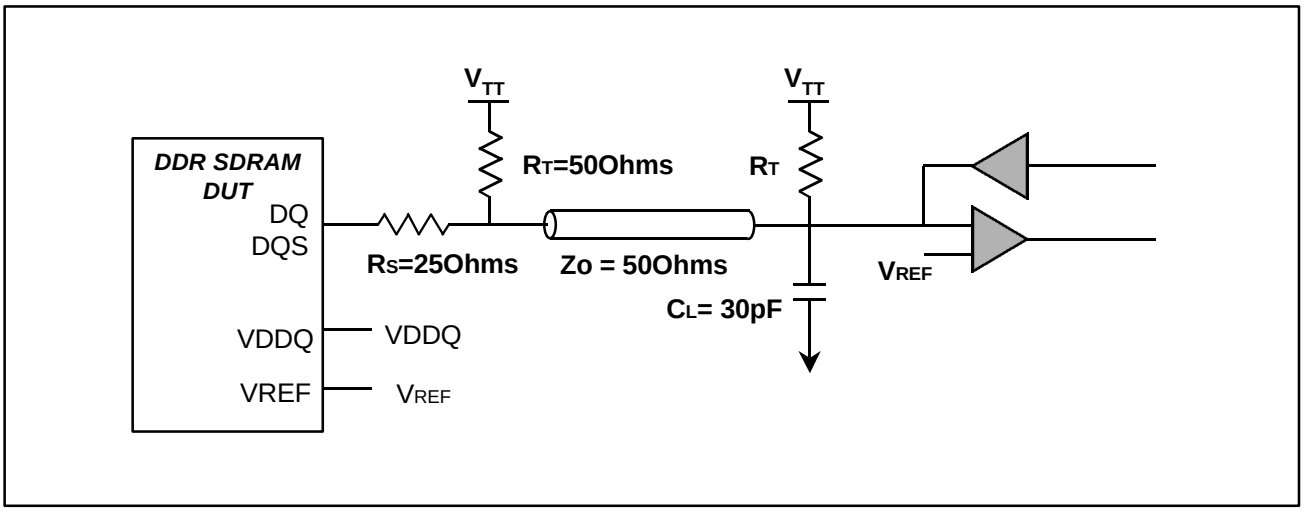
# *HYUNDAI 4 Banks X 4/2/1M X 4/8/16 bits DDR SDRAM*

## AC CHARACTERISTICS II - TEST LOAD

( $V_{DD}$=3.3V, $V_{DDQ}$=2.5V, $T_A$ = 0~70 °C)

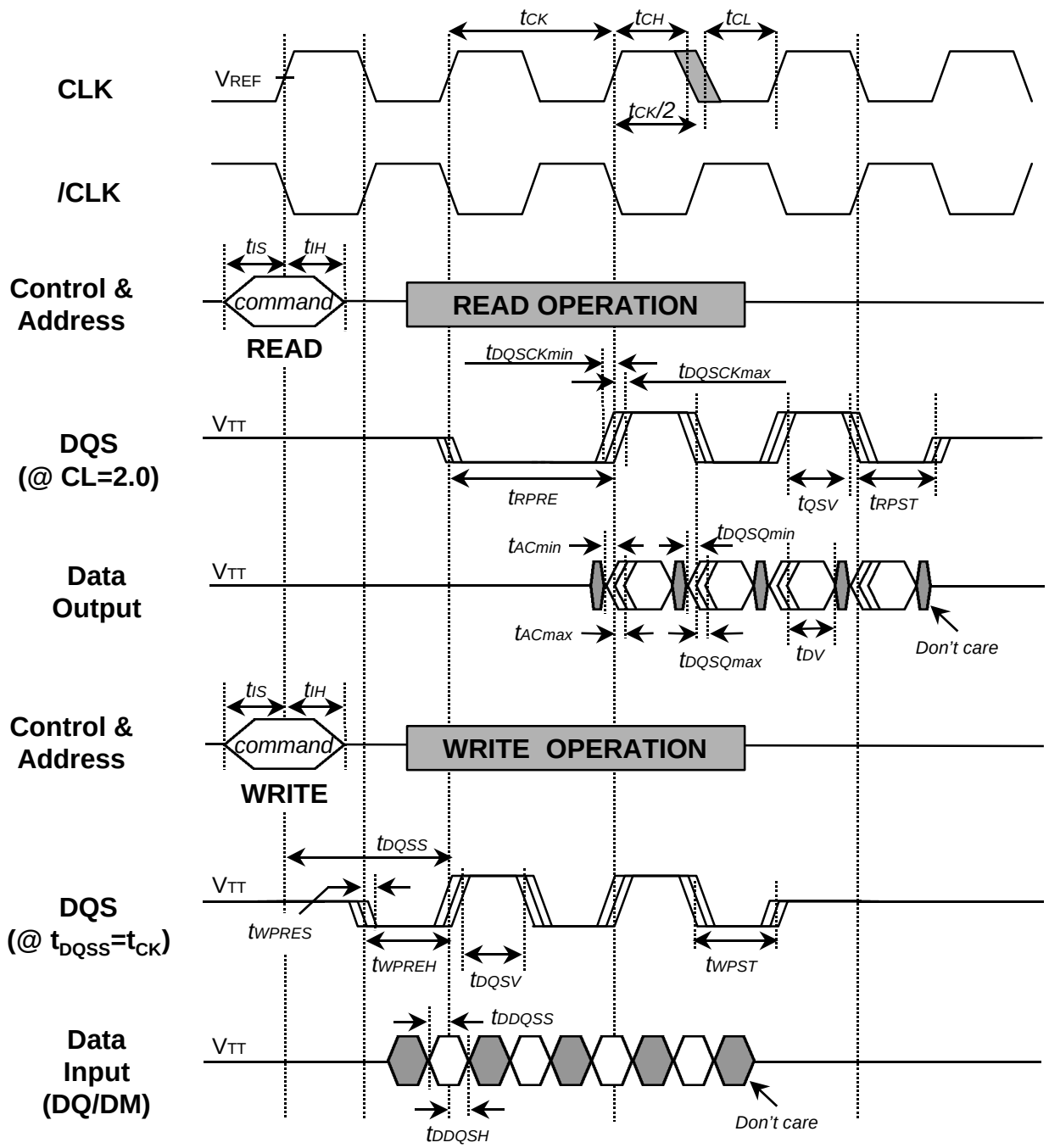
| Parameter | Condition | Unit |
|---|---|---|
| Reference voltage, $V_{REF}$ | $V_{DDQ}$ x 0.5 | Volts |
| Termination voltage, $V_{TT}$ | $V_{DDQ}$ x 0.5 | Volts |
| Timing measurement reference level | $V_{REF}$ | Volts |
| Input signal level | 0.4 / 2.4 | Volts |
| Input signal slew rate | 1 | V/ns |
| Output load | See test load circuits below | - |

## AC CHARACTERISTICS III - REFERENCE TEST LOAD CIRCUITS



# *HYUNDAI 4 Banks X 4/2/1M X 4/8/16 bits DDR SDRAM*

## AC CHARACTERISTICS IV - TIMING DIAGRAM




**Notes** : CAS Latency (CL) is defined as the number of ticks of clock from the rising edge of the command CLK to the first edge of DQS which transits from low to high level.

# *HYUNDAI 4 Banks X 4/2/1M X 4/8/16 bits DDR SDRAM*

## PACKAGE INFORMATION

**Unit : mm(inch)**