

OKI Semiconductor

MSM6255

DOT MATRIX LCD CONTROLLER

GENERAL DESCRIPTION

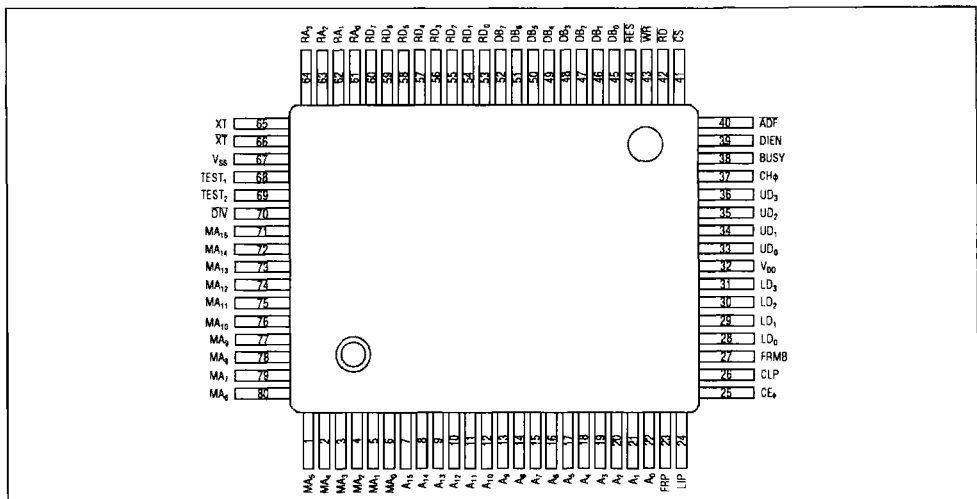
The MSM6255GS is a CMOS si-gate LSI designed to display characters and graphics on a DOT MATRIX LCD panels in characters and graphics.

FEATURES

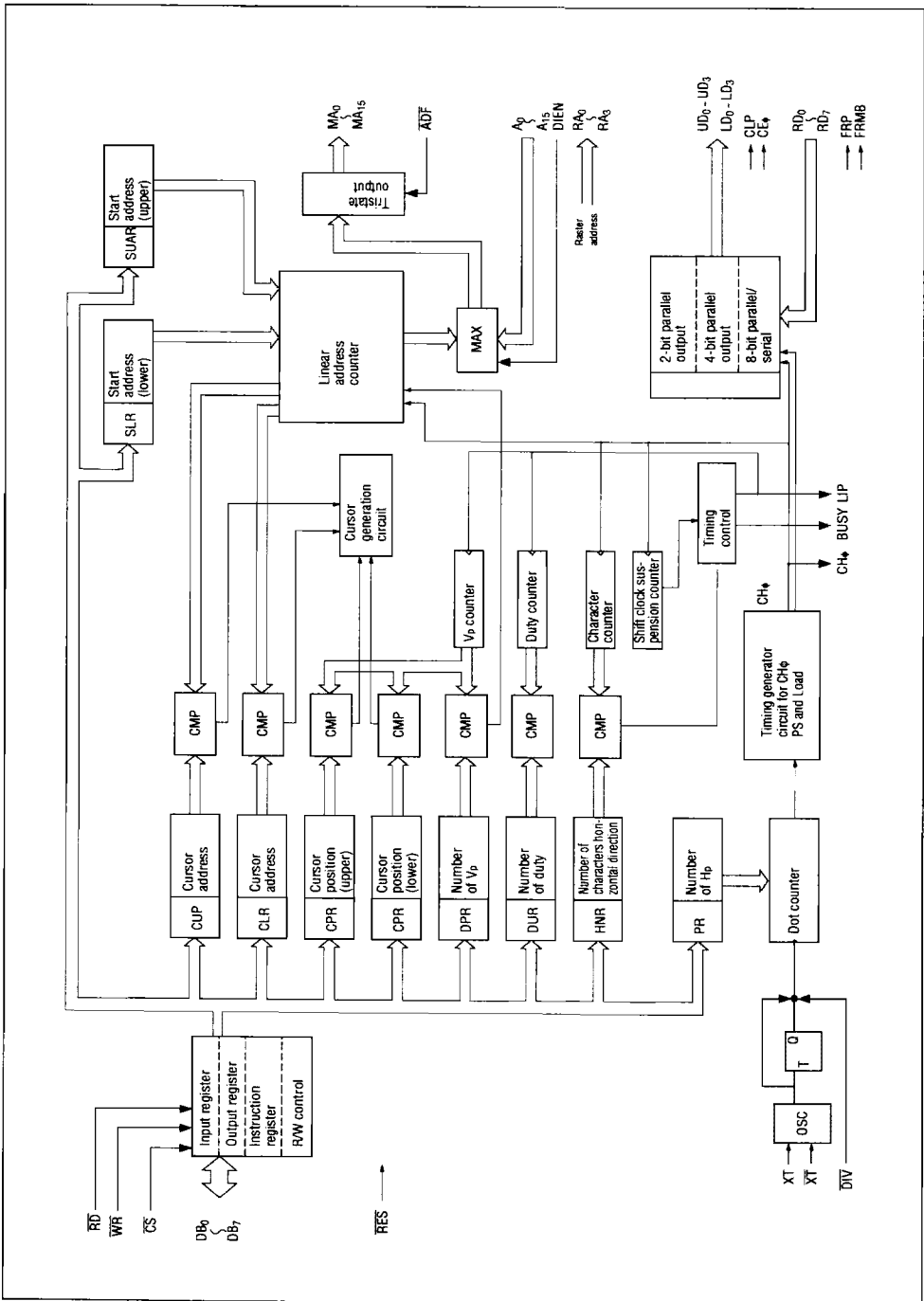
- Display control capacity
 - Graphic mode : 512,000 dots (2¹⁶ bytes)
Memory address MA₀ ~ MA₁₅
 - Character mode: 65,536 characters (2¹⁶ bytes)
Display address MA₀ ~ MA₁₅
- Direct interface with 8085 or Z80 CPU
- Duty: 1/2 to 1/256 selectable
- Attributes
 - Screen clear
 - Cursor ON/OFF/blink
- Scrolling and paging
- Display system: AC inversion at each frame
- Data output (upper and lower display outputs)
 - 4-bit parallel output, 2-bit parallel output, 1-bit serial output
- Crystal oscillation
- Low C-MOS Silicon gate process
- Single +5V power supply
- 80 pin plastic QFP (QFP80-P-1420-K)
- 80 pin -V1 plastic QFP (QFP80-P-1420-V1K)

PIN CONFIGURATION

(Top view) 80 pin plastic QFP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Limits	Unit
Supply voltage	V_{DD}	$T_a = 25^\circ\text{C}$	-0.3 ~ 6	V
Input voltage	V_{IN}	$T_a = 25^\circ\text{C}$	-0.3 ~ V_{DD}	V
Storage temperature	T_{stg}	-	-50 ~ 150	$^\circ\text{C}$

OPERATING RANGE

Parameter	Symbol	Condition	Limits	Unit
Supply voltage	V_{DD}	-	4.5 ~ 5.5	V
Operating temperature	T_{OP}	-	-20 ~ 85	$^\circ\text{C}$
Operating frequency	f_{osc}	$V_{DD} = 5V \pm 10\%$	0 ~ 11	MHz

INPUT CHARACTERISTICS

($V_{DD} = 5V \pm 5\%$, $T_a = -20 \sim 85^\circ\text{C}$)

Parameter	Symbol	MIN	TYP	MAX	Unit	Applicable pin
"H" input voltage	V_{IH}	2.4	-	-	V	DB ₀ ~ DB ₇ , $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, A ₀ ~ A ₁₅ , DIEN, ADF, RD ₀ ~ RD ₇
"L" input voltage	V_{IL}	-	-	0.7	V	
"H" input voltage	V_{IH}	4.5	-	-	V	$\overline{\text{RES}}$, $\overline{\text{DIV}}$, XT
"L" input voltage	V_{IL}	-	-	1.0	V	
"H" input voltage	I_{IH}	-	-	1	μA	DB ₀ ~ DB ₇ , $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WA}}$, A ₀ ~ A ₁₅ , DIEN, $\overline{\text{ADF}}$, RD ₀ ~ RD ₇ , $\overline{\text{RES}}$, $\overline{\text{DIV}}$
"L" input voltage	I_{IL}	-	-	-1	μA	
"H" input voltage	I_{IH}	-	-	250	μA	TEST1, TEST2
"L" input voltage	I_{IL}	-	-	-1	μA	

OUTPUT CHARACTERISTICS

($V_{DD} = 5V \pm 5\%$, $T_a = -20 \sim 85^\circ\text{C}$)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Applicable pin
"H" output current	I_{OH}	$V_{OH} = 2.8V$	-500	-	-	μA	LD ₀ ~ LD ₃ UD ₀ ~ UD ₃ MA ₀ ~ MA ₁₅ RA ₀ ~ RA ₃ CH ϕ , CE ϕ , LIP, FRP FRMB, BUSY, CLP DB ₀ ~ DB ₇
"L" output current	I_{OL}	$V_{OL} = 0.4V$	2.4	-	-	mA	

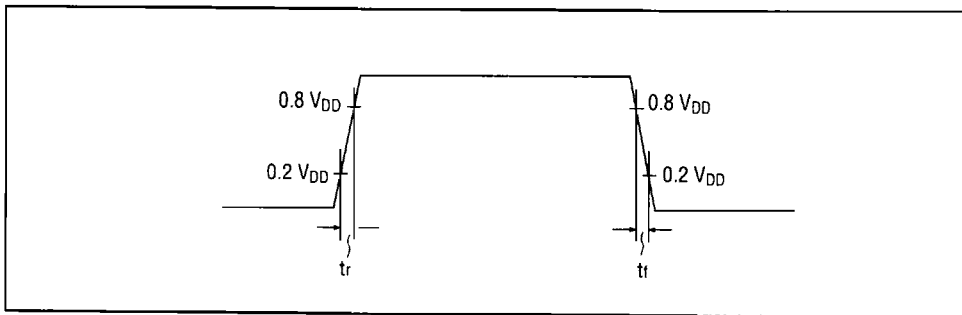
CURRENT CONSUMPTION

($V_{DD} = 5V \pm 5\%$, $T_a = -20 \sim 85^\circ C$)

Parameter	Symbol	V _{DD}	Condition	MIN	TYP	MAX	Unit
Static current	I _{DDs}	5	f _{osc} = 0 Hz, No load	-	-	50	μA
Dynamic current	I _{DD}	5	f _{osc} = 10 MHz, No load	-	-	15	mA

Note: TEST 1 and TEST2 are open, and other inputs are either V_{DD} or GND.

SWITCHING CHARACTERISTICS



($V_{DD} = 5V \pm 5\%$, $T_a = -20 \sim 85^\circ C$)

Parameter	Symbol	Load condition	MIN	TYP	MAX	Unit	Applicable pin
Rising time	t _r	60 pF	-	-	100	ns	All output pins
Falling time	t _f	60 pF	-	-	100	ns	

MAXIMUM OPERATING FREQUENCY

($V_{DD} = 5V \pm 5\%$, $T_a = -20 \sim 85^\circ C$)

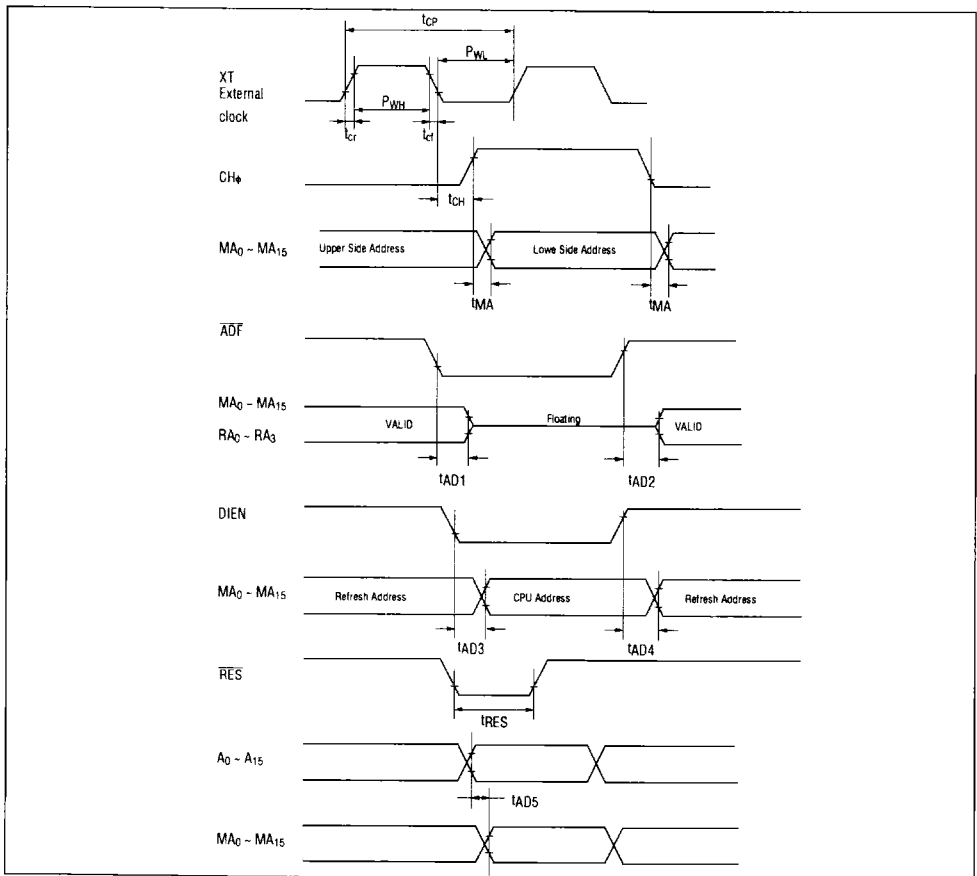
Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Notes
Oscillating frequency	f _{osc}	DIV = "L"	11	-	-	MHz	Crystal oscillator
Basic clock frequency	f _s	DIV = "H"	5.5	-	-	MHz	External clock

LCDC CONTROL SIGNAL TIMING CHARACTERISTICS

($C_L = 30\text{pF}$, $V_{DD} = 5V \pm 5\%$, $T_a = -20 \sim 85^\circ\text{C}$)

Parameter	Symbol	MIN	TYP	MAX	Unit
Clock cycle time	t_{CP}	180	-	-	ns
Clock "H" level pulse width	PWH	80	-	-	ns
Clock "L" level pulse width	PWL	80	-	-	ns
Clock rising/falling time	t_{cr}/t_{cf}	-	-	20	ns
Character clock delay time	t_{CH}	-	-	200	ns
Memory address clock delay time	t_{MA}	-	-	100	ns
Memory address disable delay time	t_{AD1}	-	-	40	ns
Memory address enable delay time	t_{AD2}	-	-	40	ns
CPU address delay time	t_{AD3}	-	-	100	ns
Refresh address delay time	t_{AD4}	-	-	100	ns
Reset "H" level pulse width	t_{RES}	1	-	-	μs
CPU address delay time	t_{AD5}	-	-	100	ns

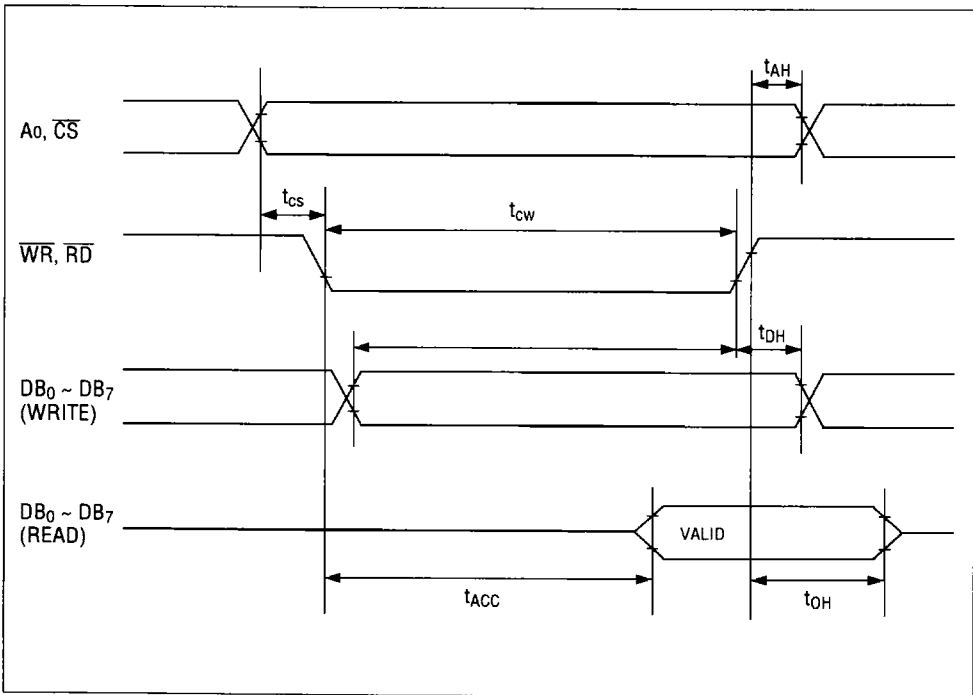
(Note) The values of t_{AD5} show when $DIEN=L$



BUS TIMING CHARACTERISTICS

($C_L = 50\text{pF}$, $V_{DD} = 5\text{V} \pm 5\%$, $T_a = -20 \sim 85^\circ\text{C}$)

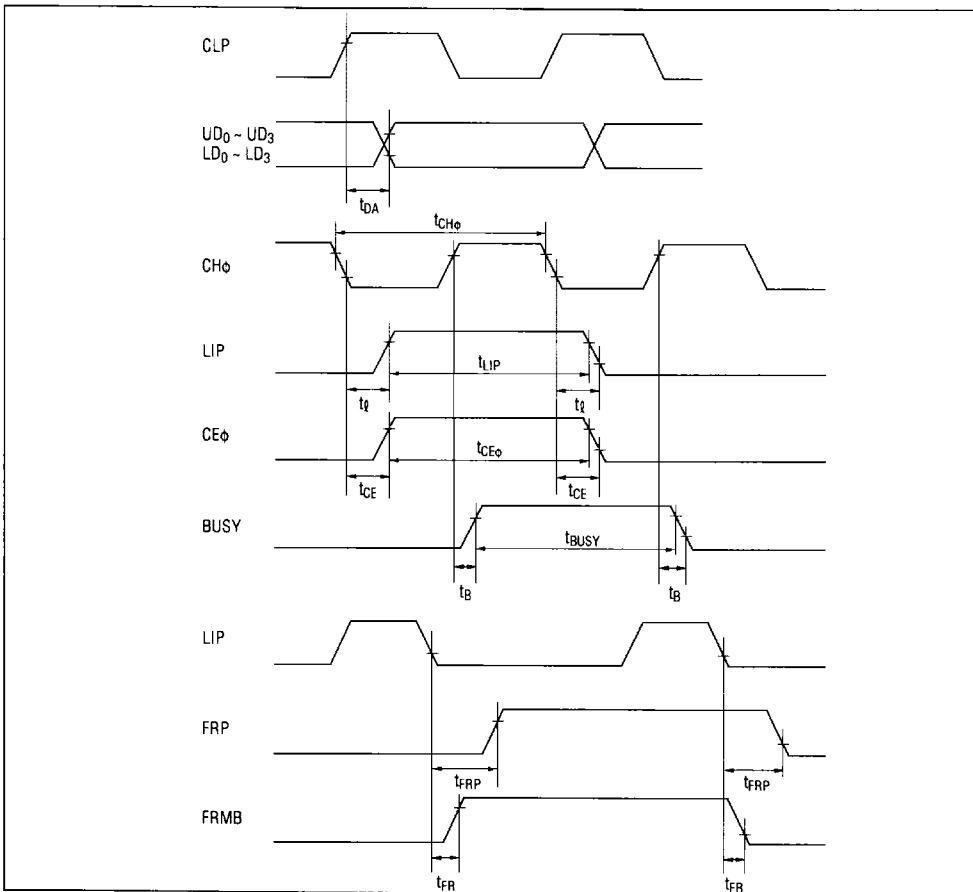
Parameter	Symbol	MIN	TYP	MAX	Unit
Ao, CS Set up time	t_{CS}	30	-	-	ns
RD, WR Pulse width	t_{CW}	250	-	-	ns
Address hold time	t_{AH}	10	-	-	ns
Data set-up time	t_{DS}	60	-	-	ns
Data hold time	t_{DH}	20	-	-	ns
Output disable time	t_{OH}	0	-	40	ns
Access time	t_{ACC}	-	-	200	ns



LCDC DRIVER INTERFACE TIMING CHARACTERISTICS

($C_L = 30\text{pF}$, $V_{DD} = 5\text{V} \pm 5\%$, $T_a = -20 \sim 85^\circ\text{C}$)

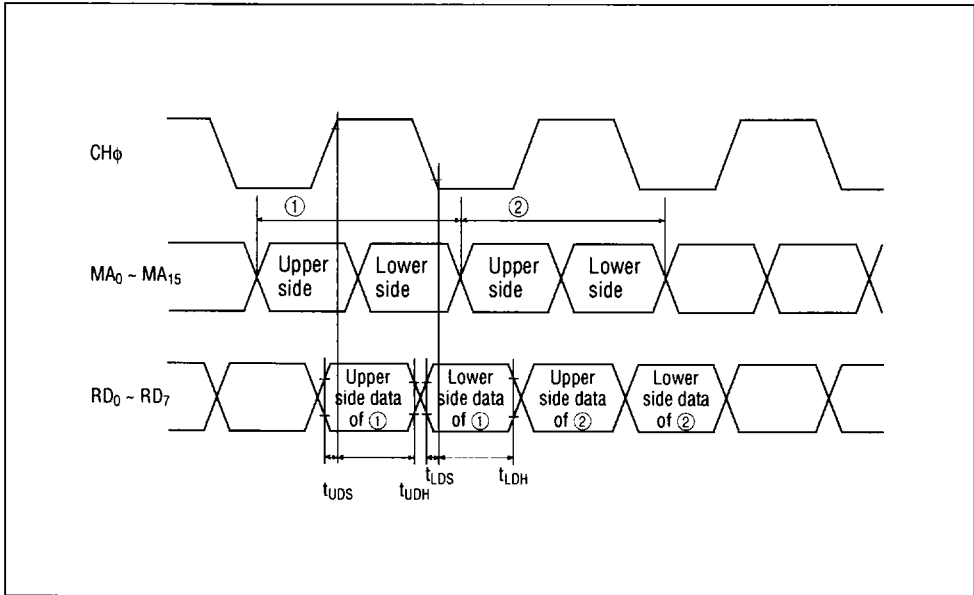
Parameter	Symbol	MIN	TYP	MAX	Unit
Data delay time	t_{DA}	-	-	100	ns
1 Character cycle time	$t_{CH\phi}$	730	-	-	ns
Latch signal delay time	t_l	-	-	200	ns
Latch signal "H" time	t_{LIP}	1.46	-	-	μs
Chip enable clock delay time	t_{CE}	-	-	200	ns
Chip enable clock "H" time	$t_{CE\phi}$	730	-	-	ns
Ready signal delay time	t_B	-	-	200	ns
Ready signal "H" time	t_{BUSY}	5.11	-	-	ns
Frame signal delay time	t_{FRP}	$2t_{CH\phi}$	-	$2t_{CH\phi} + 200$	ns
Alternating frame signal delay time	t_{FR}	-	-	200	ns



TIMING FOR FETCHING PATTERN DATA

($V_{DD} = 5V \pm 5\%$, $T_a = -20 \sim 85^\circ C$)

Parameter	Symbol	MIN	TYP	MAX	Unit
Upper side data set-up time	t_{UDS}	120	-	-	ns
Upper side data hold time	t_{UDH}	40	-	-	ns
Lower side set-up time	t_{LDS}	120	-	-	ns
Lower side data hold time	t_{LDH}	40	-	-	ns



PIN DESCRIPTION

Pin No.	Pin name	I/O/Z	Function
1 ~ 6	MA ₀	O/Z	Address output for displaying RAM.
71 ~ 22	MA ₁₅		
7	A ₀	I	Memory address input terminals
22	A ₁₅		
23	FRP	O	Frame signal . . . Synchronization of display
24	LIP	O	Display data latch signal
25	CE _φ	O	Chip enable clock for LCD segment driver
26	CLP	O	Display data shift clock
27	FRMB	O	AC signal
28	LD ₀	O	Display data parallel output for lower side
31	LD ₃		
32	V _{DD}		Supply voltage
33	UD ₀	O	Display data parallel output, Upper display 4-bit output (OD1, ED1, OD2 and ED2 outputs)
36	UD ₃		
37	CH _φ	O	
38	Busy	O	Ready state signal. This signal is used while serial transmission stops.
39	DIEN	I	Display enable signal. When this signal is H, display is enabled.
40	ADF	I	Address floating input. When this signal is L, MA ₀ ~ MA ₁₅ , RA ₀ ~ RA ₃ are high impedance. Whereas, it is H, A ₀ ~ A ₁₅ or a refresh address is output to MA ₀ ~ MA ₁₅ .
41	CS	I	Chip select.
42	RD	I	Read Reading data is valid when RD = L
43	WR	I	Write Data is written when WR = H
44	RES	I	Reset Resets each counter.
45	DB ₀	I/O/Z	8-bit data bus . . . Common terminal for three state I/O.
52	DB ₇		
53	RD ₀	I	ROM/RAM data input . . . Dot pattern data for the character generator
60	RD ₇		
61	RA ₀	O/Z	Raster address output. *This output is not used in the graphic mode.
64	RA ₃		
65	XT	I	X'tal osc When an external clock is used by setting DIV to "L", feeds it to XT.
66	X \bar{T}	O	
67	V _{SS}		Ground pin.
70	DIV	I	"H" : EXT clock "L" : Self oscillation

FUNCTIONAL DESCRIPTION

1. LCDC Internal Registers

The internal registers include one instruction register (IR) and nine data registers. (See Table 1).

Table 1 MSM6255GS Internal registers

\overline{CS}	Ao	Instruction register				Register	Register name	READ	WRITE	Data bit								
		3	2	1	0					7	6	5	4	3	2	1		
H	X	X	X	X	X		Invalid	-	-									
L	H	X	X	X	X	IR	Instruction register	○	○	X	X	X	X					
L	L	L	L	L	L	MOR	Mode control register	X	○	X								
L	L	L	L	L	L	PR	Character pitch register	○	○							X		
L	L	L	L	H	L	HNR	Horizontal character number register	○	○	X								
L	L	L	L	H	H	DVR	Duty number register	X	○									
L	L	L	H	L	L	CPR	Cursor form register	○	○									
L	L	L	H	L	H	SLR	Start address (lower) register	○	○									
L	L	L	H	H	L	SUR	Start address (upper) register	○	○									
L	L	L	H	H	L	SUR	Cursor address (lower) register	○	○									
L	L	H	L	L	L	CUR	Cursor address (upper) register	○	○									

Note: "L" is read if the data of the registers marked X is read.

- Instruction register

The instruction register is a register for specifying the address of the data register which is accessed.

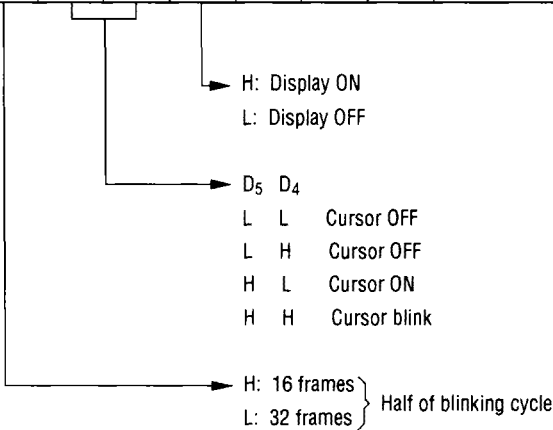
This register is cleared when \overline{RES} input is "L".

- Mode control register

The mode control register is specified by writing "00_H" in the instruction register.

Register	A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Instruction register	H	L	L	L	L	L	L	L	L
Mode control register	L	L	MODE DATA						

D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Output system	
H/L	H/L	H/L	H/L	L	L	L	1-bit serial	Character display
				H	L		2-bit parallel	
				X	H		4-bit parallel	
				X	H			
				L	L	H	1-bit serial	Graphics
				H	L		2-bit parallel	
				X	H		4-bit parallel	
				X	H			
Blink time	Cursor ON/OFF	Cursor blink	Display ON/OFF	2-bit parallel	4-bit parallel/ 1-bit serial	Mode		



- Character pitch register

Register	A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Instruction register	H	L	L	L	L	L	L	L	H
Character pitch register	L	(V _p - 1)				L	(H _p - 1)		

H_p represents the number of bits to be displayed among one byte display data sent from RAM. The value of H_p is the following five types.

H _p	D ₂	D ₁	D ₀
4	L	H	H
5	H	L	L
6	H	L	H
7	H	H	L
8	H	H	H

- Horizontal character number register

Register	A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Instruction register	H	L	L	L	L	L	L	H	L	
Character number register	L	L	(H _N - 1)							

Assuming that the total horizontal dot number of the display is η_H,

$$\eta_H = H_p \times H_N, \quad \text{where } H_N = 2 \sim 128.$$

The maximum value of η_H = 8 × 128 = 128 bytes = 1,024 dots.

- Duty number register

Register	A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Instruction register	H	L	L	L	L	L	L	H	H	
Time division register	L	(H _X - 1)								

$$N_x = 2 \sim 256$$

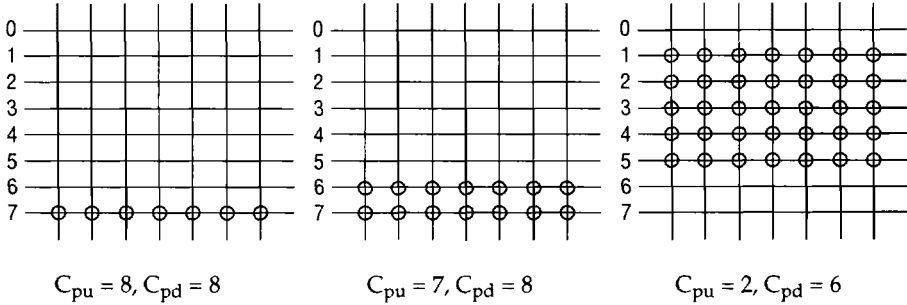
- Cursor form register

Register	A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Instruction register	H	L	L	L	L	L	H	L	L
Cursor position register	L	(C _{pu} - 1)				L	(C _{pd} - 1)		

The cursor is displayed on the lines from C_{pu} to C_{pd} in the character display mode. The length of the cursor in the horizontal direction is equal to the character pitch in the horizontal direction, H_p.

The cursor is not displayed in graphic mode. The relation between the cursor and V_p is as follows.

Font configuration of $H_p = 7$ and $V_p = 8$



- Note: (1) Setting of $C_{pu}, C_{pd} > V_p$ is not available.
- (2) The cursor signal and pattern data are displayed subject to EX-OR.

– Start address (lower) register

Register	A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Instruction register	H	L	L	L	L	L	H	L	H
Display start address register (lower byte)	L	Start address (lower)							

– Start address (upper) register

Register	A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Instruction register	H	L	L	L	L	L	H	H	L
Display start address register (upper byte)	L	Start address (upper)							

The display start address shows an address of the RAM which stores data displayed at the left end and the most upper position. The start address is composed of upper and lower 8 bits (16 bits in total).

– Cursor address (lower) register

Register	A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Instruction register	H	L	L	L	L	L	H	H	H
Cursor address register (lower byte)	L	Cursor address (lower)							

– Cursor address (upper) register

Register	A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Instruction register	H	L	L	L	L	H	L	L	H
Cursor address register (upper byte)	L	Cursor address (upper)							

By this instruction, the value of the cursor address is written in the cursor address register. The cursor is displayed at the position specified by the cursor address register.

2. LCD Display

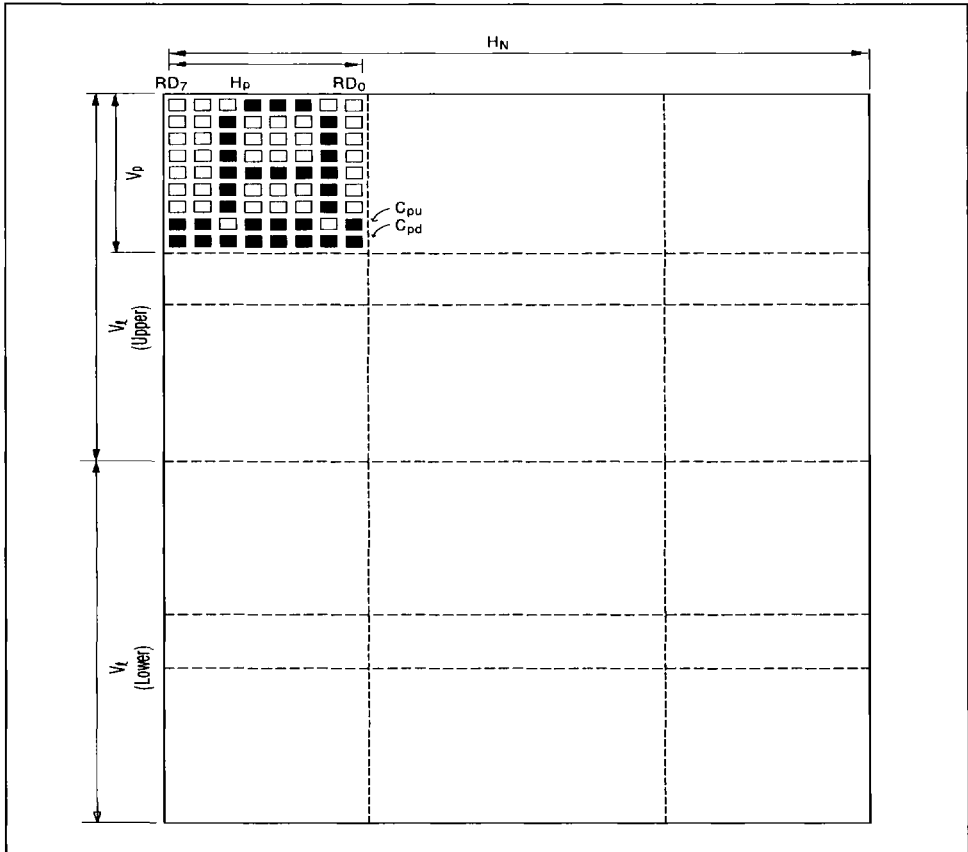


Table 2 Legend

Symbol	Name	Meaning	Value
H_p	Horizontal pitch	Pitch of characters in horizontal direction	4 ~ 8 dots
H_p	Vertical pitch	Pitch of characters in vertical direction	1 ~ 16 dots
H_N	Number of characters in one line	Number of characters per line or number of words per line	2 ~ 128 characters
V_q	Number of rows	Display duty	2 ~ 256
C_{pu}	Cursor start position	A position where the cursor starts display	Line 1 ~ 16
C_{pd}	Cursor end position	A position where the cursor stops display	Line 1 ~ 16

3. Built-in Bus Averter

The bus averter which switches the address buses $A_0 \sim A_{15}$ of the CPU with the memory address buses of the refresh. The refresh memory addresses are output to $MA_0 \sim MA_{15}$ when the input terminal of DIEN is set at high level and $A_0 \sim A_{15}$ are output to $MA_0 \sim MA_{15}$ when the input terminal of DIEN is set at low level.

4. External Clock Operation

An external clock enables the MSM6255GS to operate when the input terminal of \overline{DIV} is set at high level. The external clock is input to XT.

5. Address Output Floating

$MA_0 \sim MA_{15}$ and $RA_0 \sim RA_3$ become high impedance when the input terminal of \overline{ADF} is set at low level. This function is used when the address buses of memory are opened to others than $MA_0 \sim MA_{15}$. $MA_0 \sim MA_{15}$ and $RA_0 \sim RA_3$ become normal impedance when the input terminal of \overline{ADF} is set at high level.

6. Power Down Function

Power down function of the MSM5279GS (segment driver) can be used by connecting the output terminal of CE_0 to the ECLK input of the MSM5279GS. This function is valid only in 4-bit parallel output mode.

7. Refresh Memory Address

($MA_0 \sim MA_{15}$) Operation

In the horizontal direction, MA_{xx} is counted up at the trailing edge of CH_ϕ . Upper side is addressed while CH_ϕ is set at low level and lower side is addressed while CH_ϕ is set at high level.

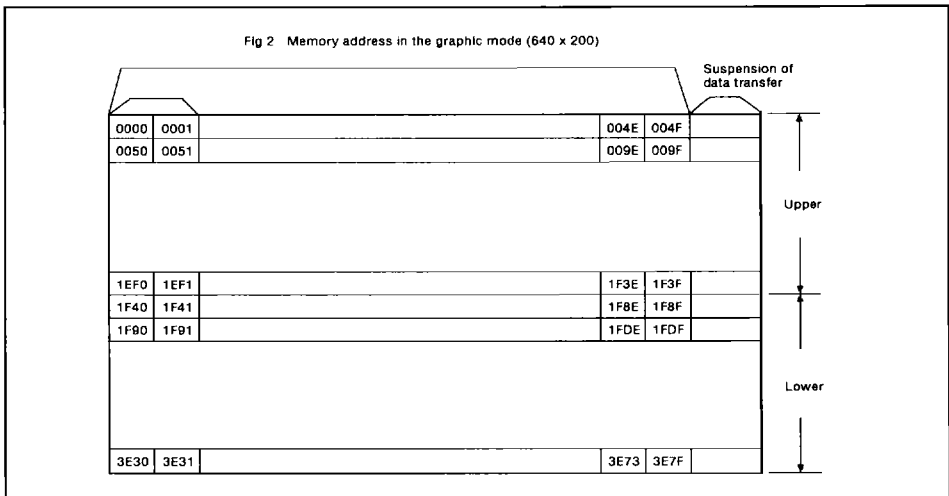
MA_{xx} is counted up even if it exceeds the number of horizontal display characters, but this does not affect the display since no data is being transferred at the time.

The period in which the data transfer is suspended corresponds to eight characters. When the period passes, one horizontal cycle is completed and the next cycle is commenced.

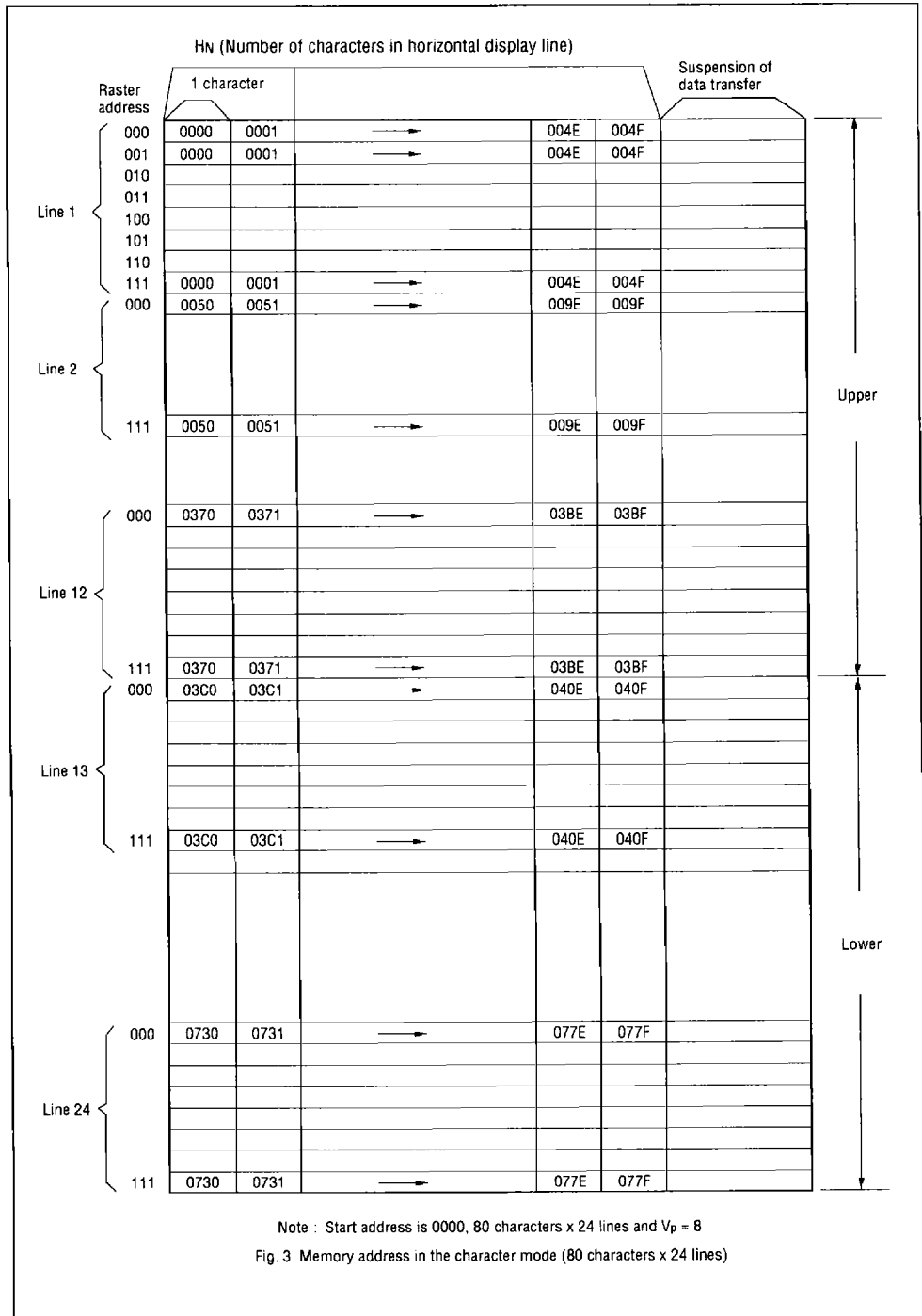
Memory address operation in the graphic mode is shown in Fig. 2 and that in the character mode is shown in Fig. 3.

Address configuration of display RAM

HSB														LSB	
MA ₁₅	MA ₁₄	MA ₁₃	MA ₁₂	MA ₁₁	MA ₁₀	MA ₉	MA ₈	MA ₇	MA ₆	MA ₅	MA ₄	MA ₃	MA ₂	MA ₁	MA ₀



Note: L is output for $RA_0 \sim RA_3$.



8. Output Mode

Three kinds of modes, 1-bit serial, 2-bit parallel and 4-bit parallel, are available as output modes. Data flow of each mode are shown below.

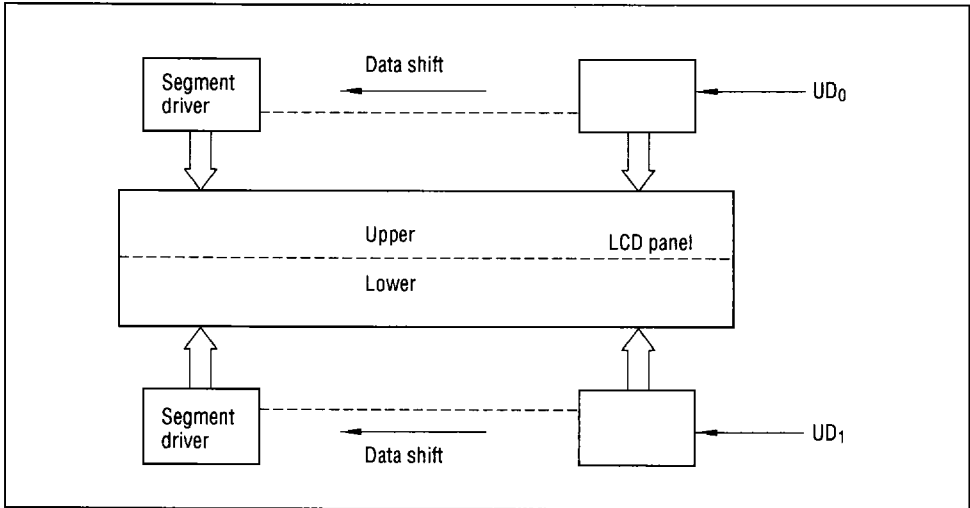


Fig. 4 1-bit serial data transfer

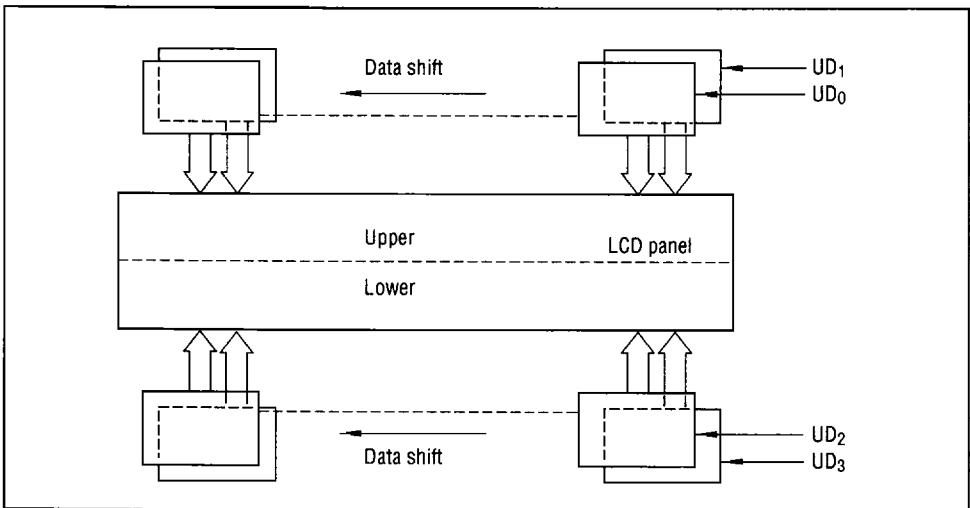


Fig. 5 2-bit parallel data transfer

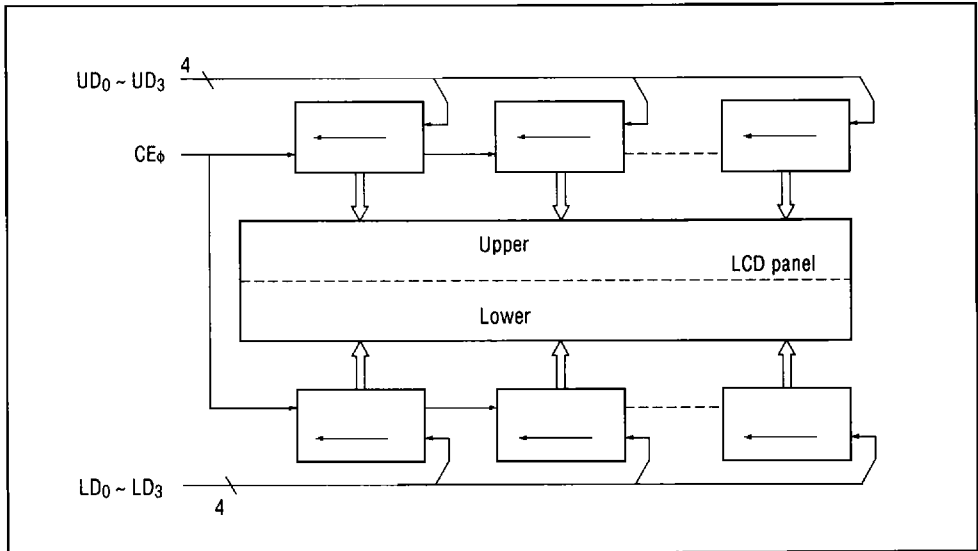


Fig. 6 4-bit parallel data transfer

Time charts corresponding to data transfers shown in Fig. 4 – Fig. 6 are shown in Fig 7 – Fig. 9.

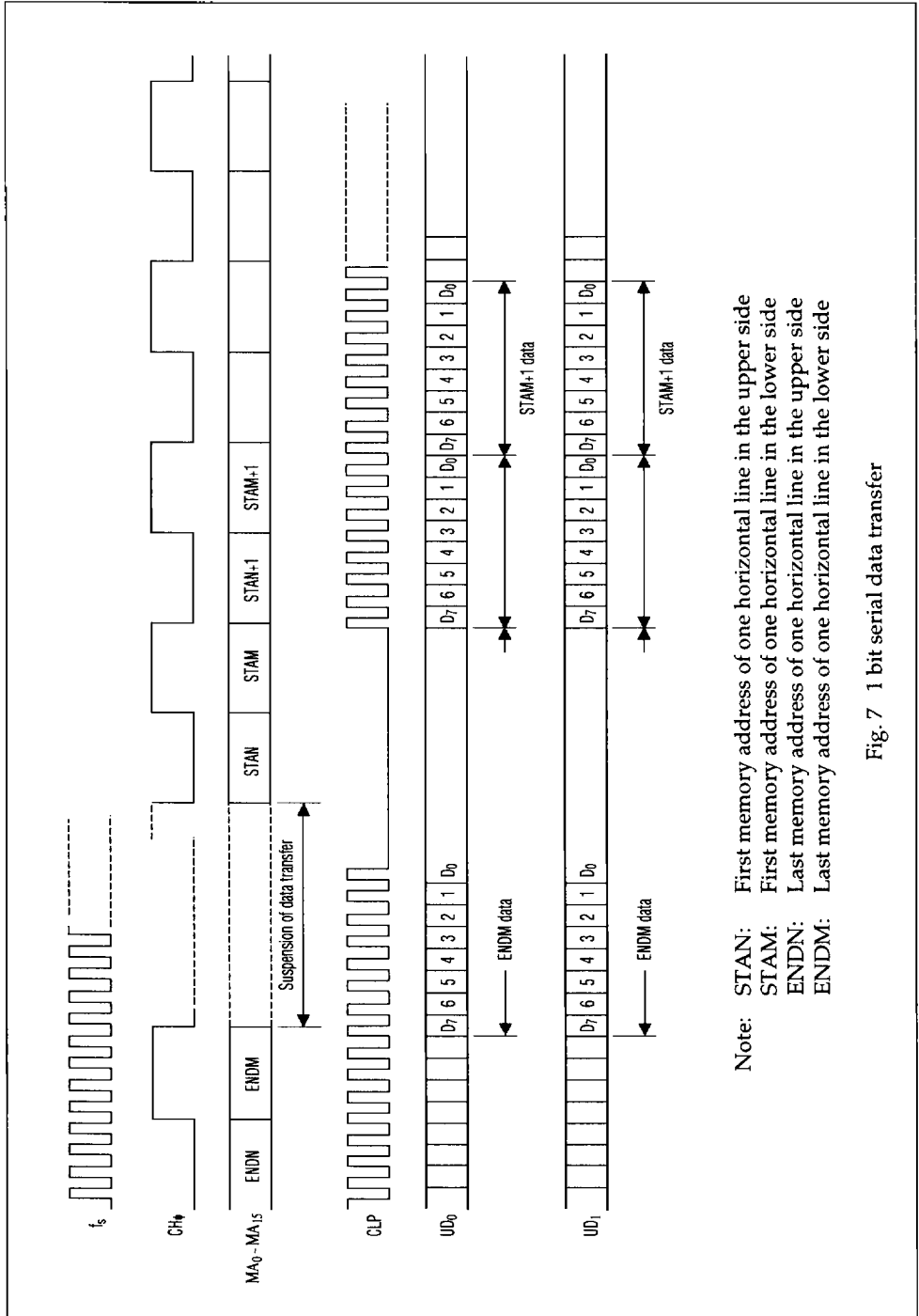
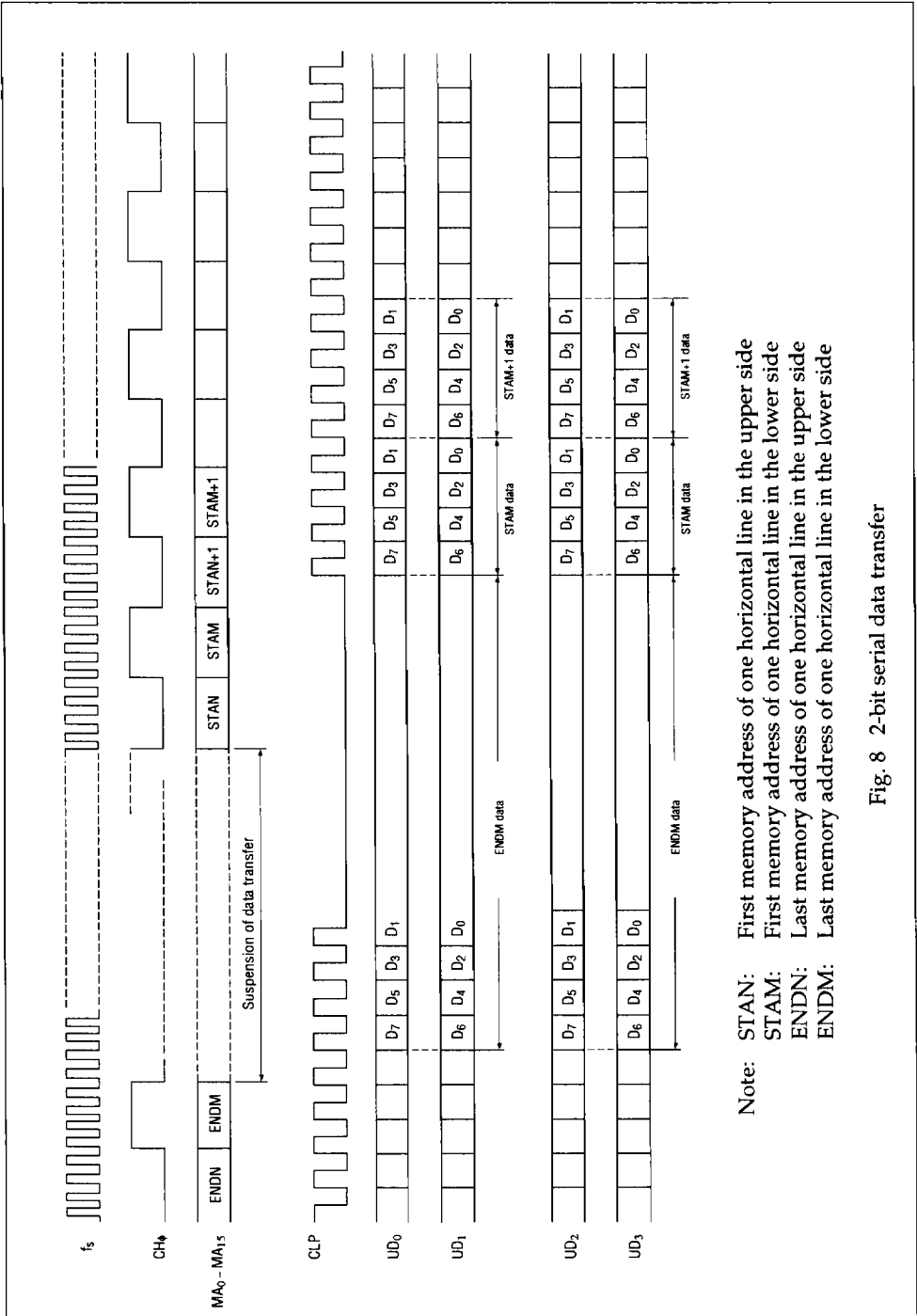


Fig. 7 1 bit serial data transfer



Note: STAN: First memory address of one horizontal line in the upper side
 STAM: First memory address of one horizontal line in the lower side
 ENDN: Last memory address of one horizontal line in the upper side
 ENDM: Last memory address of one horizontal line in the lower side

Fig. 8 2-bit serial data transfer

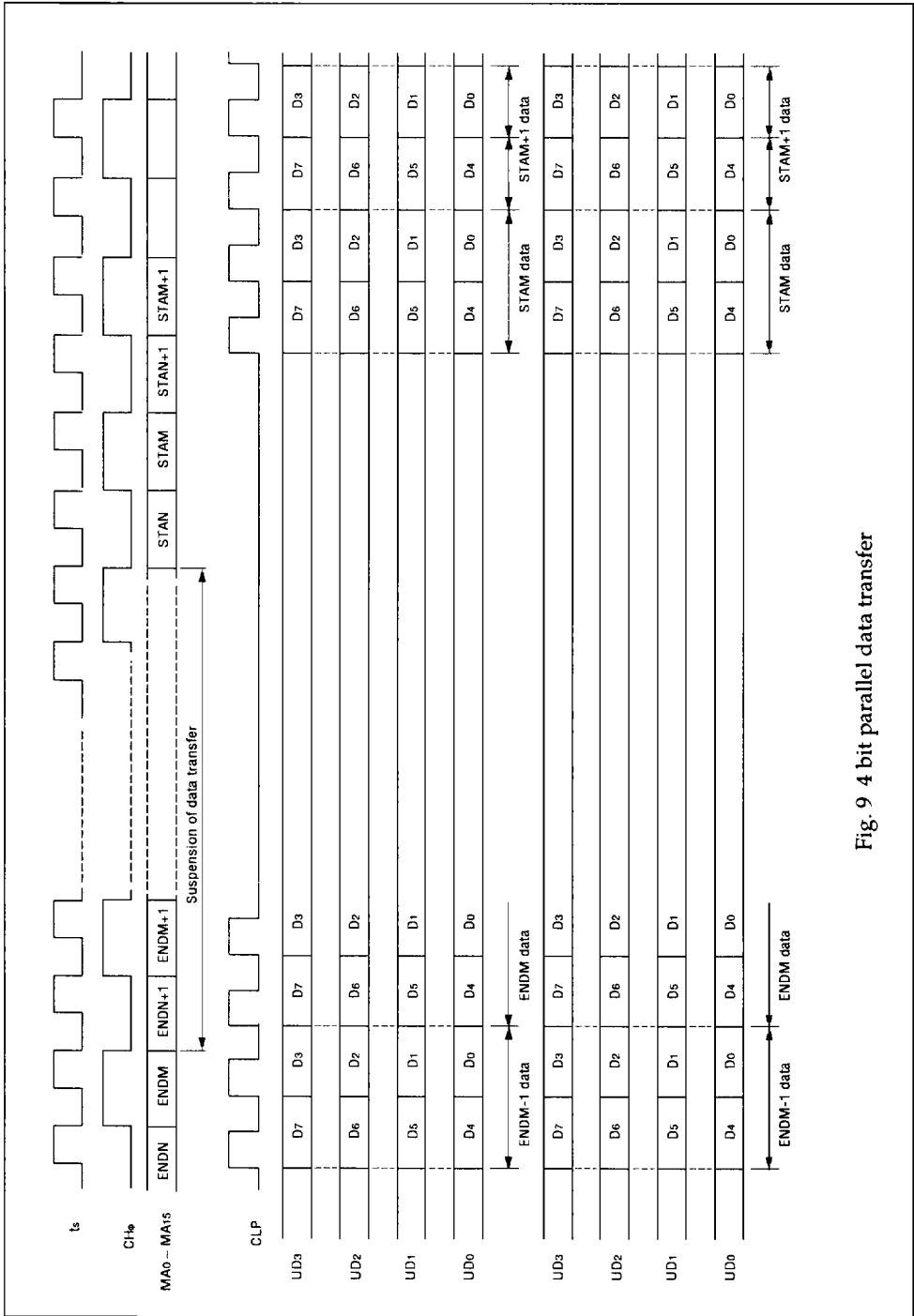


Fig. 9 4 bit parallel data transfer

9. LCD Driver

The most suitable LCD drivers for 4-bit parallel data transfer are MSM5278GS (common driver) and MSM5279GS (segment driver). MSM5260GS is the most suitable common/segment LCD driver in the case of 1-bit serial data transfer and 2-bit parallel data transfer.

Note: 4-bit parallel data transfer cannot be applied to MSM5260GS. Both 1-bit serial data transfer and 2-bit parallel data transfer cannot be applied to MSM5279GS.

10. Relation Between Duty and Number of Lines

Number of lines is determined by V_p , vertical character pitch, and V_{λ} , number of lines in vertical direction.

$$\text{Number of lines} = V_{\lambda} / V_p \times 2$$

Note: In the graphic mode, number of lines should not be odd number.

11. Calculation of Crystal Oscillation Frequency (f_{osc})

Table 3 Calculation formula of f_{osc}

DIV	Output mode	Calculation formula of f_{osc}	Calculation exmaple (MHz)
L	①	$FRP \times (H_N + 8) \times H_p \times V_{\lambda} \times 2$	9,856
	②	$FRP \times (H_N + 8) \times V_{\lambda} \times 4$	2,464
H	①	$FRP \times (H_N + 8) \times V_p \times V_{\lambda}$	4,928
	②	$FRP \times (H_N + 8) \times V_{\lambda} \times 2$	1,232

Note: (1) Table 3 shows a calculation example assuming that $FRP = 70$ Hz, $H_N = 80$, $H_p = 8$ and $V_1 = 100$, however, the example of $H_p = 4 \sim 7$ in 4-bit parallel is not included.

- (2) Output mode ① : $H_p = 4 \sim 7$ in 1-bit serial, 2-bit parallel and 4-bit parallel
- Output mode ② : $H_p = 8$ in 4-bit parallel

12. Calculation of Character Clock (CH_{ϕ}) Frequency

$$CH_{\phi} = FRP \times (H_N + 8) \times V_{\lambda}$$

Example: Assuming $FRP = 70$ Hz, $H_N = 80$ and $V_{\lambda} = 100$, $CH_{\phi} = 1.62$ (μ s)

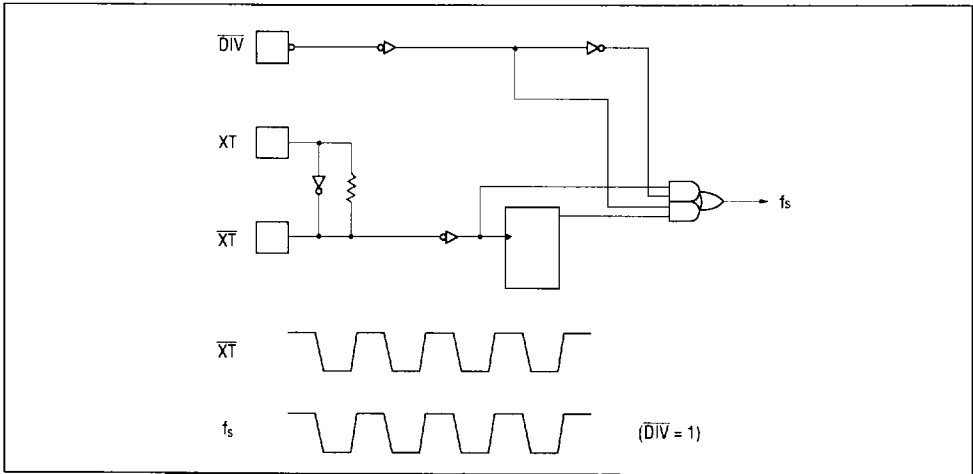
13. Calculation Shift Clock (CLP) Frequency

Table 4 Calculation formula of CLP

Output mode	Calculation formula of CLP	Calculation exmaple (MHz)
1-bit serial	$FRP \times (H_N + 8) \times H_p \times V_{\lambda}$	4,928
2-bit parallel	$FRP \times (H_N + 8) \times H_p \times V_{\lambda} \times 1/2$	2,464
4-bit parallel	$FRP \times (H_N + 8) \times H_p \times V_{\lambda} \times 1/4$	1,232

Note: Table 4 shows a calculation example assuming that $FRP = 70$ Hz, $H_N = 80$, $H_p = 8$ and $V_{\lambda} = 100$.

14. Relation Between Reference Clock (f_s) and External Clock



f_s functions as a dot clock in LCDC and the dot counter inside the IC is counted up at the trailing edge of f_s .

The dot counter operates in N number system and its signals are output as CH_ϕ . (Refer to the time charts Fig. 7~9 and Fig. 14.)

15. Access to the Display RAM

In writing/reading the data to/from the display RAM, DIEN should be low level. By setting DIEN signal at low level, the address from the CPU are output from MA0~MA15, and this enables the access to the display RAM.

There are 3 methods about accessing display RAM from the CPU.

(1) Direct access from CPU

Display RAM is accessed directly from the CPU, irrespective of MSM6255GS condition (refresh cycle or not).

In this method, the RAM address changes to the CPU address when the display is on the screen. So, frequent address to the RAM causes flickering on the screen.

(2) Access while BUSY signal is at high level

BUSY signal indicates the period when the data transfer stops, and BUSY signal

is set at high level when the data transfer stops. The period when BUSY signal is high corresponds to that of seven characters'. If display RAM is accessed during this period (when BUSY is high), the display on the screen does not flicker.

Note: This method is effective when the size of screen is small. In the case of big size screen, 640 x 200 dots, 1-character needs approx. 1.6 μ s. So, in this case, the period when BUSY is at high level is 11.2 μ s, which is impossible to write a lot of data.

(3) Synchronized access

Refresh cycle and CPU cycle are alternately performed. So, there is not flickering on the screen and there is no need to sense the BUSY signal.

In this method, however, some external circuits are necessary. The timing chart of this method is described in the figure 10 below.

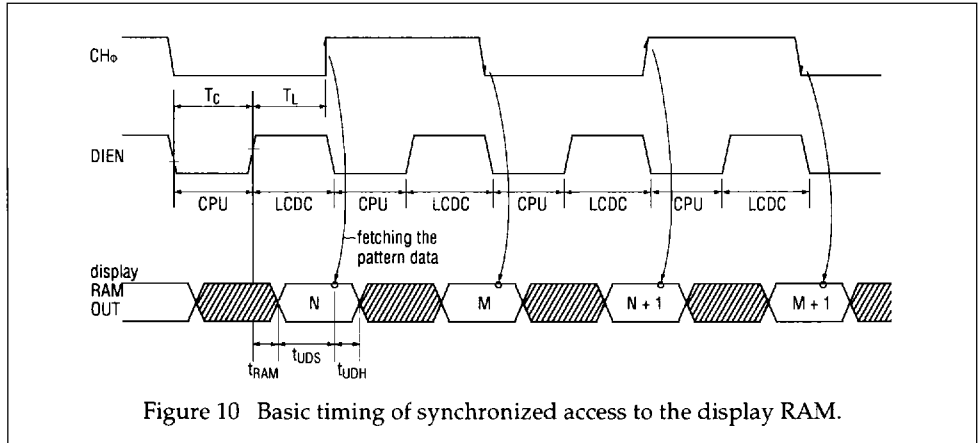


Figure 10 Basic timing of synchronized access to the display RAM.

legend

- TC : Period when the address bus is occupied by CPU
 - TC : Period when the LCDC fetches the refreshed data
 - tRAM : Refresh address delay time + memory access time
 - tUDS : Upper side data set-up time
 - tUDH : Upper side data hold time
 - MA₀ ~ MA₁₅ output address to the upper side when DIEN is high and CH_φ is low.
- To perform synchronized access method, the timing between DIEN and CH_φ should be as described in Figure 10.

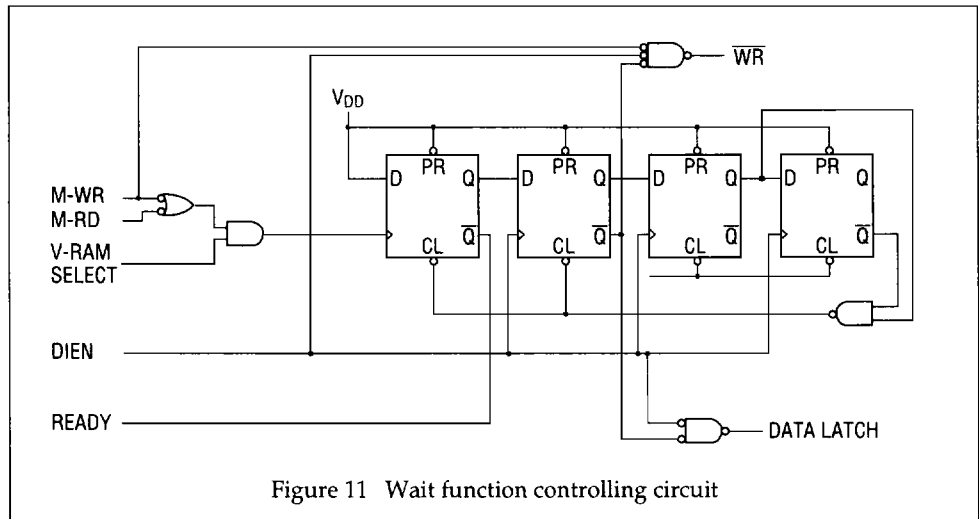


Figure 11 Wait function controlling circuit

Display RAM must meet the following requirement.

$$T_L > t_{RAM} + t_{UDS}$$

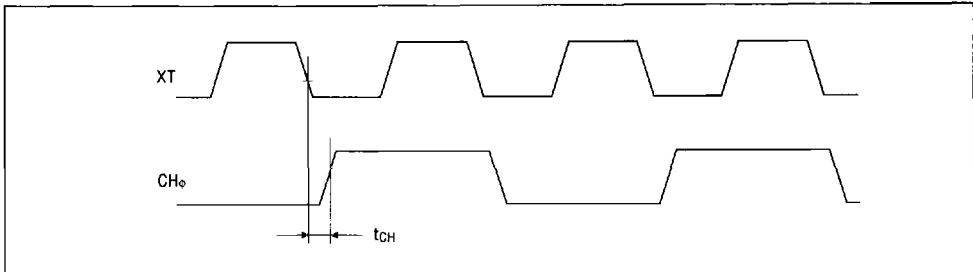
In writing data into the display RAM, LCDC

should be synchronized so that the write pulse should occur during the period of T_C. In reading the pattern data from the CPU, the data of display RAM should be latched first. Figure 11 shows the controlling circuit.

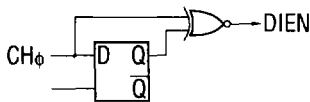
16. DIEN

DIEN has to be generated when the display RAM is accessed by Synchronized access method described in 15-(3).

- (1) Control the LCD module by separating upper side and lower side
The timing chart of XT and CH_φ are described as below. In this case, 4-bit data transfer is applied and H_p = 8.



DIEN signal is generated by XT and CH_φ.
DIEN signal generating circuit is described in the figure bellow.



When H_p ≠ 8 in the 1-bit serial, 2-bit parallel and 4-bit parallel mode, the relation between XT and CH_φ should be referred to Figures 7 and 8.

17. Scroll-Paging

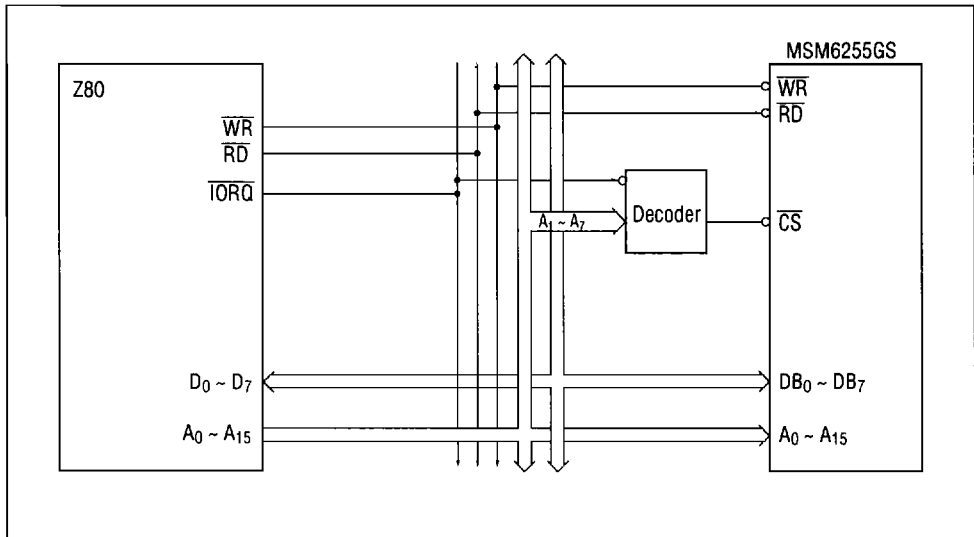
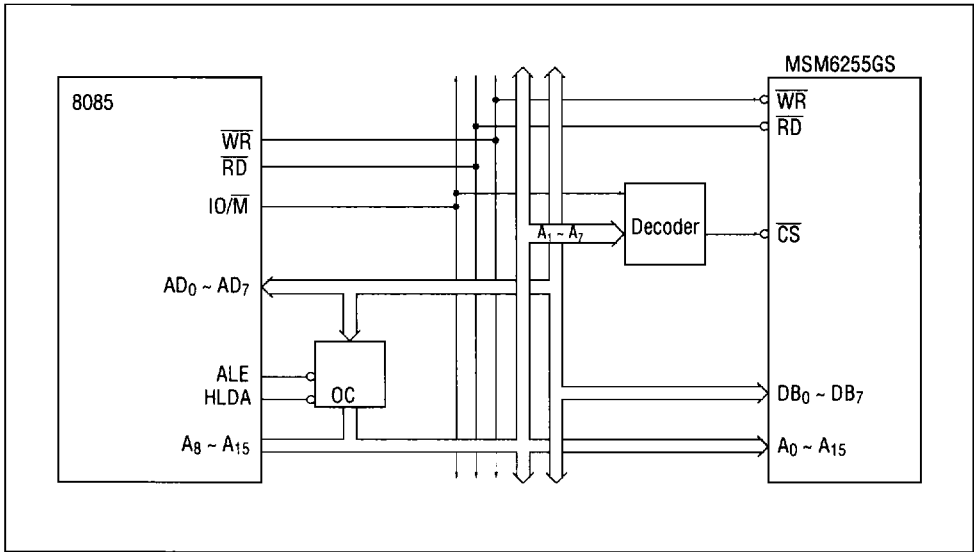
Scroll-paging is enabled by setting the display start address to the scroll address register.

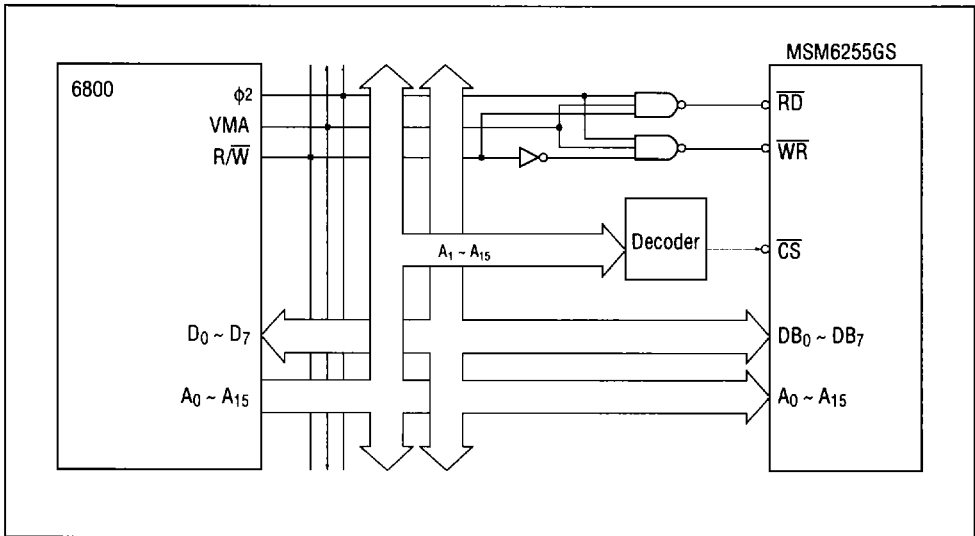
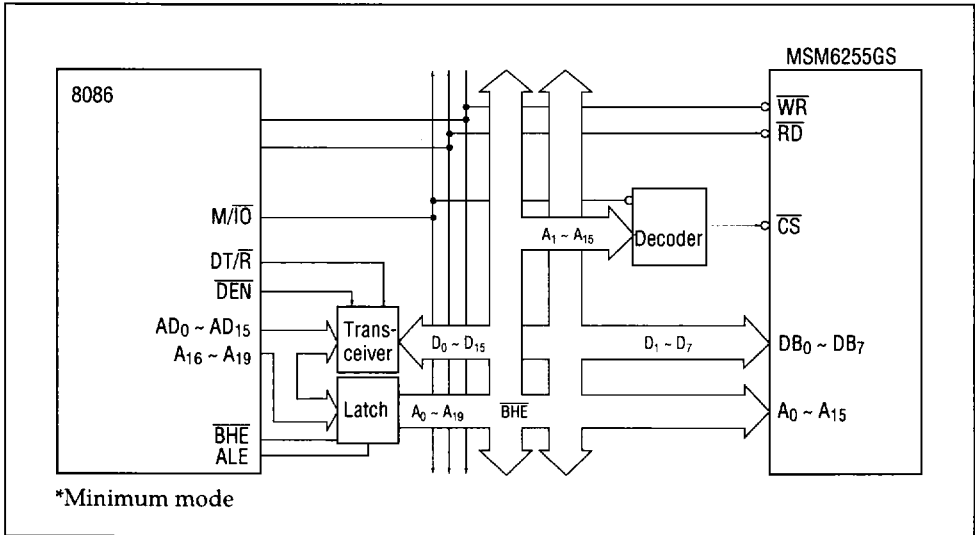
- (1) Memory address of vertical scroll-paging
Figure 2 shows the memory address when the start address is 0000. When the start address is set at 0050, the display will be vertically shifted by +1.
By setting the starting address one by one, the screen will scroll vertically.

paging will be performed by setting the start address as 3E80.

- (2) Memory address of horizontal scroll
When the starting address is set at 0001 in Figure 2, the display on the screen will be shifted by +1 byte horizontally. The data shown as 004F in Figure 2 corresponds to the memory data in the 2nd line shown as 0050.

INTERFACE WITH CPU





SYSTEM CONFIGURATION

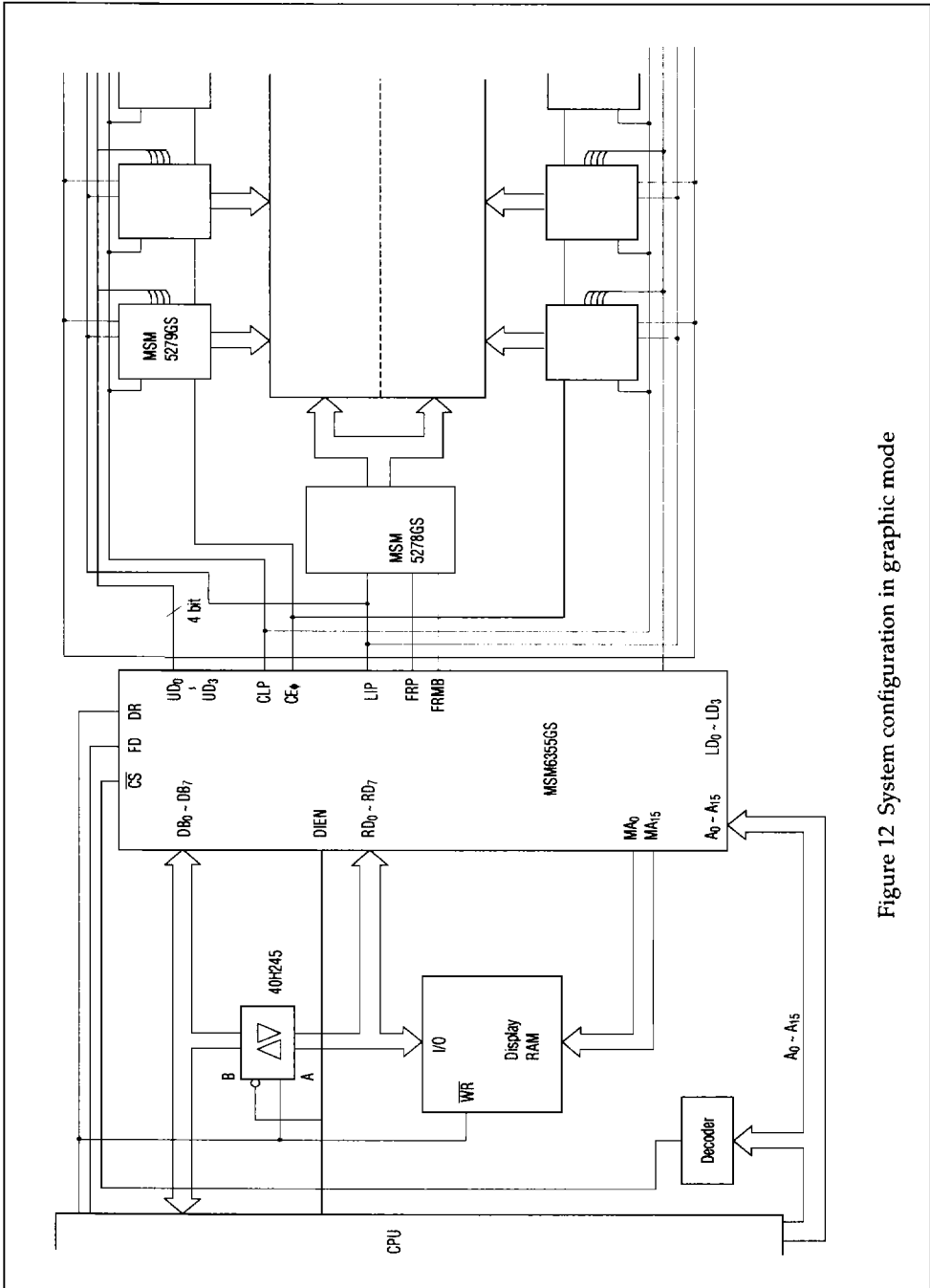


Figure 12 System configuration in graphic mode

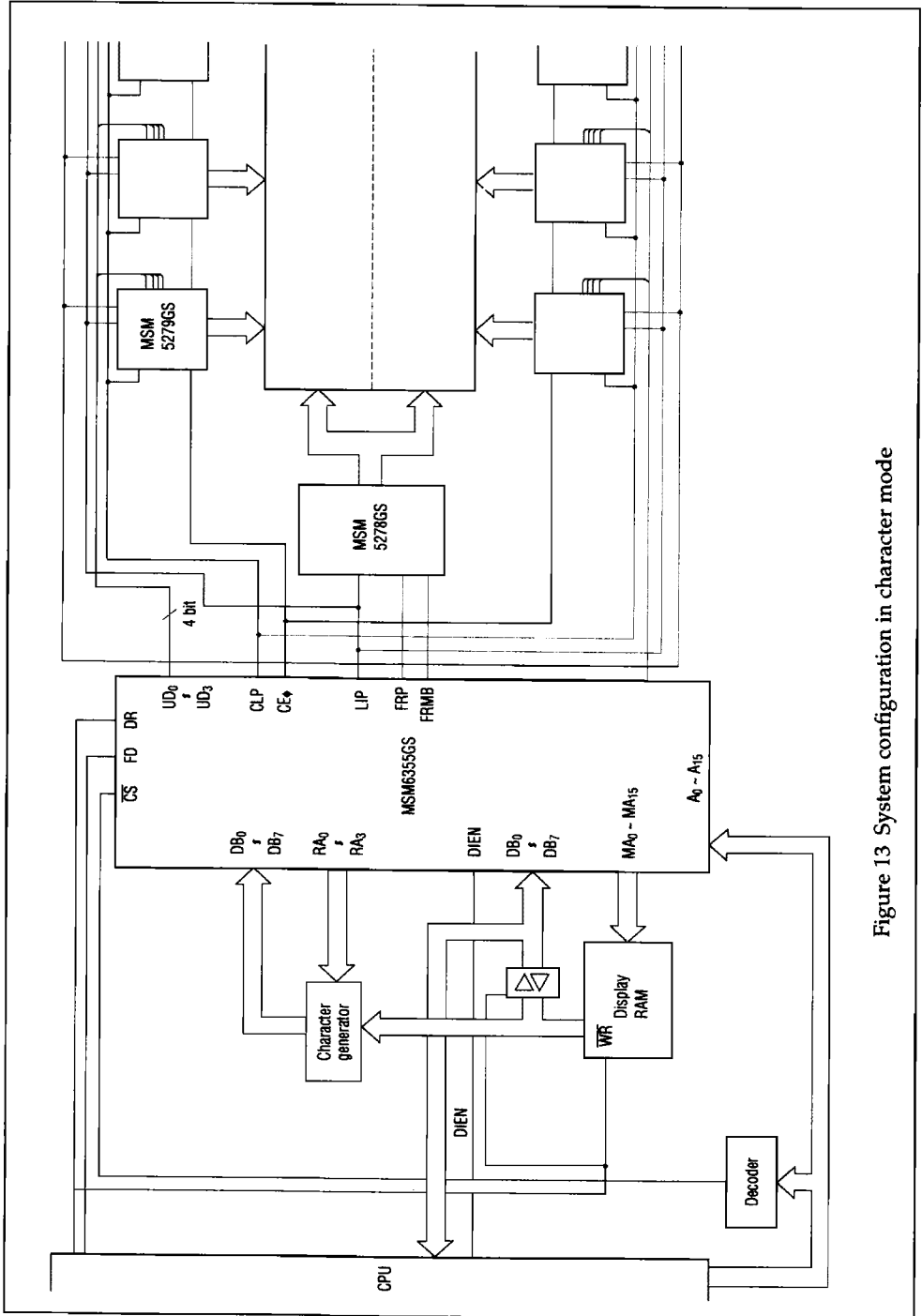


Figure 13 System configuration in character mode

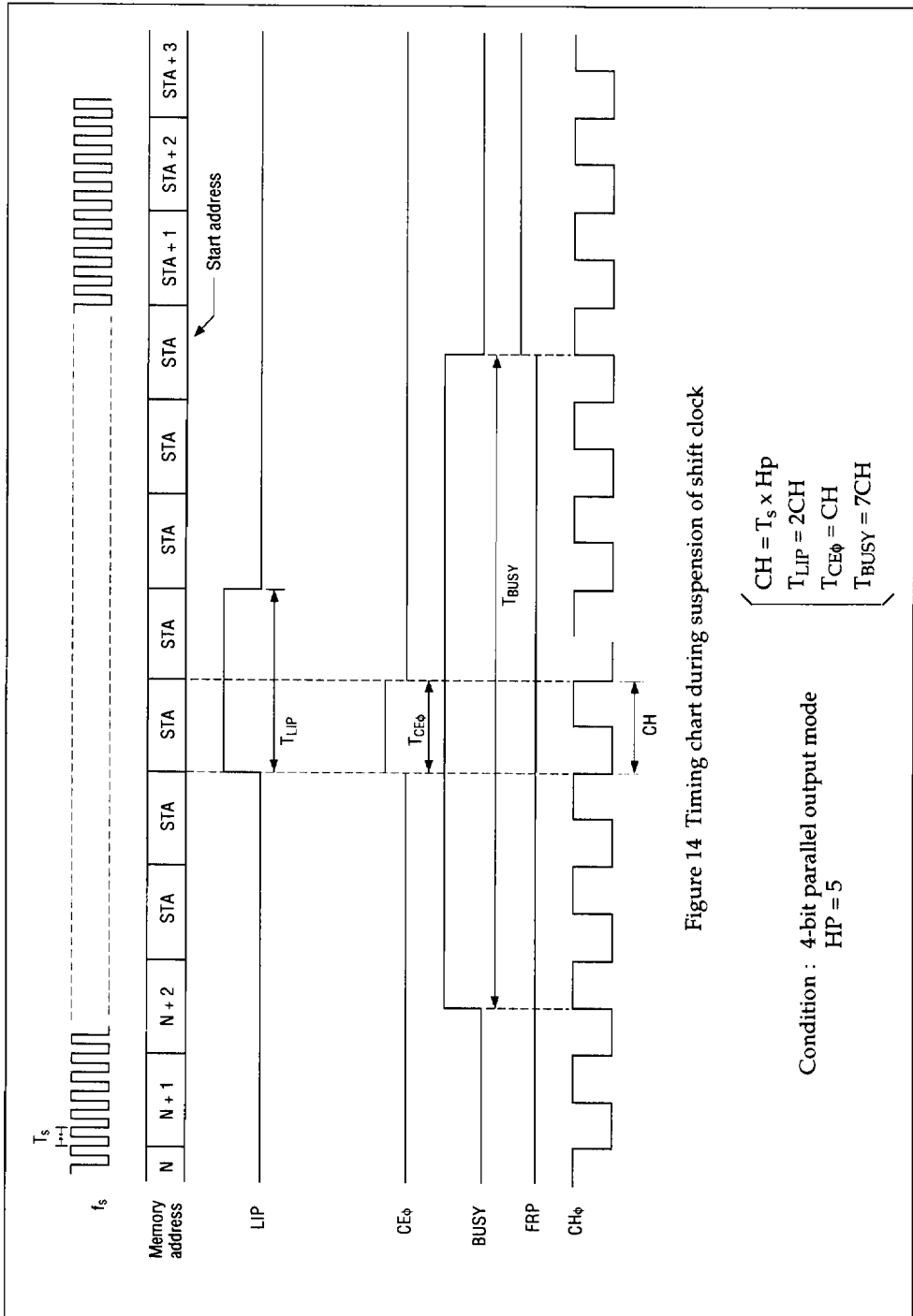


Figure 14 Timing chart during suspension of shift clock

$$\left. \begin{aligned} CH &= T_s \times Hp \\ T_{LIP} &= 2CH \\ T_{CE\phi} &= CH \\ T_{BUSY} &= 7CH \end{aligned} \right\}$$

Condition : 4-bit parallel output mode
HP = 5

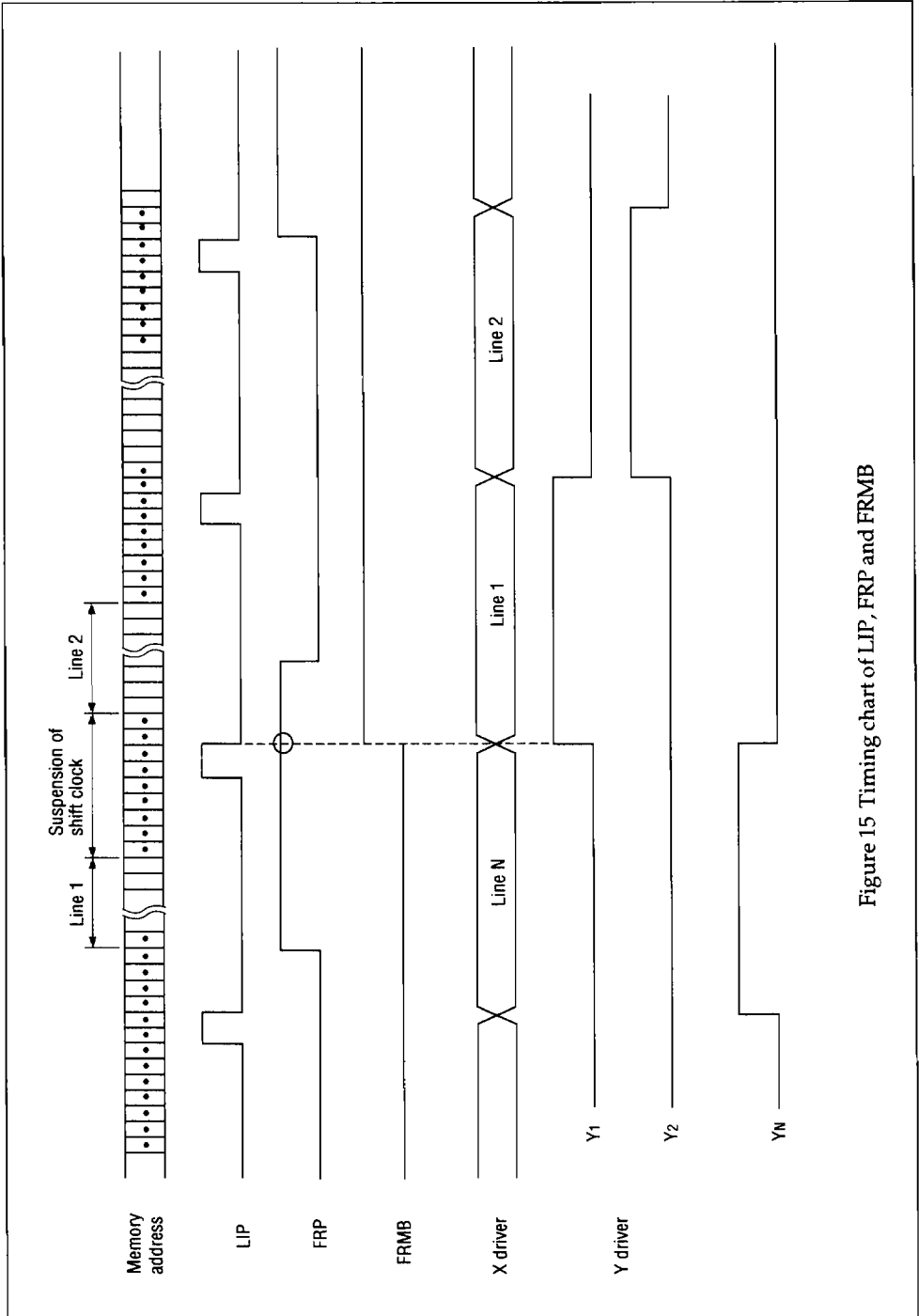


Figure 15 Timing chart of LIP, FRP and FRMB

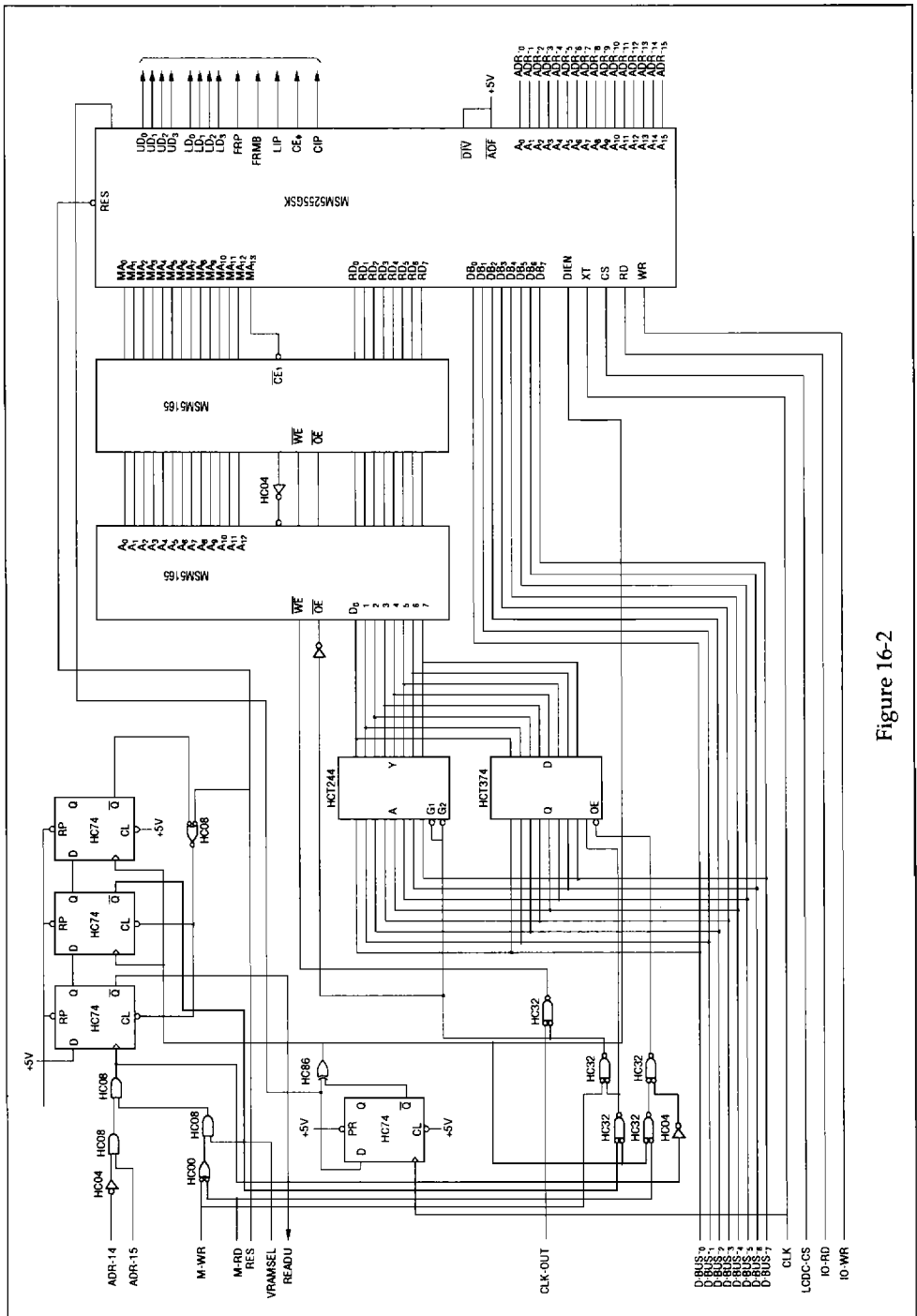


Figure 16-2

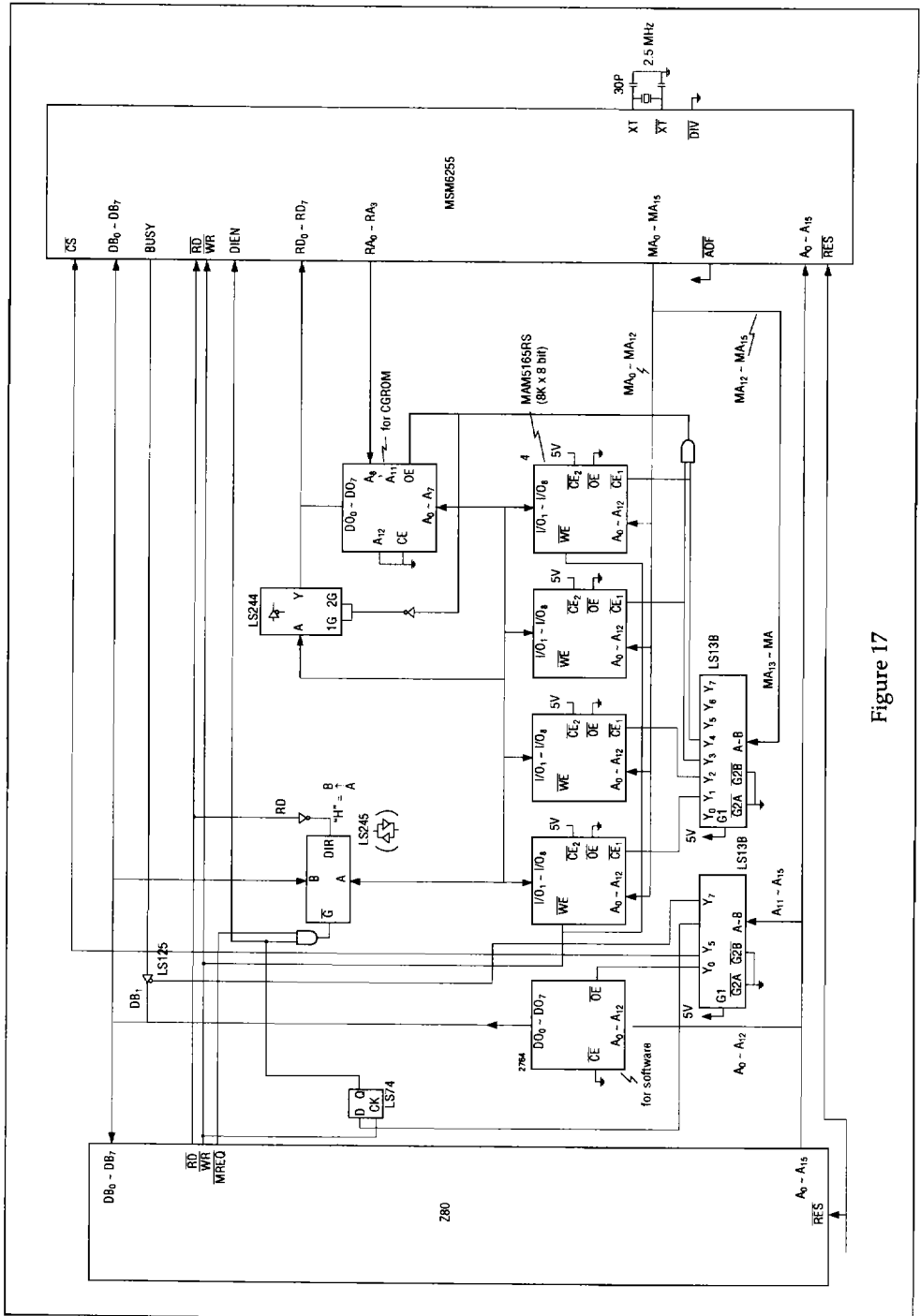


Figure 17