Advance Information

128K/64K **X84F128/064** MPS™ Serial Flash

Micro Port Saver SerialFlash with Block Lock™ Protection

FEATURES

- **Direct Interface to Micros**
  - **—Eliminates I/O port requirements**
  - **—No interface glue logic required**
  - **—Eliminates need for parallel to serial converters**
- **New Programmable Block Lock™ Protection**
  - **—Software Program Protection**
  - **—Programmable Hardware Program Protection**
- **Block Lock (0, 1/4, 1/2, or all of the array)**
- **Up to 5Mbps data transfer rate**
- **Low Power CMOS**
  - **—3V or 5V "Univolt" Read and Program Power Supply Versions**
  - **—Standby Current Less than 1μA**
  - **—Active Current Less than 1mA**
- **Minimum 45ns Read Access Time**
- **256-Bit Sector Program Mode**
- **Typical Nonvolatile Program Cycle Time: 5ms**
- **High Reliability**
  - **—100,000 Endurance Cycles**
  - **—Data Retention: 100 Years**

DESCRIPTION

The X84F128/064 Micro Port SerialFlash devices are 16K/8K-bit CMOS memories designed for direct interface to port limited microcontroller or I/O limited ASIC and microprocessor designs. The MPS interface eliminates the need for parallel to serial conversion hardware simplifying system design.

The X84F128/064 provide all of the benefits of serial memories, such as low cost, low power, low voltage operation, and small package size, while featuring higher data transfer rates and reduced interface code requirements—without the need for a dedicated serial bus. All of the products are organized into 256 bit sectors and are suitable in 8-bit, 16-bit, 32-bit, or 64-bit environments, due to the bit serial nature of the interface.

The X84F128/064 devices directly connect to the system bus and communicate over a single data line using a sequence of standard bus read and write operations. This eliminates the need for dedicated port pins, parallel to serial converters, complicated ASIC implementations, or other glue logic, lowering system cost.

The X84F128/064 provides additional data security features through Block Lock and programmable Hardware Program Protection. These allow some or all of the array to be program protected by software command or by hardware. System Configuration, Company ID, calibration information, or other critical data can be secured a gainst unexpected or inadvertent program operations, leaving the remainder of the memory available for the system or user access.

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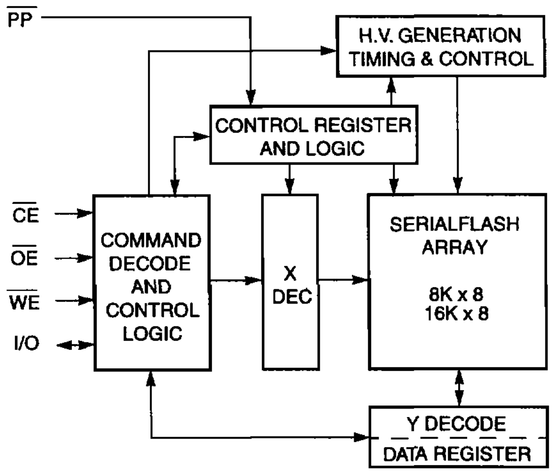
BLOCK DIAGRAM



7022 FRM F01

Xicor E^2PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

PIN DESCRIPTIONS

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, the chip is deselected, the I/O pin is in the high impedance state, and unless a nonvolatile program operation is underway, the device is in the standby power mode.

Output Enable ($\overline{OE}$)

The Output Enable input must be LOW to enable the output buffer and to read data from the device on the I/O line.

Write Enable ($\overline{WE}$)

The Write Enable input must be LOW to write either data or command sequences to the device.

Data In/Data Out (I/O)

Data and command sequences are serially written to or serially read from the device through the I/O pin.

Program Protect ($\overline{PP}$)

The Program Protect input controls the Hardware Program Protect feature. When $\overline{PP}$ is LOW and the nonvolatile bit PPEN is "1", nonvolatile programming of the X84F128/064 control register is disabled, but the part otherwise functions normally. When $\overline{PP}$ is held HIGH, all functions, including nonvolatile programming operate normally. $\overline{PP}$ going LOW while $\overline{CS}$ is still LOW will interrupt a program to the X84F128/064 control register. If the internal Program cycle has already been initiated, $\overline{PP}$ going LOW will have no effect on programming.

The $\overline{PP}$ pin function is blocked when the PPEN bit in the control register is "0". This allows the user to install the X84F128/064 in a system with $\overline{PP}$ pin grounded and still be able to program to the control register. The $\overline{PP}$ pin functions will be enabled when the PPEN bit is set "1".

PIN NAMES

I/O	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{PP}$	Program Protect Input
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	No Connect

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PINOUT/PACKAGE SELECTION GUIDE

X84F064	8-Lead Dip (P) 14-Lead SOIC (S)
X84F128	8-Lead Dip (P) 16-Lead SOIC (S)

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PIN CONFIGURATIONS

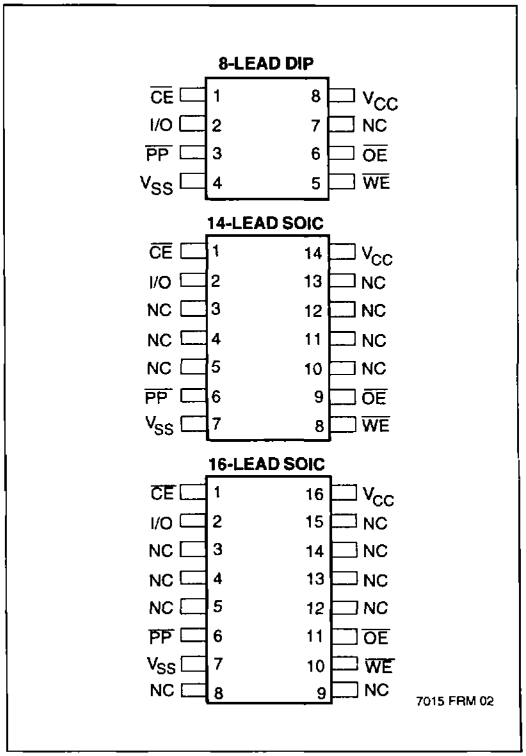
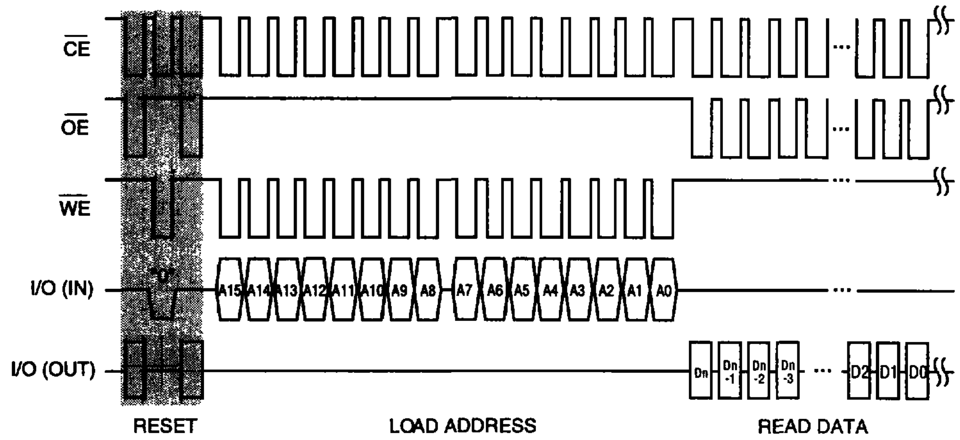


Figure 1. Read Sequence



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DEVICE OPERATION

The X84F128/064 are SerialFlash devices designed to interface directly with most microprocessor buses. Standard $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ signals control the read and program operations, and a single I/O line is used to send and receive data and commands serially.

Data Timing

Data input on the I/O line is latched on the rising edge of either $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Data output on the I/O line is active whenever both $\overline{OE}$ and $\overline{CE}$ are LOW. Care should be taken to ensure that $\overline{WE}$ and $\overline{OE}$ are never both LOW while $\overline{CE}$ is LOW.

Read Sequence

A read sequence consists of sending a 16-bit address followed by the reading of data serially. The address is written by issuing 16 separate write cycles ($\overline{WE}$ and $\overline{CE}$ LOW, $\overline{OE}$ HIGH) to the part without a read cycle between the write cycles. The address is sent serially, most significant bit first, over the I/O line. Note that this sequence is fully static, with no special timing restrictions, and the processor is free to perform other tasks on the bus whenever the device $\overline{CE}$ pin is HIGH. Once the 16 address bits are sent, a byte of data can be read on the I/O line by issuing 8 separate read cycles ($\overline{OE}$ and $\overline{CE}$ LOW, $\overline{WE}$ HIGH). At this point, writing a '1' will terminate the read sequence and enter the low power standby state, otherwise the device will await further reads in the sequential read mode.

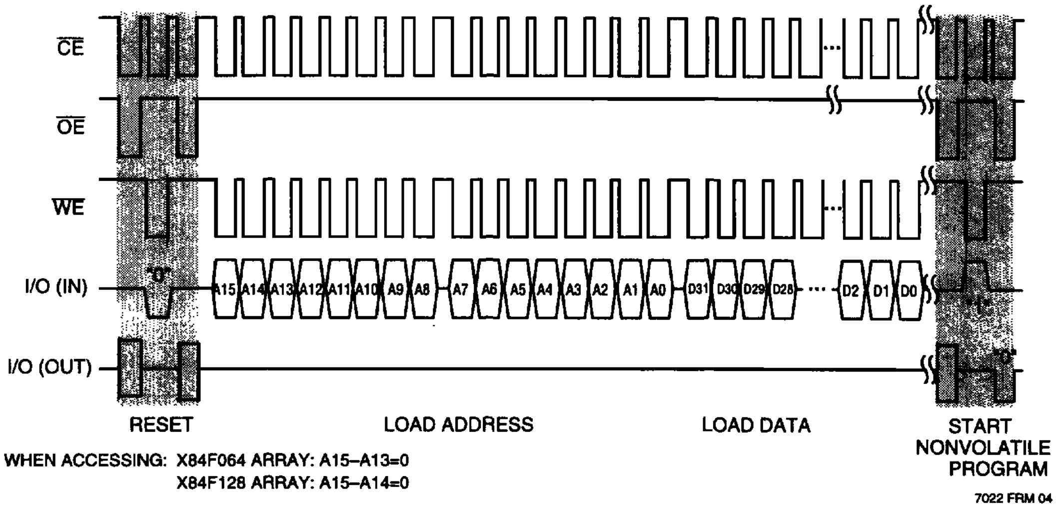
Sequential Read

The bit address is automatically incremented to the next higher address after each bit of data is read. The data stored in the memory at the next address can be read sequentially by continuing to issue read cycles. When the highest address in the array is reached, the address counter rolls over to address $000 and reading may be continued indefinitely.

Reset Sequence

The reset sequence resets the device and sets an internal Program enable latch. A reset sequence can be sent at any time by performing a read/write "0"/read operation (see Figs. 1 and 2). This breaks the multiple read or Program cycle sequences that are normally used to read from or program the part. The reset sequence can be used at any time to interrupt or end a sequential read or page load. As soon as the write "0" cycle is complete, the part is reset (unless a nonvolatile program cycle is in progress). The second read cycle in this sequence, and any further read cycles, will read a HIGH on the I/O pin until a valid read sequence (which includes the address) is issued. The reset sequence must be issued at the beginning of both read and program sequences to be sure the device initiates these operations properly.

Figure 2: Program Sequence



Program Sequence

A nonvolatile program sequence consists of sending a reset sequence, the 16-bit address of the first location in a sector, 256-bits bytes of data, and then a special "start nonvolatile program cycle" command sequence. The reset sequence is issued first (as described in the Reset Sequence section) to set an internal program enable latch. The address is written serially by issuing 16 separate write cycles (WE and CE LOW, OE HIGH) to the part without any read cycles between the writes.The address is sent serially, most significant bit first,on the I/O pin. The 256-bits of data are programmed by issuing 256 separate write cycles. Again, no read cycles are allowed between writes and a full 256-bit sector must be programmed.

The nonvolatile program cycle is initiated by issuing a special read/write "1"/read sequence. The first read cycle ends the sector load, then the write "1" followed by a read starts the nonvolatile program cycle. The device recognizes 256-bit sectors beginning at addresses XXXX00000. When sending data to the part, attempts to exceed the upper address of the page will result in undefined data being programmed in the array.

A nonvolatile program cycle will not start if a partial or incomplete program sequence is issued. The internal program enable latch is reset when the nonvolatile program cycle is completed to prevent inadvertent programming.

Nonvolatile Program Status

The status of a nonvolatile program cycle can be determined at any time by simply reading the state of the I/O pin on the device. This pin is read when OE and CE are LOW and WE is HIGH. During a nonvolatile program cycle the I/O pin is LOW. When the nonvolatile program cycle is complete, the I/O pin goes HIGH. A reset sequence can also be issued during a nonvolatile program cycle with the same result: I/O is LOW as long as a nonvolatile program cycle is in progress, and I/O is HIGH when the nonvolatile program cycle is done.

CONTROL REGISTER

The X84F128/064 has one register that contains control bits for the devices. The control bits, PPEN, BP1, and BP0, are shown in Table 1. To read or change the contents of this register requires a one byte operation to address FFFFh.

A read from FFFFh returns the one byte contents of the control register unused bits return 0. Continued reads return undefined data. Programming address FFFFh changes the value of the bits. Unused bits are programmed as "0". Writing more than one byte to the control register is a violation and the operation will be aborted. After sending one byte to the control register, a start nonvolatile program cycle will latch in the new state.

Table 1

7	6	5	4	3	2	1	0
PPEN	0	0	0	BP1	BP0	0	0

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PPEN: Program Protect Enable Bit

The Program-Protect-Enable (PPEN) bit is an enable bit for the $\overline{PP}$ pin.

Table Table 2

PPEN	$\overline{PP}$	Protected Blocks	Unprotected Blocks	Control Register
0	X	Protected	Programmable	Programmable
1	LOW	Protected	Programmable	Protected
X	HIGH	Protected	Programmable	Programmable

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The Program Protect ($\overline{PP}$) pin and the nonvolatile Program Protect Enable (PPEN) bit in the Control Register control the programmable hardware program protect feature. Hardware program protection is enabled when $\overline{PP}$ pin is LOW, and the PPEN bit is "1". Hardware program protection is disabled when either the $\overline{PP}$ pin is HIGH or the PPEN bit is "0". When the chip is hardware program protected, nonvolatile programming is disabled to the Control Register, including the Block Protect bits and the PPEN bit itself, as well as the block-protected sections in the memory array. Only the sections of the memory array that are not block-protected can be programmed.

Note: When the $\overline{PP}$ pin is tied to V_{SS} and the PPEN bit is HIGH, the PPEN bit is Program protected. It cannot be changed back to a "0", as long as the $\overline{PP}$ pin is held LOW.

BP1, BP0: Block Protect Bits

The Block Protect (BP0 and BP1) bits are nonvolatile and allow the user to select one of four levels of protection. The X84F128/064 is divided into four segments. One, two, or all four of the segments may be protected. That is, the user may read the segments but will be unable to alter (program) data within the selected segments. The partitioning is controlled as illustrated in table 3 below.

Table 3. Block Lock Protection

Control Register Bits		Array Address Protected		
BP1	BP0	X84F064	X84F128	
0	0	None	None	
0	1	1800h–1FFFh	3000h–3FFFh	upper 1/4
1	0	1000h–1FFFh	2000h–3FFFh	upper 1/2
1	1	0000–1FFFh	0000–3FFFh	Full Array (Not including the control register.)

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Low Power Operation

The device enters an idle state, which draws minimal current when:

—an illegal sequence is entered. The following are the more common illegal sequences:

- Read/Write/Write—any time
- Read/Write '1'—When writing the address or writing data.
- Write '1'—when reading data
- Read/Read/Write '1'—after data is written to device, but before entering the NV program sequence.

—the device powers-up;

—a nonvolatile program operation completes.

While a sequential read is in progress, the device remains in an active state. This state draws more current than the idle state, but not as much as during a read itself. To go back to the lowest power condition, an invalid condition is created by writing a '1' after the last bit of a read operation.

Program Protection

The following circuitry has been included to prevent inadvertent nonvolatile programming:

—The internal program enable latch is reset upon power-up.

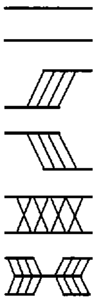
—A reset sequence must be issued to set the internal program enable latch before starting a program sequence.

—A special "start nonvolatile program" command sequence is required to start a nonvolatile program cycle.

—The internal program enable latch is reset automatically at the end of a nonvolatile program cycle.

—The internal program Enable latch is reset and remains reset as long as the $\overline{PP}$ pin is LOW, which blocks all nonvolatile program cycles.

SYMBOL TABLE



WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

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ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias .... –65°C to +135°C
Storage Temperature .... –65°C to +150°C
Terminal Voltage with
Respect to V_{SS} .... –1V to +7V
DC Output Current... 5mA
Lead Temperature (Soldering, 10 seconds)..........300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Extended	–20°C	+85°C
Industrial	-40°C	+85°C

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Supply Voltage	Limits
X84F128/064	5V ±10%
X84F128/064	3V ± 20%

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D.C. OPERATING CHARACTERISTICS: (VCC = 5V ±10%)

(Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Conditions
I_{CC1}	V_{CC} Supply Current (Read)		1	mA	$\overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, I/O = Open, $\overline{CE}$ clocking @ 5MHz
I_{CC2}	V_{CC} Supply Current (Program)		3	mA	I_{CC} During Nonvolatile Program Cycle All Inputs at CMOS Levels
I_{SB1} (2)	V_{CC} Standby Current		1	µA	$\overline{CE} = V_{CC}$, Other Inputs = V_{CC} or V_{SS}
I_{LI}	Input Leakage Current		10	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output Leakage Current		10	µA	$V_{OUT} = V_{SS}$ to V_{CC}
V_{IL} (1)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH} (1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	V_{CC} – 0.8		V	I_{OH} = –1mA

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Notes: (1) V_{IL} Min. and V_{IH} Max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

D.C. OPERATING CHARACTERISTICS (V_{CC} = 3V ± 20%)

(Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		500	µA	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, I/O = Open, $\overline{CE}$ clocking @ 3MHz
I_{CC2}	V_{CC} Supply Current (Program)		2	mA	I_{CC} During Nonvolatile Program Cycle All Inputs at CMOS Levels
I_{SB1}(2)	V_{CC} Standby Current		1	µA	$\overline{CE}$ = V_{CC}, Other Inputs = V_{CC} or V_{SS}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 1mA
V_{OH}	Output HIGH Voltage	V_{CC} – 0.4		V	I_{OH} = –400µA

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CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(2)	Input/Output Capacitance	8	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V

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POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(3)	Power-up to Read Operation	1	ms
t_{PUW}(3)	Power-up to Program Operation	1	ms

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A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Levels	V_{CC} x 0.5

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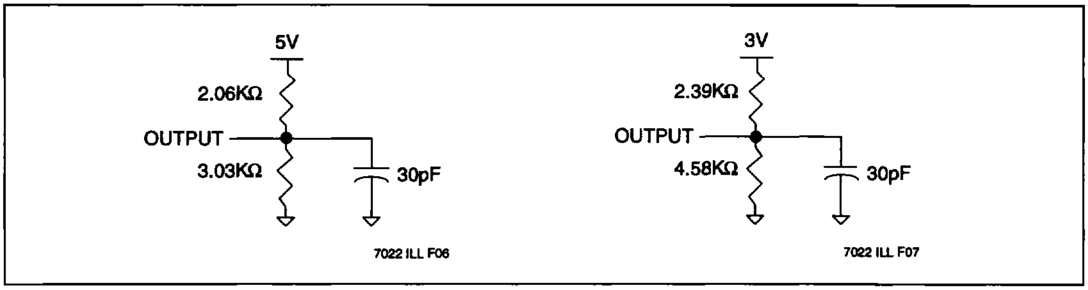
Notes: (3) Time delays required from the time the V_{CC} is stable until the specific operation can be initiated. Periodically sampled, and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUITS



A.C. CHARACTERISTICS

(Over the recommended operating conditions, unless otherwise specified.)

Read Cycle Limits – X84F128/064

Symbol	Parameter	V_{CC} = 5V ±10% Min.	V_{CC} = 5V ±10% Max.	V_{CC} = 3V ± 20% Min.	V_{CC} = 3V ± 20% Max.	Units
t_{RC}	Read Cycle Time	200		330		ns
t_{CE}	$\overline{CE}$ Access Time		45		120	ns
t_{OE}	$\overline{OE}$ Access Time		45		120	ns
t_{LOW}	$\overline{CE}$ LOW Time	70		150		ns
t_{HIGH}	$\overline{CE}$ HIGH Time	70		150		ns
t_{LZ}(4)	$\overline{CE}$ LOW to Output In Low Z	0		0		ns
t_{HZ}(4)	$\overline{CE}$ HIGH to Output In High Z	0	30	0	45	ns
t_{OLZ}(4)	$\overline{OE}$ LOW to Output In Low Z	0		0		ns
t_{OHZ}(4)	$\overline{OE}$ HIGH to Output In High Z	0	30	0	45	ns
t_{OH}	Output Hold from $\overline{CE}$ or $\overline{OE}$ HIGH	0		0		ns
t_{WES}	$\overline{WE}$ HIGH Setup Time	25		25		ns
t_{WEH}	$\overline{WE}$ HIGH Hold Time	25		25		ns

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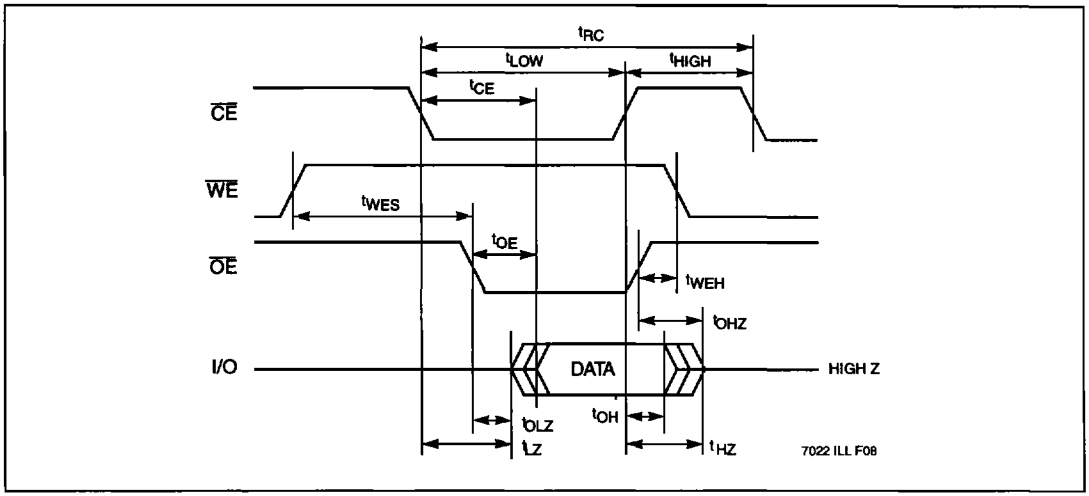
Notes: (4) Periodically sampled, but not 100% tested. t_{HZ} and t_{OHZ} are measured from the point where $\overline{CE}$ or $\overline{OE}$ goes HIGH (whichever occurs first) to the time when I/O is no longer being driven into a 5pF load.

Read Cycle



Program Cycle Limits – X84F128/064

Symbol	Parameter	V_{CC} = 5V ±10% Min.	Max.	V_{CC} = 3V ± 20% Min.	Max.	Units
t_{NVPC}[(5)]	NonVolatile Program Cycle Time		5		5	ms
t_{CYC}	Cycle Time	200	10,000	330	10,000	ns
t_{WP}	$\overline{WE}$ Pulse Width	30		45		ns
t_{WPH}	$\overline{WE}$ HIGH Recovery Time	170		255		ns
t_{CS}	Program Setup Time	0		0		ns
t_{CH}	Program Hold Time	0		0		ns
t_{CP}	$\overline{CE}$ Pulse Width	30		45		ns
t_{CPH}	$\overline{CE}$ HIGH Recovery Time	170		255		ns
t_{OES}	$\overline{OE}$ HIGH Setup Time	25		37		ns
t_{OEH}	$\overline{OE}$ HIGH Hold Time	25		37		ns
t_{DS}[(6)]	Data Setup Time	30		45		ns
t_{DH}[(6)]	Data Hold Time	5		5		ns
t_{PPCS}[(7)]	$\overline{PP}$ HIGH Before $\overline{CE}$	100		150		ns
t_{PPCH}[(7)]	$\overline{PP}$ HIGH After $\overline{CE}$	100		150		ns

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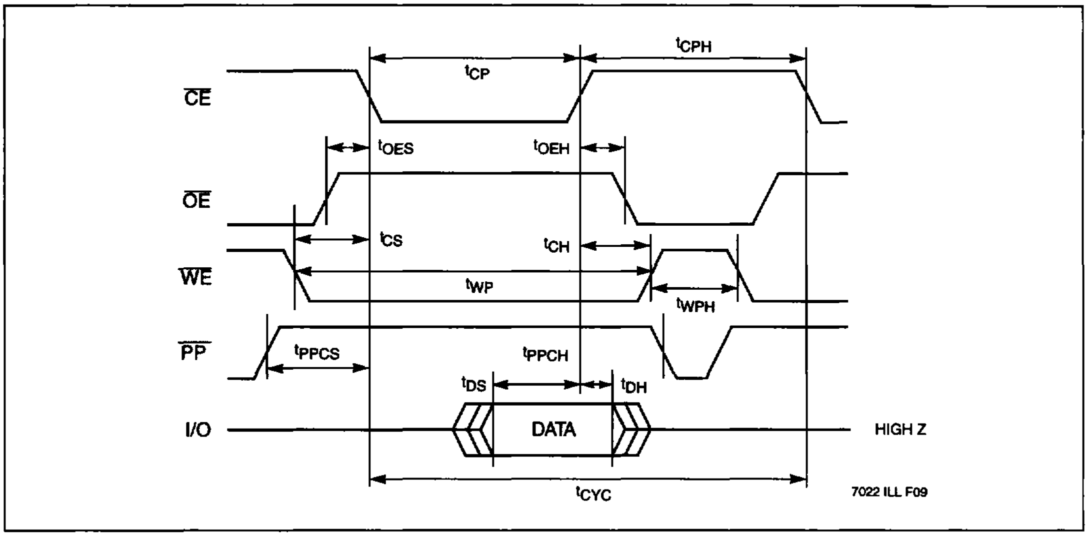
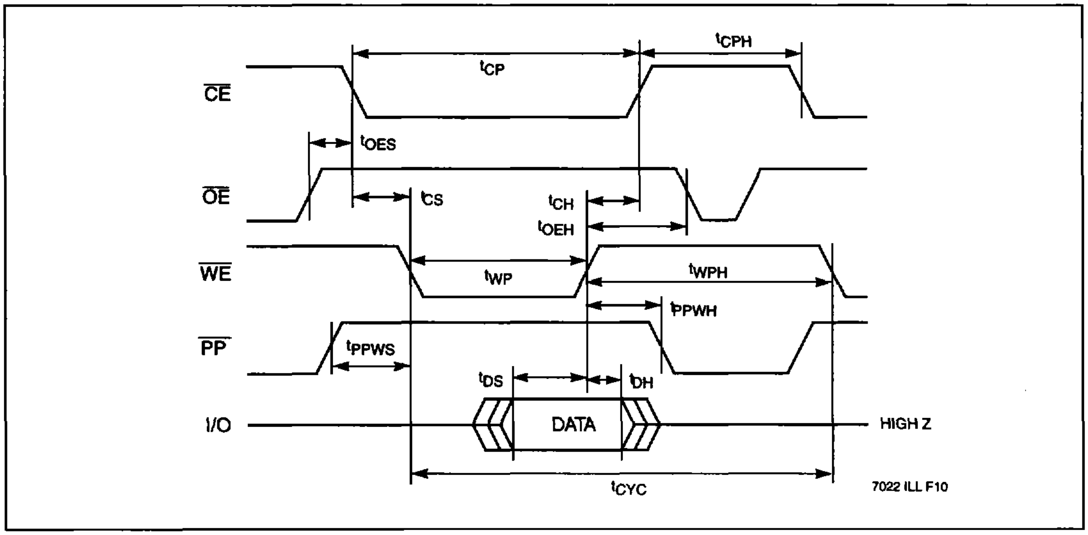
Notes: (5) t_{NVPC} is the time from the falling edge of $\overline{OE}$ or $\overline{CE}$ (whichever occurs last) of the second read cycle in the "start nonvolatile program cycle" sequence until the self-timed, internal nonvolatile program cycle is completed.
(6) Data is latched into the X84F128/064 on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.
(7) Periodically sampled, but not 100% tested.

CE Controlled Program Cycle



WE Controlled Program Cycle



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ORDERING INFORMATION

X84F128/064 X X –X

Device — X84F128/064

V_{CC} Range
Blank = 2.4V to 3.6V
5 = 4.5V to 5.5V

Temperature Range
Blank = Commercial = 0°C to +70°C
I = Industrial = –40°C to +85°C
E = Extended = –20°C to +85°C

Packages:

X84F064
P = 8-Lead Plastic DIP
S = 14-Lead SOIC

X84F128
P = 8-Lead Plastic DIP
S = 16-Lead SOIC