National Semiconductor

PRELIMINARY
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DP8469 Synchronizer/2,7 Endec

General Description

The DP8469 data synchronizer/2,7 endec is intended for use in magnetic disk, optical disk, or tape drives during reading and writing operations. The device utilizes a fully integrated PLL to synchronize 2,7 serial code and convert data between one of several hard and soft sectored versions of 2,7 RLL (Run Length Limited) and serial NRZ code format. The DP8469 synchronizer/endec incorporates both the DP8459 synchronizer and the DP8463 2,7 code endec functions together in a 28-pin PCC package.

In the read mode, the device receives 2,7 RLL coded data from the drive's pulse detector, resynchronizes it, and then decodes the data to NRZ format for output to the controller.

In the write mode, the device receives NRZ data from the disk controller, encodes it in one of nine different 2,7 RLL hard/soft sectored formats, and then sends the data out to the drive with optional 3T precompensation adjustments.

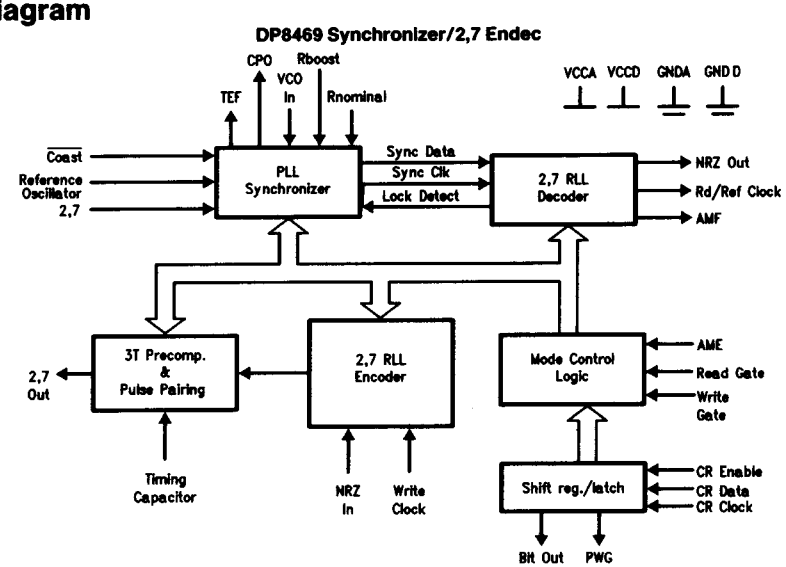
The device generates and recognizes the following 2,7 address mark formats; ESDI, ESDI noise tolerant, SMD, SMD noise tolerant, ST506(A), hard sector and three variations of ESDI, IBM, & ST506(B) optimized for the DP8466 controller. The address mark format is selected by 4 bits in a control register. A user defined variable-length preamble pattern can be used with any of the address mark modes. The pattern type, 3T or 4T, is set with one control register bit, and the preamble length is defined by the input NRZ data.

The synchronizer provides a dual gain phase locked loop which offers a high bandwidth mode for preamble lock acquisition and a low bandwidth mode for reading data. Two ports are provided for the PLL filter to enable use of higher order filter designs. The synchronizer has a Zero-Phase-Start feature which helps to minimize acquisition time in both read and write modes. A PHASE COMPARATOR TEST function is also provided for observation of PLL loop dynamics and determination of average media bit shift. The 2,7 OUTPUT pin provides the logical OR of the phase comparator's pump up and down outputs when programmed for Test Mode 1 operation. (Continued)

Features

- NRZ to 2,7 RZ RLL encoding/decoding
- 3T and 4T preamble generation/detection
- 1.5 Mbit/s to 24 Mbit/s data rates
- User specified preamble length
- ESDI, SMD, and ST506 soft sectoring
- Hard sectoring
- Fully integrated dual-gain PLL
- Zero-Phase-Start lock sequence
- Digitally controlled window strobe
- Digital write precompensation
- TTL compatible inputs and outputs
- +5V supply
- Packaging availability:
  — 28-pin Plastic Chip Carrier (PCC)
  — 40-pin TapePak

Block Diagram



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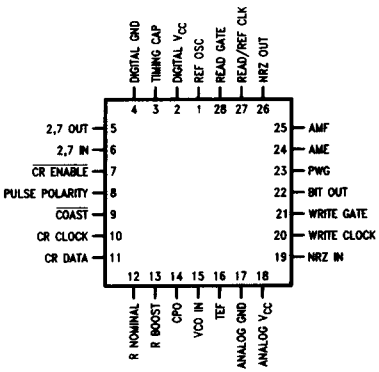
Connection Diagrams

PCC



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Top View

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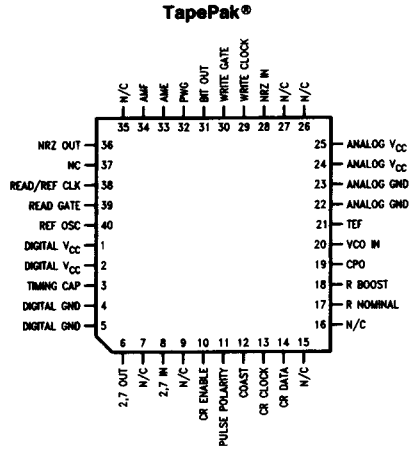

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Top View

General Description (Continued)

A precise synchronization window is provided on chip using a self-aligned silicon delay line which remains accurate independent of temperature, power supply, external components and IC process variations. A strobe early/late function is provided which allows the synchronization window to be digitally adjusted to allow for error recovery or margin testing. The window can be shifted up to 20% in steps of 1.25% by 5 bits in a control register.

The synchronizer's data rate range is 1.5 Mbit/s to 24 Mbit/s. This range is divided into four operating regions each providing a 2 to 1 span in VCO frequency. Selection of one of the four data rate regions is controlled by two bits in a control register.

The READ/REFERENCE CLOCK provides both a read and write clock source for the controller. In read mode, once READ GATE has gone active and the Zero-Phase-Start sequence has been completed, the READ/REFERENCE CLOCK outputs the VCO divided by two. In the non-read mode, READ/REFERENCE CLOCK outputs REFERENCE OSCILLATOR divided by two. The circuitry incorporates a non-glitching multiplexer to ensure no erroneous clock pulses occur during the switch between input sources.

A digital precompensation feature is provided for write operations to compensate for bit shift due to data crowding on the media. The device will precompensate 3T code which is adjacent to greater than 3T code by selecting 1 of 6 bit shifted steps determined externally on the TC pin with an RC time constant set by the user.

The BIT-OUT output directly follows the logic level programmed in Control Register bit #10. By connecting BIT-OUT to the TC pin through a resistor, it is possible to have the controller select different pre-comp ranges via the control register.

Pin Descriptions

POWER SUPPLIES

ANALOG V_{CC}: Analog positive 5V supply, ±5%.

DIGITAL V_{CC}: Digital positive 5V supply, ±5%.

ANALOG GND: Analog negative supply pin.

DIGITAL GND: Digital negative supply pin.

INPUTS FROM CONTROLLER

NRZ IN (NRZI): NRZI input from the controller. Data is encoded and written to the disk in 2,7 format on the positive edge of WRITE CLOCK. NRZI is held LOW during the Preamble and Address fields, and transitioned HI at the start of data encoding.

Non-ST506 modes: NRZI must remain LOW throughout the address mark field and transition HI for a minimum of two NRZ bits to terminate preamble and start the controller sync byte.

ST506 modes: NRZI must remain LOW through both the address mark and preamble fields, and then transition HI for a minimum of one NRZ bit to start the controller sync byte.

WRITE CLOCK: Clock input from the controller synchronized with the NRZ IN data.

WRITE GATE (WG): A mode control input from the controller which allows the writing of header and data to the disk when active HI and prohibits writing of header or data when LOW.

ADDRESS MARK ENABLE (AME): AME must be held HI while writing an Address Mark. During an ESDI or SMD read operation, the AME pin must be held HI to search for an address mark. Termination of the AME HI level will reset AMF to the LOW state. The AME logic is not relevant during non ESDI and SMD read operations.

Pin Descriptions (Continued)

INPUTS FROM CONTROLLER (Continued)

READ GATE (RG): A mode control input from the disk controller. In ESDI and IBM modes, RG should not be transitioned HI until AMF is active HI. In SMD and ST506 modes, RG is qualified to the synchronizer internally as follows:

ST506: device must recognize 4 consecutive 3T or 4T preamble patterns.

SMD: AMF goes active HI.

In Hard Sector mode, RG should not be transitioned HI until the Index Sector Gap is found. After RG goes HI, the synchronizer locks to the 2,7 INPUT data rate using a Zero Phase Start frequency lock routine. When RG goes LOW, the synchronizer locks to the Reference Oscillator (REG OSC) using a Zero Phase Start frequency lock routine. RG timing is allowed to be fully asynchronous.

OUTPUTS TO CONTROLLER

ADDRESS MARK FOUND (AMF): An active HI output for the controller to indicate the first 2,7 pulse beyond a valid address mark has been found. In the ESDI and SMD modes, AMF remains HI until AME transitions LOW. In the ST506A mode, AMF stays HI until RG is deasserted. In the DP8466 modes, ESDI, IBM and ST506B, AMF returns LOW after the second 2,7 pulse is encountered.

NRZ OUTPUT (NRZO): Decoded output data for the controller that is strobed on the positive transition of READ REF CLK. Control register bit 11 selects either TRI-STATE® or totem pole output. Bit 11 = LOW sets NRZO to active totem pole output, and Bit 11 = HI sets NRZO to TRI-STATE output.

READ REF CLK (R/RCLK): This supplies the controller clock source. In read mode, after the Zero Phase Start sequence is completed, R/RCLK issues the VCO divided by two signal. The NRZO is synchronized with this clock. In the non-read mode, R/RCLK will issue the REF CLK input signal divided by two.

INPUTS/OUTPUTS TO DRIVE

2,7 OUTPUT: Output 2,7 Return-to-Zero (RZ) data for recording onto the storage media. Each positive edge represents a single recorded code bit. The 2,7 OUTPUT active transition edge can be shifted by specific controllable time steps by setting control register bits 7,6,5. Only certain minimum 3T patterns are affected.

2,7 INPUT: Incoming data derived from the storage media, issued from a pulse detector circuit. Each positive edge represents a single recorded bit.

PULSE POLARITY (PP): Input derived from DP8464/8 pulse detector's channel polarity output telling the pulse pairing circuitry which pulse to shift.

EXTERNAL SOURCES

REFERENCE OSCILLATOR (REF OSC): A reference frequency input *required* for DP8469 operation. The signal must be crystal or servo derived (accurate and highly stable), and at a frequency approximately equal to the 2,7 code rate (i.e., twice the NRZ data rate).

$\overline{\text{CR ENABLE}}$ ($\overline{\text{CRE}}$): When active LOW, $\overline{\text{CRE}}$ permits the loading of mode information via CRD and CRC. Data is latched into the part when $\overline{\text{CRE}}$ is transitioned HI. This input is also used to set test mode conditions as described in the Test Mode Operation section.

$\overline{\text{COAST}}$ ($\overline{\text{CST}}$): The control input for a coast function which may be activated when RG is either HI or LOW. When the $\overline{\text{CST}}$ input is LOW, the phase comparator is disabled and held in a cleared state, allowing the VCO to coast regardless of the 2,7 code input or reference oscillator activity. No other circuit functions are disturbed. When the $\overline{\text{CST}}$ is inactive HI, the synchronizer operates normally.

CR CLOCK (CRC): Positive edge triggered clock for the 24-bit control register. This input is also used to set test mode conditions as described in the Test Mode Operation section.

CR DATA (CRD): Data input for the 24 bit control register that selects the strobe window, precompensation and pulse pairing bit shift, data rate range, and address mark modes. This input is also used to set test mode conditions as described in the Test Mode Operation section.

ANALOG SIGNAL PINS

RNOMINAL (R_{NOM}): A resistor is tied from this pin to V_{CC} to set the *nominal* operating current. The current is internally multipled by 2 for charge pump use. This pin is also used to load the test modes as described in the Test Mode Operating section.

RBOOST (R_{BST}): A resistor is tied from this pin to V_{CC} to set the chrage pump *boost* (or adder) current, which is multiplied by 2 internally for use by the charge pump. The R_{BST} resistor is electrically paralleled with the R_{NOM} resistor until either RG is passed to the synchronizer, or preamble lock is acquired. This selection is made with control bit 18;

Bit 18 = HI: forces synchronizer switch to Low Gain on assertion of RG.

Bit 18 = LOW: forces synchronizer switch to Low Gain when preamble lock is acquired.

RBOOST (R_{BST}) (Continued): ST506 operating modes are special in that the switch to Low Gain is forced on the assertion of RG regardless of the state of bit 18. If no boost current is desired, a high value resistor must be tied to this pin to ensure its level is not allowed to drop below V_{IH} = 2V and activate the production test mode circuitry. This pin is also used for the test modes as described in the Test Mode Operating section.

CHARGE PUMP OUT (CPO): The output of the high-speed bi-directional current source switching circuitry of the charge pump. The external, passive PLL filter network is established between this pin, the VCO Input and ground.

VCO IN (VCOI): The high-impedance control voltage input to the voltage controlled oscillator (VCO). The external, passive PLL filter network is established between this pin, CPO pin and ground.

Pin Descriptions (Continued)

ANALOG SIGNAL PINS (Continued)

TIMING EXTRACTOR FILTER (TEF): Connection pin for external, passive components employed to stabilize the delay line timing extraction circuitry.

Note: The delay line accuracy *is not* a function of external component values or tolerances.

OTHER OUTPUTS

RC ADJ: An open collector Bipolar output which can be used to adjust the precompensation or pulse pairing external RC time constants. By connecting a resistor between the RC ADJ pin and the TC pin, a different RC timing constant can be used between precompensation and pulse pairing. RC ADJ is the logical true or complement of WG depending on the state of register bit 8:

Bit 8 = HI: RC ADJ is inverted from WG.

Bit 8 = LOW: RC ADJ follows WG.

BIT OUT: An undedicated open collector Bipolar output whose state is set using bit 10 in the control register. This output can be used for any purpose, including adding extra RC ranges to the precompensation and pulse pairing circuitry. Window strobe adjustments can be performed by connecting a resistor between BIT OUT and the CPO output pin.

Circuit Operation

CONTROL REGISTER OPERATION

The DP8469 is initialized by loading the desired mode selections, such as address mark format and 3T/4T Preamble pattern, via the CR DATA (CRD), CR CLOCK (CRC) and $\overline{\text{CR ENABLE}}$ ($\overline{\text{CRE}}$) inputs. Loading is accomplished by taking $\overline{\text{CRE}}$ active LOW, and clocking in the mode selection data on the positive going edge of CRC. The modes are latched in when $\overline{\text{CRE}}$ is transitioned HI. The selections are indicated in the 24-Bit Control Register section. The test modes are also loaded using CRD, $\overline{\text{CRE}}$, CRC as explained in the special Test Mode Operation section.

SYNCHRONIZER OPERATION

In non-read mode, the DP8469 PLL is locked to the REFERENCE OSCILLATOR signal (REF OSC). This permits the VCO to remain at a frequency very close to the media bit-rate while the PLL is "idling" and thus will minimize the frequency step and associated lock time requirement encountered at the initiation of lock to 2,7 INPUT data. When READ GATE is transitioned LOW to terminate the Read mode, a Zero-Phase-Start and frequency acquisition sequence is employed to insure lock. The REF OSC signal is also used during this time to set the time delay of the internal delay line. Note that this requires the REF OSC signal to be present *at all times* at a stable and accurate frequency for proper DP8469 operation.

In non-ST506 modes of operation, after the assertion of READ GATE (fully asynchronous, with no timing requirements), and following the completion of two subsequent VCO cycles, the DP8469 VCO is stopped momentarily. The VCO is then restarted in accurate phase alignment with the second data bit which arrives subsequent to the VCO pause. This minimization of phase misalignment between the 2,7 READ DATA and the VCO (referred to as Zero-Phase-Start or ZPS) significantly reduces the data lock acquisition time.

The DP8469 incorporates a preamble-specific acquisition feature which is employed for all non-ST506 modes of operation where READ GATE is asserted only within a preamble. In these modes, after READ GATE is asserted HI, the device will be forced to lock to the exact 3T or 4T selected preamble frequency. The frequency discriminating action of the PLL provided in these modes produces a lock-in range equivalent to the available VCO operating range and thus eliminates the possibility of fractional-harmonic lock. Windowing (pulse-gate action; see Pulse Gate section) is prevented. (Application Note AN-414 has an explanation of typical false lock modes.)

In the ST506 modes of operation, at the assertion of READ GATE, the 2,7 IN data pattern is first sampled asynchronously and the synchronizer ZPS lock-on sequence is prevented until eight preamble patterns are recognized. The synchronizer only operates Low Bandwidth Gain, and in a phase lock mode (pulse gate action) during the ST506 operation.

In the non-ST506 modes, the user is provided, the option of an elevated PLL bandwidth during preamble acquisition for an extended capture range. An R_{BOOST} pin is provided to allow for an increase in charge pump gain over and above the level set by the $R_{NOMINAL}$ pin. The net current through either $R_{NOMINAL}$ or $R_{BOOST}//R_{NOMINAL}$ is multipled internally by 2 for use by the charge pump. The user should connect a high value resistor to R_{BOOST} if an elevated PLL bandwidth is not desired to ensure the pin does not fall below the 2V test inactive HI logic threshold.

The READ/REFERENCE CLOCK (R/R CLK) issues a waveform derived from the REF OSC input during the non-read mode (i.e., READ GATE inactive). In the read mode, following the assertion of READ GATE, the completion of the ZPS sequence, and in the case of ST506 modes, the recognition of a short 3T or 4T preamble pattern, R/R CLK issues a waveform derived from the VCO signal. Once data lock is achieved in the read mode and the first bit of the controller Byte Sync field is encountered, the NRZ OUT and R/R CLK outputs are held in a fixed, specified timing relationship. The R/R CLK output switches between input sources without glitches.

The DP8469 provides a $\overline{\text{COAST}}$ control input which serves to clear the phase comparator and disable charge pump action whenever taken to an active, logical-zero level. This function is made available to allow the PLL to be set to free-

Circuit Operation (Continued)

run, undisturbed, while a detectable defect is being read from the media in a region where re-initiation of the lock procedure is impractical (e.g., data field). External data controller circuitry is responsible for the detection of the defect and issuance of the $\overline{\text{COAST}}$ command. For a more detailed explanation of the synchronizer, and loop filter design, please see the DP8459 datasheet.

ENDEC OPERATION

2,7 Encoder: The data encoding path is responsible for generating an address field, preamble field, and the data field. This allows synchronous generation of preamble and data in all cases, insuring the fastest possible PLL lock during readback. The encoder has two modes of operation, ST506 and non-ST506 mode. The primary difference between these two modes is the placement of the fields:

Preamble Field	Address Field	Data Field

ST-506 Mode (Synchronous Type Address Mark)

Address Field	Preamble Field	Data Field

Non ST-506 Mode (Gap Type Address Mark)

In the ST506 modes, the controller issues a WRITE GATE (WG) command to begin the preamble generation. During the Preamble and Address Mark fields, NRZ IN is blanked. Preamble length is user defined since the ENDEC will continue to generate preamble until Address Mark Enable (AME) is asserted. Assertion of AME terminates the preamble, generates a Phase Sync (for decoding), and begins the N7V address mark. In both ST506 modes, the AME input *must be held high for exactly one Byte* (8 bits). The N7V address mark is one byte in length, does not violate the 2,7 code rules, and cannot be generated by the encoder. Immediately following the completion of the Address Mark, NRZ IN is unblanked, and encoded as data. This data must be the controller's sync byte. If the controller requires more then one byte of AME, then both AME and NRZ IN *must be held LOW* during the second byte to insure that during readback the first non-zero data presented to the controller will be a valid Sync Byte. The Sync Byte must begin with a leading "1", however the user has total freedom of the last 7 bits (1------). The encoder continues to encode the data according to the 2,7 code rules until WG is deasserted.

In non-ST506 modes, the controller issues WG to begin the header generation. Normally AME is also issued at the same time. If there is a delay between the assertion of WG and AME, the encoder will begin generating a preamble pattern. Assertion of AME generates the address gap. ESDI and SMD address marks require 3 bytes of AME while the IBM mark only requires 2 bytes of AME. Immediately upon the deassertion of AME, the encoder will begin generating the preamble field. NRZ IN is blanked while AME is asserted. The first non-zero NRZ data following the deassertion of AME *must be the controller's Sync Byte* as any NRZ IN data presented to the encoder after deassertion of AME terminates the preamble, and is encoded. The Sync Byte restrictions are as follows:

3T: 1-------

4T: 11------

For 3T preamble, the Customer has total freedom of the last 7 bits of the Sync Byte, however in the 4T preamble, the Customer has total freedom of only the last 6 bits.

NRZ IN data is internally blanked while AME is asserted as the DP8469 generates its own address mark data depending upon the type of address mark selected in control register bits 15 to 12. In the ST506 case, NRZ data presented to the DP8469 *immediately after* deassertion of AME *will* be encoded as data, while in the non-ST506 modes, the encoder will return to preamble generation *until the first non-zero* NRZ data following deassertion of AME. The preamble pattern is selected in control register bit 9; HIGH for 3T and LOW for 4T. Once the pattern is selected, it is transparent to the user.

2,7 Decoder: The data readback path is responsible for detecting the address field, preamble field, and finally the data field. The controller issues an active READ GATE (RG) to initiate clock synchronization and 2,7 decoding.

In ST506 mode, the controller first issues RG for the detection of the preamble field. The DP8469 employs a two phase preamble prequalifier on the internal RG. The prequalifier must first find several bytes of valid preamble pattern before it passes RG to the synchronizer and enables the standard preamble detector. In the event there is enough valid looking data to qualify as a preamble, the synchronizer is switched into phase-only low gain mode on the assertion of RG to guarantee that it can pass through any subsequent Write Splice without problems. The synchronizer employs a Zero Phase Start circuit to minimize its lock time.

Once preamble has been located (thirty-one 3T patterns or fifteen 4T patterns) the decoder begins searching for the N7V address mark. Phase-sync and address mark detection are accomplished at the same time, and the decoder then unblanks the NRZ OUT at the start of Controller's Sync Byte.

The non-ST506 modes (commonly called "Gap Type") breakdown into two groups:

a) ESDI and IBM modes where the controller does not assert RG until after AMF signifies the start of the Preamble.

b) SMD mode where the controller asserts RG prior to AMF, and the ENDEC is responsible for blocking RG to the synchronizer until the Preamble field has been found.

In both cases, the address mark precedes the preamble field. The controller instructs the DP8469 to search for the address mark, a 2 NRZ byte gap, transitionless ESDI and SMD gaps and an IBM gap with 3 specific transitions. Once the gap has been located, the AMF output signals the controller, and the controller responds with assertion of RG in ESDI and IBM. In the SMD mode, RG is internally qualified with AMF, providing the same function.

Once RG has been passed to the synchronizer, the same thirty-one 3T or fifteen 4T preamble pattern requirements must be met before the decoder can look for the Phase Sync, and unblank. The first non-zero NRZ OUT data is the controller's Sync Byte.

Circuit Operation (Continued)

Both the encoder and decoder follow the encoding rules as shown in the table below:

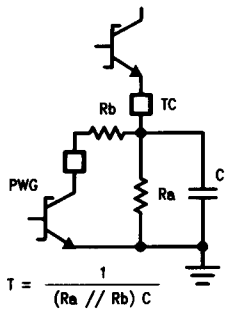
IBM 2,7 Conversion Table

NRZ				2,7 Code						
	0	0	0			0	0	0	1	0	0
		1	0					0	1	0	0
	0	1	0			1	0	0	1	0	0
0	0	1	0	0	0	1	0	0	1	0	0
		1	1					1	0	0	0
	0	1	1			0	0	1	0	0	0
0	0	1	1	0	0	0	0	1	0	0	0

2 = Minimum # of Zeros between adjacent Ones
7 = Maximum # of Zeros between adjacent Ones
1 = NRZ bits for relative conversion ratio
2 = Code bits for relative conversion
3 = # of different length code words

Precompensation

The Precomp circuitry uses the same basic delay-line technique to provide controllable time-delay steps. The user applies the necessary external RC components to the TC pin to provide the desired time step sizes. By using the BIT OUT and PWR outputs, different RC values can be used for different circumstances ... Programming Bit 8 = LOW sets the PWG output to follow WRITE GATE, while programming Bit 8 = HI sets PWG to the logical inverse of WRITE GATE. This allows complete freedom in setting the precomp time constants independently for different Write channel anomolies such as inner vs outer track recording densities.



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Bit-crowding on the disk results in a maximum frequency pattern (3T) timing error to the data written on the disk. Whenever the 3T pattern is adjacent to a non-3T pattern, the two 3T bits are pushed apart, resulting in a time skew during readback. The precompensation feature allows the user to adjust the 3T pattern on a cycle-by-cycle basis to correct for this problem.

Precompensation Bit Patterns

Bit t−3	Bit t−2	Bit t−1	Target Bit t	Bit t+1	Bit t+2	Bit t+3
0	0	0	No Shift	0	0	0
1	0	0	No Shift	0	0	1
1	0	0	Shift Early	0	0	0
0	0	0	Shift Late	0	0	1

Test Mode Operation

The DP8469 provides 7 special test modes. With the exception of the Phase Comparator Test (PCT), SYNC DATA and SYNC CLK, these special test modes are used for production testing. The PCT data is the logical OR'ing between charge Pump Up and charge Pump Down, and can be used to examine the locking action of the PLL. The SYNC DATA and SYNC CLK outputs allow window strobe measurements. All together, they will allow the user to fine tune the application to insure minimum jitter during readback. The PCT function is present on the AMF output in test mode 1 (load 001, MSB first). SYNC DATA and SYNC CLK are present in test mode 7 (load 111, MSB first) on the READ/REF CLK and OUTPUT 2,7 outputs respectively.

The test modes are set by a 3 bit test register that is accessed via the R_{BOOST} and $R_{NOMINAL}$ inputs. In an application, both R_{BOOST} and $R_{NOMINAL}$ are held above the 2V threshold clearing the test register to mode 0, and allowing both HI and LOW gain PLL action. This insures that the device will always power-up in the normal operating mode. By pulling R_{BOOST} below the 2V threshold, the test register can now accept 3 bits of data that will decode to one of seven test modes (the eighth mode, 000, is normal operation). The $R_{NOMINAL}$ input is used to select between loading the 24 bit control register and the 3 bit test register; $R_{NOMINAL}$ = HI sends the data to the 24 bit register while $R_{NOMINAL}$ = LOW sends the data to the 3 bit test register. The test register is then loaded using $\overline{CRE}$, CRC, and CRD. After loading the test register, first return $\overline{CRE}$ = HI *to protect the data in both the Control Register, as well as the data in the Test Register.* It is required to set $\overline{CRE}$ = HI *before changing the state of any other control input* (including both $R_{NOMINAL}$ and R_{BOOST}) in order to prevent any internal switching from generating false clocks and changing the state of any register data. Next, return $R_{NOMINAL}$ HI to allow normal synchronizer operation. Maintain R_{BOOST} LOW to preserve the test mode. This combination will only allow low gain PLL action during testing. CRD and CRC must also be returned LOW, and held there during testing as they are used as special testing inputs.

The action of pulling $R_{NOMINAL}$ low disables the charge pump, and drives the VCO to the lower clamp limit. For any test where the PLL loop needs to run, such as window strobe tests, the test mode must be loaded before the loop is locked. First, load the test register and return $\overline{CRE}$ HI, and then $R_{NOMINAL}$ HI. Then reload the control register, and return $\overline{CRE}$ HI. Finally, exercise the device starting with RG deasserted, and running the device through the complete Read cycle. Note that for the device to remain in test mode, R_{BOOST} must be held low, and this eliminates the high gain mode of operation for the synchronizer. To observe the synchronizer in a high gain mode, replace $R_{NOMINAL}$ with a resistor equivalent to the parallel combination of $R_{NOMINAL}$ and $R_{NOMINAL}$. Do not exceed the 1 mA maximum total input current specification for the $R_{NOMINAL}$ pin.

DP8469 24 Bit Control Register

Control Register is Loaded MSB (Bit 23) First, and LSB (Bit 0) Last.

23 MSB	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 LSB
Window Strobe					Gain Control	VCO Frequency Range Select		Address Mark Mode Select				NRZ Hi-Z Enable	Bit Out Hi	3T Preamble	RC Adjust	Precomp Step Select			Invert 2,7 Out	Edge Polarity	Pulse Pairing Step Select		

Pulse Pairing Delay Steps

Pulse Pairing Early/Late 3*	2	1	0	Delay Step % Bit Shift
X	0	0	0	Bypassed
X	0	0	1	0.0
0 / 1	0	1	0	± 2.5*
0 / 1	0	1	1	± 5.0*
0 / 1	1	0	0	± 7.5*
0 / 1	1	0	1	±10.0*
0 / 1	1	1	0	±12.5*
0 / 1	1	1	1	±15.0*

*Bit 3 selects which flux change from the Pulse Detector is Pulse Pairing Corrected.

Control Register Bit Definitions for Bits 4, 8, 9, 10, 11, 18

Bit 4	2,7 Output	0	True
		1	Inverted
Bit 8	RC ADJ Follows	0	$\overline{\text{WRT GATE}}$
		1	WRT GATE
Bit 9	3T/4T Preamble	0	4T
		1	3T
Bit 10	BIT OUT	0	Active LOW
		1	Inactive HI
Bit 11	NRZ OUT	0	Totem Pole
		1	TRI-STATE
Bit 12	PLL Switch to Low Gain	0	READ GATE
		1	LOCK DETECT

Precomp Delay Steps

Precomp Early/Late 2	1	0	Delay Step % Bit Shift
0	0	0	Bypassed
0	0	1	0.0
0	1	0	± 2.5*
0	1	1	± 5.0*
1	0	0	± 7.5*
1	0	1	±10.0*
1	1	0	±12.5*
1	1	1	±15.0*

Control Register # 15	14	13	12	Address Mark Mode
0	0	0	0	ESDI
0	0	0	1	SMD
0	0	1	0	ESDI*
0	0	1	1	N/A
0	1	0	0	ST506A
0	1	0	1	ST506B
0	1	1	0	HARD
0	1	1	1	IBM*
1	0	0	0	ESDI NT
1	0	0	0	SMD NT

*DP8466 Compatible

VCO Freq Range

Bits 15	14	Freq Range (Mbits/sec)
0	0	1.5–3
0	1	3–6
1	0	6–12
1	1	12–24

Control Register # 23	22	21	20	19	Strobe Word	Typical Window Strobe
0	1	1	1	1	−15	$-0.270\times T_{vco}$
0	1	1	1	0	−14	$-0.252\times T_{vco}$
0	1	1	0	1	−13	$-0.234\times T_{vco}$
0	1	1	0	0	−12	$-0.216\times T_{vco}$
0	1	0	1	1	−11	$-0.198\times T_{vco}$
0	1	0	1	0	−10	$-0.180\times T_{vco}$
0	1	0	0	1	−9	$-0.162\times T_{vco}$
0	1	0	0	0	−8	$-0.144\times T_{vco}$
0	0	1	1	1	−7	$-0.126\times T_{vco}$
0	0	1	1	0	−6	$-0.108\times T_{vco}$
0	0	1	0	1	−5	$-0.090\times T_{vco}$
0	0	1	0	0	−4	$-0.072\times T_{vco}$
0	0	0	1	1	−3	$-0.054\times T_{vco}$
0	0	0	1	0	−2	$-0.036\times T_{vco}$
0	0	0	0	1	−1	$-0.018\times T_{vco}$
0	0	0	0	0	0	0
1	0	0	0	0	0	0
1	0	0	0	1	1	$0.018\times T_{vco}$
1	0	0	1	0	2	$0.036\times T_{vco}$
1	0	0	1	1	3	$0.054\times T_{vco}$
1	0	1	0	0	4	$0.072\times T_{vco}$
1	0	1	0	1	5	$0.090\times T_{vco}$
1	0	1	1	0	6	$0.108\times T_{vco}$
1	0	1	1	1	7	$0.126\times T_{vco}$
1	1	0	0	0	8	$0.144\times T_{vco}$
1	1	0	0	1	9	$0.162\times T_{vco}$
1	1	0	1	0	10	$0.180\times T_{vco}$
1	1	0	1	1	11	$0.198\times T_{vco}$
1	1	1	0	0	12	$0.216\times T_{vco}$
1	1	1	0	1	13	$0.234\times T_{vco}$
1	1	1	1	0	14	$0.252\times T_{vco}$
1	1	1	1	1	15	$0.270\times T_{vco}$

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	−0.5V to +7.0V
Inputs (Note 1)	
TTL	−0.5V to +7.0V
CMOS	−0.5V to +5.5V
Outputs (Note 1)	
TTL	−0.5V to +7.0V
CMOS	−0.5V to +5.5V
Input Current Maximum ($R_{NOMINAL}$, R_{BOOST}, CPO, VCOI, TEF)	±2 mA
Storage Temperature	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
ESD Susceptibility	1500V

Recommended Operating Conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{CC}	Supply Voltage			4.75	5.00	5.25	V
T_A	Ambient Temperature			0	25	70	°C
V_{IH}	High Logic Level Input Voltage			2.0			V
V_{IL}	Low Logic Level Input Voltage					0.8	V
I_{OH}	High Logic Level Output Current	I_{OH1}	2,7 Output			−400	µA
		I_{OH2}	AMF, NRZ OUT, RD/REF CLK			−2.0	mA
		I_{OH3}	AMF, NRZ OUT, RD/REF CLK			−20	µA
I_{OL}	Low Logic Level Output Current	I_{OL1}	2,7 Output			20	mA
		I_{OL2}	RC ADJ, BITOUT			8.0	mA
			AMF, NRZ OUT, RD/REF CLK			4.0	mA
		I_{OL3}	AMF, NRZ OUT, RD/REF CLK			20	µA
$I_{RC\ ADJ}$	Pulse-Pairing/Pre-Compensation Maximum External Load Current			0.0		−16	mA
f_{NRZ}	Operating Data Rate Range			1.5		24	Mb/s
t_{mpwr}	Minimum Pulse Width of REF CLK, HIGH or LOW			10			ns
t_{mpwi}	Minimum Pulse Width of INPUT 2,7, HIGH			20			ns
t_{mpww}	Minimum Pulse Width of WRT CLK, HIGH or LOW			20			ns
t_{mpwcc}	Minimum Pulse Width of CRC, HIGH or LOW			40			ns
t_{mpwc}	CONTROL REGISTER CLOCK Minimum Pulse Width HIGH or LOW (Note 2)			40			ns
t_{scec}	CONTROL REGISTER CLOCK Setup-Time with respect to CRC (Note 2)			80			ns
t_{hcec}	CONTROL REGISTER ENABLE Hold-Time with respect to CRC (Note 2)			80			ns
t_{scdc}	CONTROL REGISTER DATA Setup-Time with respect to CRC (Note 2)			40			ns
t_{hcdc}	CONTROL REGISTER DATA Hold-Time with respect to CRC (Note 2)			40			ns
I_{CPIN}	Combined R_{NOM} and R_{BOOST} Input Current					1000	µA

Note 1: Bipolar Inputs: REF CLK, $\overline{COAST}$, R_{NOM}, R_{BOOST}
Bipolar Outputs: TC, 2,7 OUT, RC ADJ, BITOUT
CMOS Inputs: 2,7 IN, $\overline{CRE}$, CRD, CRC, PULSE POL, NRZ IN, WRT CLK, WRT GATE, AME, READ GATE
CMOS Outputs: AMF, NRZ OUT, RD/REF CLK
Analog Inputs: TEF, CPO, VCO IN

Note 2: Parameter guaranteed by correlation to characterization data. No outgoing test performed.

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IC}	Input Clamp Voltage (All Inputs)	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH1}	High Level Output Voltage	V_{CC} = Min, I_{OH} = I_{OH1}	V_{CC} − 2V	V_{CC} − 1.6V		V
		V_{CC} = Min, I_{OH} = I_{OH2}	3.5			V
		V_{CC} = Min, I_{OH} = I_{OH3}	V_{CC} − 0.1V			V
V_{OL1}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = I_{OL1}			0.5	V
		V_{CC} = Min, I_{OL} = I_{OL2}			0.4	V
		V_{CC} = Min, I_{OL} = I_{OL3}			0.1	V
I_{OZ}	Maximum TRI-STATE Leakage (Note 1)	V_{CC} = Max, 0.4V ≤ V_O ≤ 2.7V			±2.0	μA
I_{CEX}	Open-Collector Leakage (Note 2)	V_{CC} = Max, V_O = Max			−100	μA
I_{IH}	High Level Input Current (Note 3)	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current (Note 3)	V_{CC} = Max, V_I = 0.4V			−200	μA
I_{IN}	Maximum Input Current (Note 4)	V_{CC} = Max, V_{IN} = V_{CC} or GND	−1		+1	μA
I_O (Note 5)	Output Drive Current OUTPUT 2,7	V_{CC} = Max, V = 2.125V	−12		−110	mA
	TC Pin (Note 6)	V_{CC} = Max, V = 2.125V	−36			mA
I_{CPO}	Charge Pump Output Current (K1)	100 ≤ I_{RP} ≤ 1000 (Note 7)	1.7 I_{RP}	2.0 I_{RP}	2.5 I_{RP}	μA
$I_{CPO-OFF}$	Charge Pump Output Inactive Current	100 ≤ I_{RP} ≤ 1000 (Note 7)	−0.85		+0.85	μA
I_{VCOI}	VCOI Input Leakage Current	VCOI Voltage 1.5V	−0.25		+0.25	μA
V_{RNOM}	Voltage Across R-NOM Resistor	1.2 kΩ ≤ R_{NOM} ≤ 12 kΩ	Typ − 18%	0.26 V_{CC}	Typ + 18%	V
V_{RBST}	Voltage Across R-BOOST Resistor	1.2 kΩ ≤ R_{BOOST} ≤ 12 kΩ	Typ − 18%	0.26 V_{CC}	Typ + 18%	V
I_{CC1}	Supply Current, Nominal Strobe	V_{CC} = Max (Note 8)			190	mA
I_{CC2}	Supply Current, Early Strobe	V_{CC} = Max, (Note 9)			TBD	mA

Note 1: Applies to the TRI-STATE output NRZ OUT with CTRL BIT 11 set HI, and WRT GATE HI.

Note 2: Applies to the Bipolar outputs: RC ADJ, BITOUT.

Note 3: Applies to the Bipolar inputs: REF CLK, $\overline{COAST}$, R_{NOM}, R_{BOOST}.

Note 4: Applies to the CMOS inputs: INPUT 2,7, $\overline{CRE}$, CRD, CRC, PULSE POL, NRZ IN, WRT CLK, WRT GATE, AME, READ GATE.

Note 5: This represents approximately one-half of the true short-circuit output current, I.

Note 6: This only applies to the TC Open Emitter output. Do not exceed 100 mA for more than 0.1 sec.

Note 7: I_{RP} = I_{NOM} + I_{BOOST}

Note 8: I_{CC1} is measured with the window strobe set at nominal timing (Register Bits 23 through 19 = 0,0,0,0,0); VCO operating at the maximum allowed frequency within any given range selection.

Note 9: I_{CC2} is measured with the window strobe set to the maximum early timing (Register Bits 23 through 19 = 0,1,1,1,1); VCO operating at the maximum allowed frequency within any given range selection.

External Component Selection

Symbol	Parameter	Min	Typ	Max	Units
R_{NOM}	Charge Pump Nominal Operating Current Setting Resistor (Note 1)	1.2		12	kΩ
R_{BOOST}	Charge Pump Boost Current Setting Resistor (Note 1)	1.2		∞	kΩ
C_{NOM}	R_{NOM} Bypass Capacitor (Note 2)	0.01			μF
C_{BOOST}	R_{BOOST} Bypass Capacitor (Note 2)	0.01			μF
R_{TC}	Pre-Comp/Pulse Pairing Timing Resistor (Note 3)	0.33		10	kΩ
C_{TC}	Pre-Comp/Pulse Pairing Timing Capacitor (Note 3)	33		10000	pF
$R_{RC\ ADJ}$	Secondary Pre-Comp/Pulse Pairing Timing Resistor (Note 4)	0.33		10	kΩ
$R_{BIT\ OUT}$	Secondary Pre-Comp/Pulse Pairing Timing Resistor (Note 4)	0.33		10	kΩ

Note 1: The minimum allowed value for the parallel combination of R_{NOM} and R_{BOOST} is 1.2 kΩ.

Note 2: C_{NOM} and C_{BOOST} should be high quality, high frequency type.

Note 3: R_{TC} and C_{TC} are both used to establish Pulse-Pairing and Pre-Comp timing on the TC pin.

Note 4: R_{RC} ADJ and R_{BIT} OUT modify the external timing on the TC pin for Read vs Write and inner track adjustability.

AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{STOP}	READ/REF CLK Positive Transitions after READ GATE until Data Lock ZPS Sequence Begins (VCO Freezes) (Notes 1, 2)		2 (Note 4)	3 (Note 4)	—
$t_{RESTART}$	Positive 2,7 INPUT Transitions following VCO Freeze until the VCO Restarts (Note 2)		2	3	—
$t_{READ\ ABORT}$	Number of REF CLOCK Cycles following READ GATE Deactivation until REF CLOCK Lock ZPS Sequence begins (Note 2)			4	—
t_T	Window Truncation (Half Window Loss); 10 and 20 Mbit/s at Strobe Position M = −2 (Note 3)		4% × T_{VCO}		ns
ϕ Linearity	Phase Range for Charge Pump Linearity (wrt VCO) (Note 2)		± π		Radians
K_{VCO}	VCO Gain Constant (Note 6)	1.0 ω_o	1.2 ω_o	1.7 ω_o	rad/sec V
$f_{MAX\ VCO}$	VCO Maximum Frequency; Control Bits 17,16 = 11	70			MHz
t_{ZPSR}	Zero Phase Start Trigger Bit Targeting Accuracy, READ GATE Activation (READ) (Note 5)		2		ns
$\Delta f_{VCO}/f_{RFC}$	Automatic f_{VCO} Range Limiting (Note 2)		50		%
t_{RRCH}	RD/REF CLK Rest Period at Assertion or Deassertion of READ GATE (Note 2)	½		3	T_{VCO}
Encoder Delay	Serial Delay Time in REF CLK Cycles + ns Delay (Note 7)			10 + 100	Cyc + ns
Decoder Delay	Serial Delay Time in REF CLK Cycles + ns Delay			8 + 100	Cyc + ns

AC Electrical Characteristics (Continued)

Symbol	Parameter		Min	Typ	Max	Units
t_{plh} AMF Assertion Time	ST506A and B; After REF CLK following Address Detection (ESDI, SMD, and IBM Gap Type Address are Asynchronous)		50		100	ns
t_{phl} AMF Deassertion Time	ESDI and SMD (Spec & Noise Tolerant); Falling Edge of AME		50		100	ns
	DP8466 Compatible (ESDI and IBM); 2nd Input 2,7 Pulse		50		100	ns
	ST506A: 2nd Input 2,7 Pulse		50		100	ns
	ST506B; Next REF CLK Positive Edge after Falling RD GATE		50		100	ns
t_{mpw}	REF CLK Minimum Pulse Width t_{mpwr+} t_{mpwr-}		5			ns
	INPUT 2,7 Minimum Input Pulse Width t_{mpwi+}		15			ns
	WRT CLK Minimum Input Pulse Widths t_{mpww+} t_{mpww-}		10			ns
$t_{s1/0}$ $t_{h1/0}$	REF CLK Setup and Hold Times to WRT CLK				10	ns
	WRT CLK Setup and Hold Times to AME, NRZ IN, WRT GATE, READ GATE				20	ns
t_{plh}, t_{phl}	Propagation Delay from REF CLK to OUTPUT 2,7				100	ns
$t_{rfc-rrc}$	Propagation Delay from REF CLOCK to RD/REF CLK, READ GATE LOW				50	ns
$t_{skw\pm}$	RD/REF CLK Negative Edge to NRZ OUTPUT Transition				±5	ns
L_{PDT}	Length of Valid Preamble Pattern Required for Internal PREAMBLE DETECTED (Note 2)	3T Preamble	31	32	33	2,7 Input Pulses
		4T Preamble	15	16	17	
t_{Str}	Window Strobe Time Step (M = Hex Value of Bits 22–19 in CONTROL REGISTER; Bit 23 = Sign Bit			M × (1.8%) × T_{RFC}		ns

Note 1: ST506 and SMD modes utilize a Preamble Prequalification routine to guarantee that the synchronizer only locks to data during a valid Preamble Field. This adds a prequalification time to the T_{STOP} time parameters as follows:
ST506: Adds 8 full preamble fields PRIOR to the T_{STOP} parameter
SMD: Adds the time it takes to locate a valid Address Mark, and output a valid AMF

Note 2: Limits are guaranteed by design or correlation to characterization data; no outing testing is performed.

Note 3: *The preliminary DP8469 static window specification, IT, applies only to the factory-tested data rates of 10 Mb/s (Control Bits 17,16 = 01) and 20 Mb/s (17,16 = 10), with the component values as listed for each corresponding data rate in Figures 7* and *12*, test configuration as shown in *Figure 24*, test procedure as shown in *Figure 25*, and strobe word M = −2. Significant variation in IT due to the use of other filters and data rates is not expected.

Note 4: t_{ZPSR} (ZPS Read) gauges the accuracy with which the ZPS circuitry aligns the VCO to the triggering 2,7 INPUT bit internally (i.e., initial phase step) at the completion of a ZPS operation following READ GATE assertion.

Note 5: $I_{IN} = V_{CC}/(4 \times R_{IN})$. $R_{IN} = R_{NOM}$ (HGD High) or $R_{NOM} \| R_{BOOST}$ (HGD Low).

Note 6: Specification for 25°C only. Temperature coefficient = −0.4%/°C.

Note 7: Encoder Serial Delay specified for Pre-Comp set to Bypass Mode (bits 2,1,0 = 000). Non-Bypass Pre-Comp adds 5 REF CLK cycles plus 50 ns.

DP8469 Loop Filter Component Values

Preamble Type	10 Mbit/Sec		20 Mbit/Sec		Units
	3T	4T	3T	4T	
Ref Clk Frequency	20	20	40	40	MHz
NRZ Data Rate	10	10	20	20	Mbit/s
Sync Field Frequency	20	20	40	40	MHz
ζ Min	20	20	40	40	None
ζ Max	20	20	40	40	None
ζ Sync	20	20	40	40	None
Sync Field Frequency	6.7	5	13.3	10	MHz
ω Sync	20	20	40	40	Krad/s
C1 (Main Loop)	0.018	0.018	0.0082	0.082	μF
R1 (Main Loop)	150	150	150	150	Ω
C2 (Main Loop)	510	510	200	200	μF
CT1 (TEF)	0.056	0.056	0.0027	0.027	μF
RT1 (TEF)	68	68	68	68	Ω
TEF Settling Time	9.6	9.6	4.6	4.6	μs

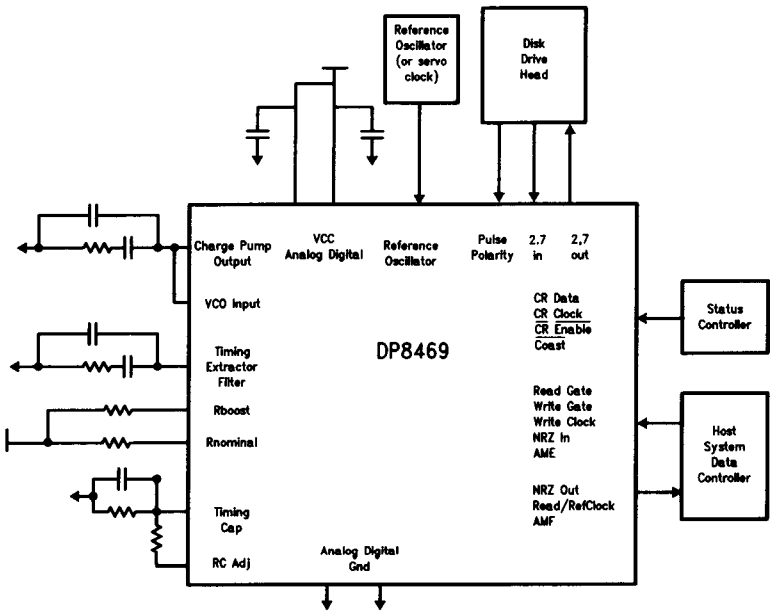
Loop Filter Component Values

Preamble Sync natural frequency has been chosen to yield phase error $\leq$ 0.063 radians (i.e., 1% $\times$ 2π) at sync field end, given a 1% frequency step at READ GATE assertion. $R_{NOM} = R_{BOOST}$ = 2.4k for all loop filter selections. These values apply for Bit 18 = HI, device switches to LOW Gain on assertion of READ GATE.

The TEF settling times are given which indicate time required for the DP8469 to accommodate a change of Strobe setting from nominal selection to either extreme (early/late), or vice versa, to within approximately 1% of final value.

The values listed in the Loop Filter Component Values table are the approximate filter values that are used for Static Window Truncation testing. These values represent a simple solution, yielding only average circuit behavior. Please see National Semiconductor's DP8459 datasheet for a more thorough discussion on loop filter component selection.

Application Diagram



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Encoder Serial Delay Times

Encoder Delay Time Parameter Definitions

t_{es} = Encoder Start time from WRT GATE

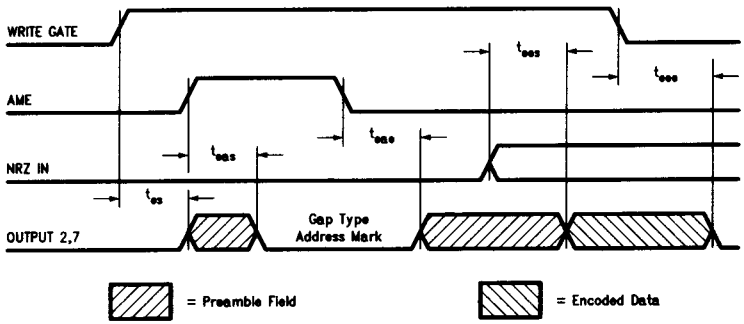
t_{eas} = Encoder Address Mark Start time from assertion of AME

t_{eae} = Encoder Address Mark End time from deassertion of AME

t_{ees} = Encoder Encyrption Start time from first NRZ IN bit

t_{eee} = Encoder Encryption End time from deassertion of WRT GATE

ESDI/SMD/IBM Modes (Gap Type Address Marks)



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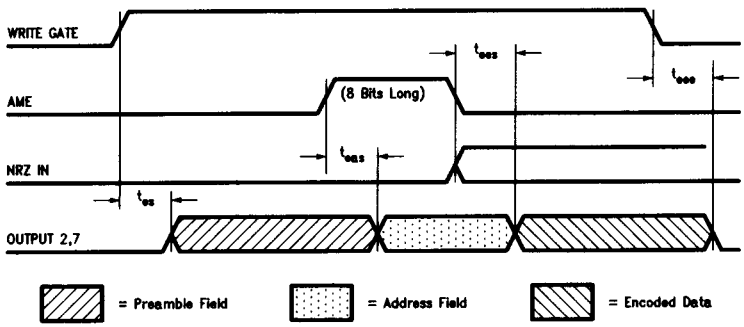
ST506A and B Modes (Synchronous Address Marks)



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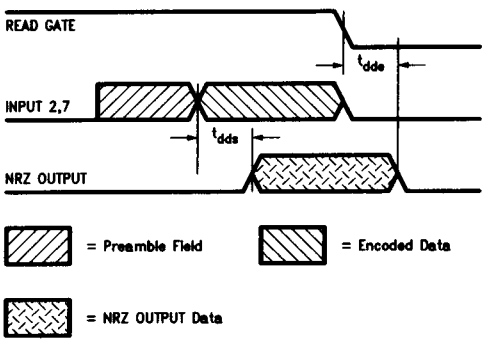
Decoder Serial Delay Times

Decoder Delay Time Parameter Definitions

t_{dds} = Decoder Decryption Start time from INPUT 2,7 data

t_{dde} = Decoder Decryption End Time from deassertion of READ GATE



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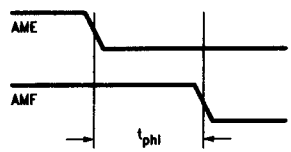
This parameter defines the time delay for a specific INPUT 2,7 pattern to enter the device, and its resulting NRZ output to be present at the NRZ OUTPUT pin.

AMF Assertion Delay Times by Mode

ESDI/SMD Spec and Noise Tolerant Modes



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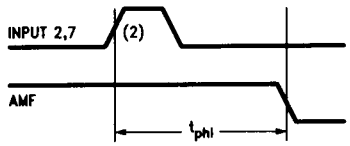
AMF deasserts on the FALLING edge of READ GATE.

AMF Assertion Delay Times by Mode (Continued)

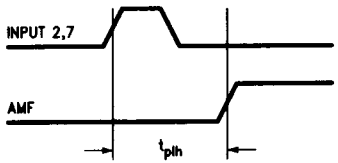
DP8466 Compatible Modes (ESDI and IBM)



TL/F/9386–19

AMF deasserts on the SECOND INPUT 2,7 pulse after assertion

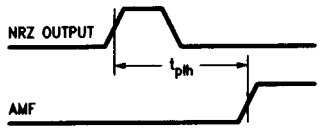
IBM and All ESDI/SMD Modes



TL/F/9386–20

AMF asserts on the FIRST INPUT 2,7 pulse after valid Address Mark

ST506 A and B Modes

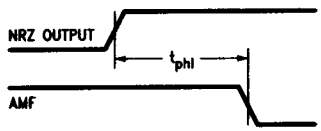


TL/F/9386–22

AMF asserts on the FIRST NRZ OUTPUT pulse after valid Address Mark

ESDI/SMD Spec and Noise Tolerent Modes

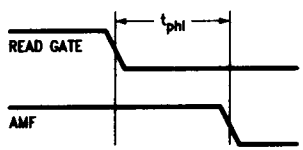
ST506A Mode



TL/F/9386–21

AMF deasserts on the SECOND NRZ OUTPUT pulse after assertion.

ST506B Mode

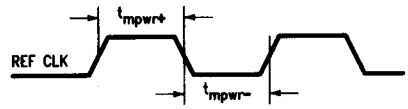


TL/F/9386–23

AMF deasserts on the FALLING edge of READ GATE.

Input Minimum Pulse Widths

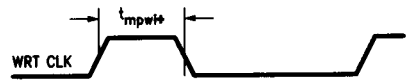
REF CLK Min Pulse Widths



TL/F/9386–24

REF CLK requires minimum input positive and negative pulse width times; including both mpw+ and t_{mpw-}

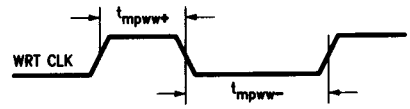
Input 2,7 Min Pulse Widths



TL/F/9386–26

INPUT 2,7 requires a minimum positive pulse width: t_{mpwi+}; there is no minimum negative pulse width spec.

WRT CLK Minimum Pulse Widths

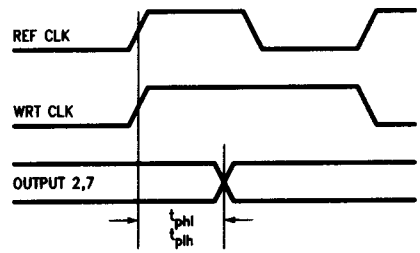


TL/F/9386–27

WRT CLK Input Minimum Positive and Negative Pulse Widths, t_{mpww+} and t_{mpww-}.

Output Propagation Delay Times

REF CLK to OUTPUT 2,7 Propagation Delay Time



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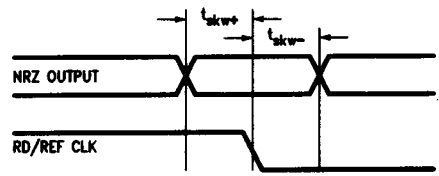
REF CLK to OUTPUT 2,7 for t_{plh} and t_{phl}. Delay time is specified in both REF CLK cycles and ns of delay. WRT CLK edges coincident with REF CLK.

NRZ OUTPUT vs RD/REF CLK T_{skew} for all Read Modes

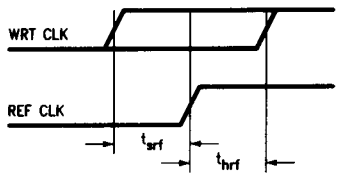


TL/F/9386–28

T_{skw+} defines data changing prior to the clock.
T_{skw-} defines data changing after the clock.

Input Setup and Hold Times

REF CLK Setup and Hold Times



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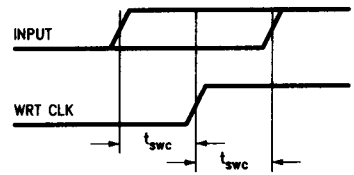
Setup and Hold Times (t_{srf} and t_{hrf}) from REF CLK to WRT CLK.

WRT CLK Setup and Hold Times
NRZ IN, AME, WRT GATE, READ GATE



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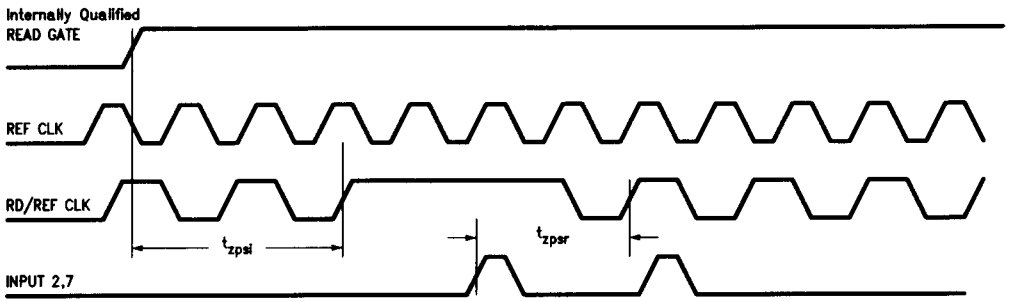
Setup and Hold Times (t_{swc} and t_{swc}) for the four inputs: AME, WG, RG and NRZ IN.

Zero Phase Start Timing Sequence

ZPS Stop and Restart Delay Time



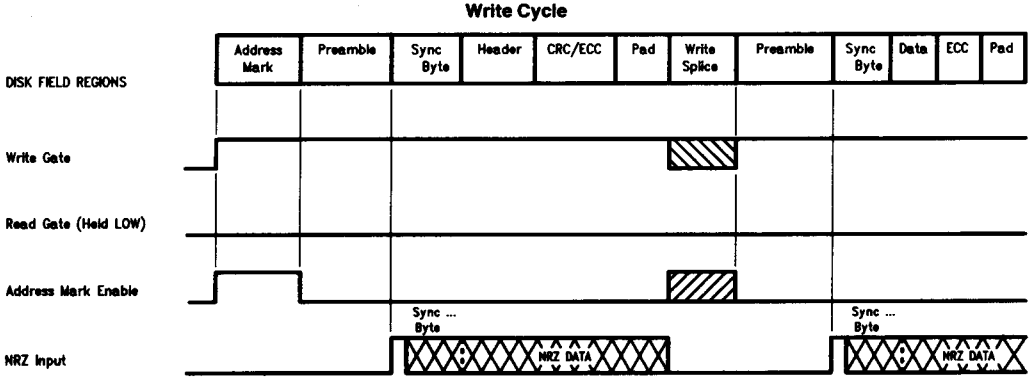
TL/F/9386–31

ZPS Delay Time measures the number of REF CLK cycles that pass from the time READ GATE is passed to the Synchronizer, until Zero Phase Start interrupts the VCO and stops RD/REF CLK. READ GATE is internally qualified in all SMD and ST506 modes to prevent the Synchronizer from attempting to lock when there is no data present (outside the Preamble Field). The basic t_{zpsi} and t_{zpsr} delay times are listed for the ESDI and IBM modes, while the SMD and ST506 modes have prequalifier adders. Delay times t_{zpsi} measures the time to interrupt the VCO, and t_{dzpsr} measure the time to Restart the VCO.

Address Mode	RG Qualified On:	t_{dzpsi} (in REF CLK) Cycles)	t_{dzpsr}
All ESDI Modes	N/A	≤3	≤ 4 after Falling RG
All SMD Modes	AMF Assertion	≤3 + AMF Detection	≤ 4 after Falling RG
All ST506 Modes	Preamble	≤3 + 12 Preamble Patterns	≤ 4 after Falling RG

ESDI (Std and Nt) MODE Control Waveforms

Write Cycle

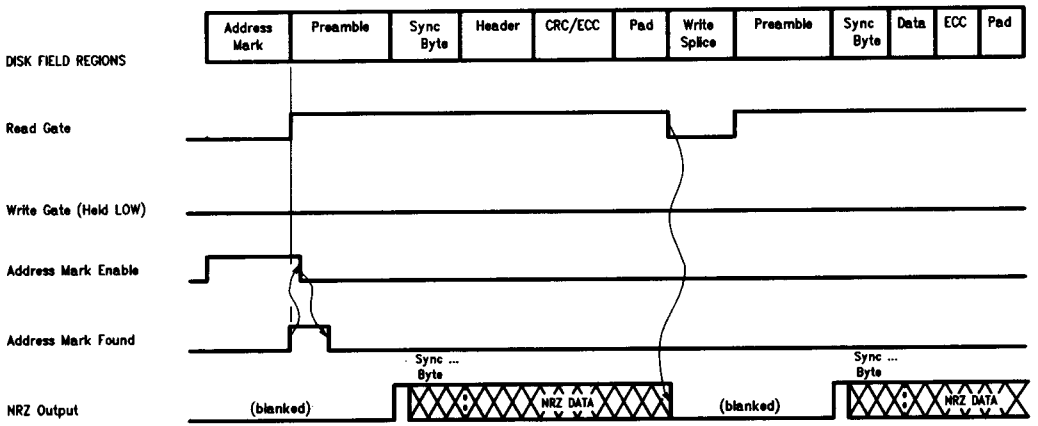


Note: Cycling either Write Gate, ▨ or AME ▨ resets the encoder, and starts the Preamble again.

TL/F/9386–4

ESDI (Std and Nt) MODE Control Waveforms (Continued)

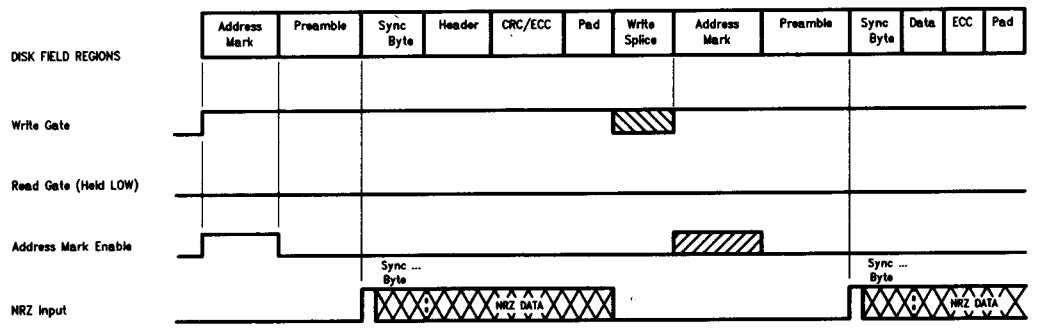
Read Cycle



TL/F/9386–5

SMD (Std and Nt) MODE Control Waveforms

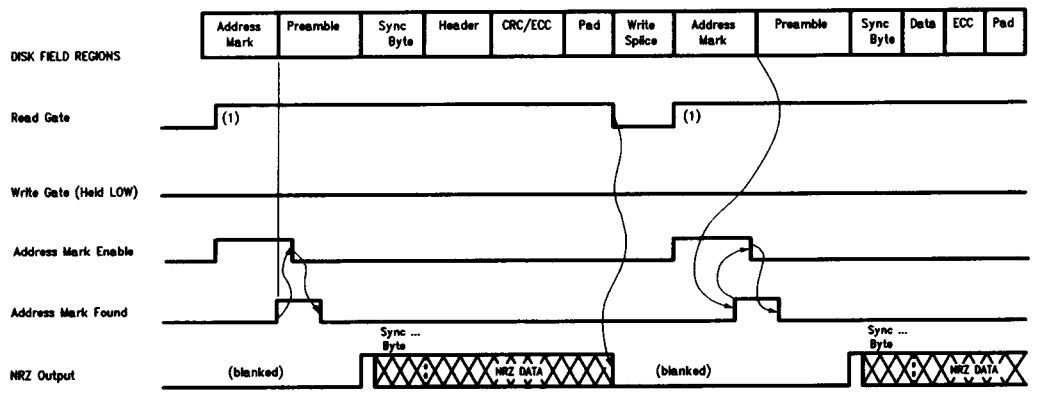
Write Cycle



Note: Cycling either Write Gate, ▨ or AME ▨ resets the encoder, and starts the Preamble again.

TL/F/9386–6

Read Cycle

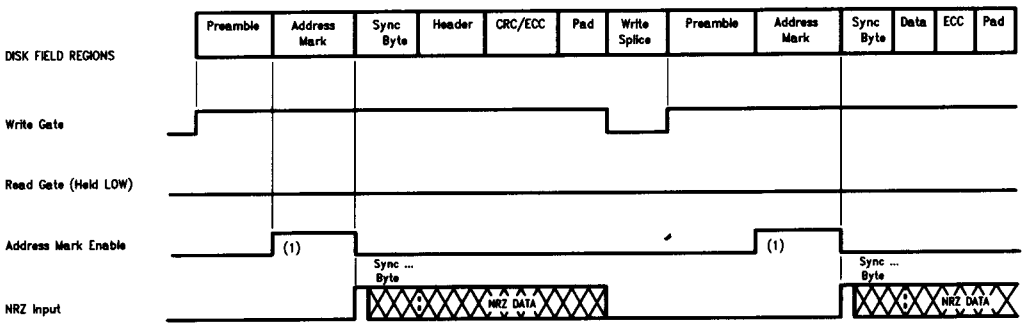


TL/F/9386–7

Note 1: Read Gate to the Synchronizer is internally qualified with AMF.

ST506A MODE Control Waveforms

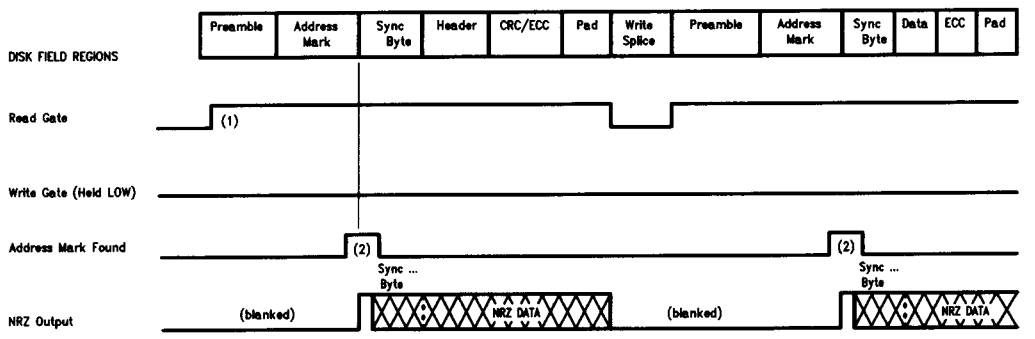
Write Cycle



TL/F/9386–8

Note 1: AME must be exactly 8 NRZ bits.

Read Cycle



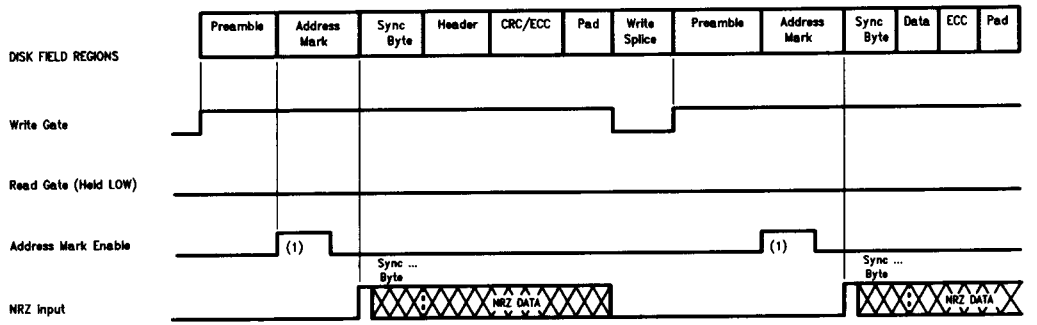
TL/F/9386–9

Note 1: The DP8469 employs a Preamble Prequalifier to ensure that the Read Gate is only passed to the synchronizer after the Preamble field has been found.

Note 2: AMF Terminated by the Second NRZ OUTPUT bit after NRZ OUTPUT unblanks.

ST506B MODE Control Waveforms

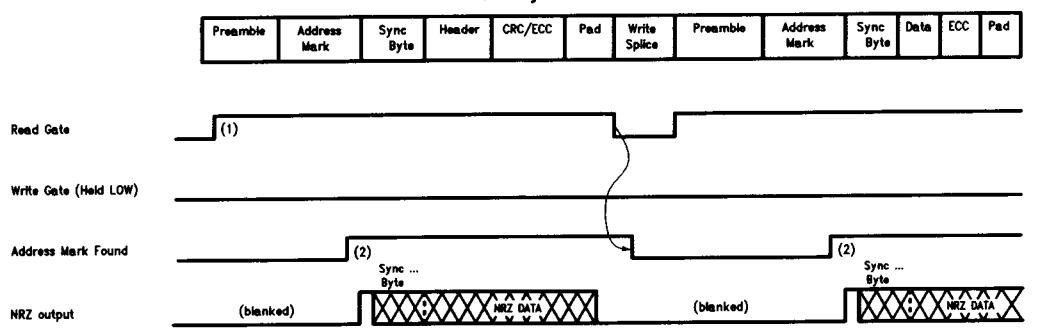
Write Cycle



TL/F/9386–10

Note 1: AME must be exactly NRZ bits.

Read Cycle



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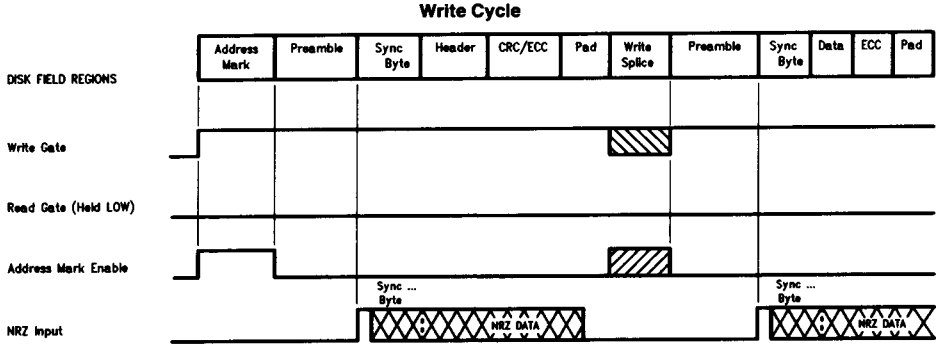
Note 1: The DP8469 employs a Preamble Prequalifier to ensure that the Read Gate is only passed to the synchronizer after the Preamble field has been found.

Note 2: AMF terminated by the deassertion of Read Gate.

IBM and DP8466 ESDI Mode Control Waveforms

Write Cycle



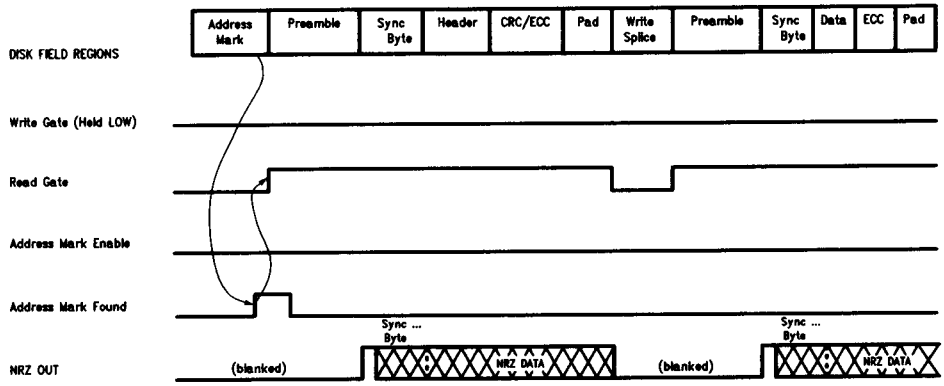
Note: Cycling either Write Gate, ▨ or AME ▨ resets the encoder, and starts the Preamble again.

IBM Address Mark is written as a 2 byte gap with 3 transitions, DP8466 ESDI uses standard 3 byte transitionless ESDI gap

TL/F/9386–32

IBM and DP8466 ESDI Mode Control Waveforms (Continued)

Read Cycle

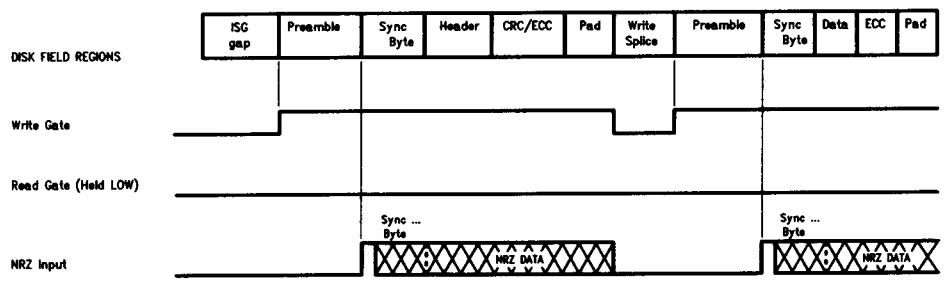


TL/F/9386–33

Note: AME is a DON'T CARE during Read Mode.

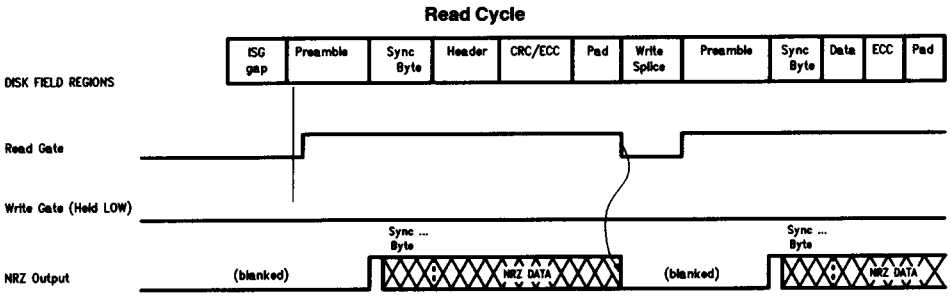
Hard Sector MODE Control Waveforms

Write Cycle



TL/F/9386–12

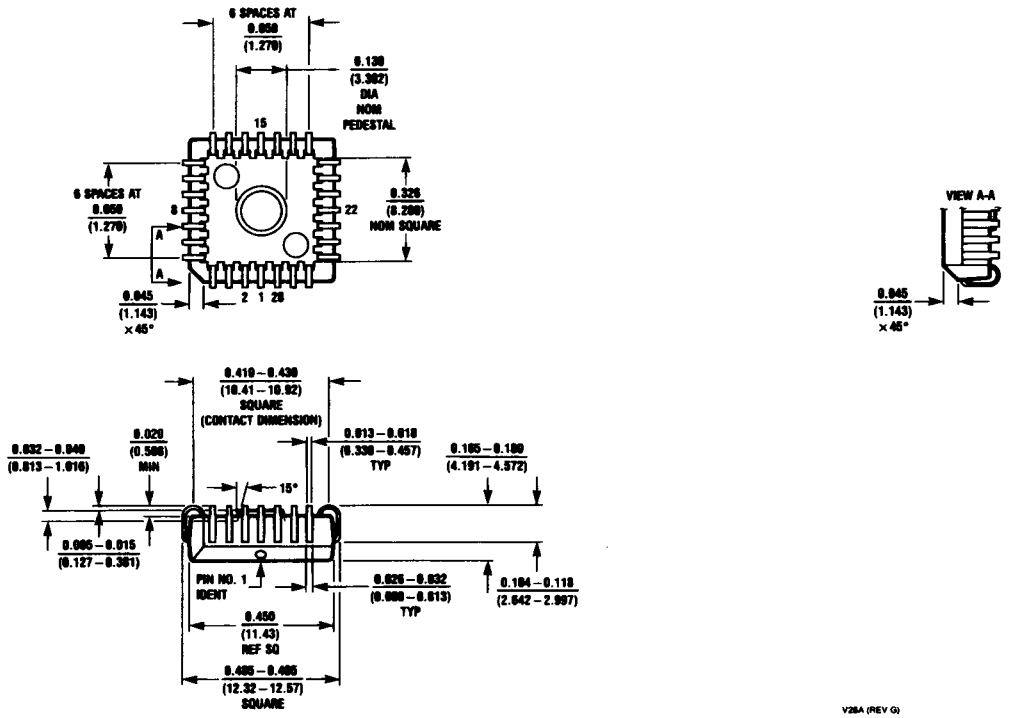
Read Cycle



TL/F/9386–13

Physical Dimensions inches (millimeters)

Lit. # 103078



Plastic Chip Carrier (V)
Order Number DP8469V
NS Package Number V28A

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