CD54HC374/3A
CD54HCT374/3A

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

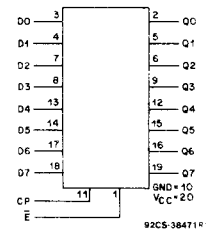
Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54HC/HCT374	2,5,6,9,12, 15,16,19	1,3,4,7,8,10,11, 13,14,17,18	20	2,5,6,9,12, 15,16,19	10	1,3,4,7,8,11,13, 14,17,18,20
Dynamic	**OPEN**	**GROUND**	**1/2 V_{CC} (3V)**	**V_{CC} (6V)**	**OSCILLATOR**	
					50 kHz	**25 kHz**
CD54HC/HCT374	--	1,10	2,5,6,9,12,15, 16,19	20	11	3,4,7,8,13,14, 17,18

NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.

CD54HC377/3A
CD54HCT377/3A

Octal D-Type Flip-Flop with Data Enable

The RCA CD54HC377 and CD54HCT377 are octal D-type flip-flops with a buffered clock (CP) common to all eight flip-flops. All the flip-flops are loaded simultaneously on the positive edge of the clock (CP) when the Data Enable ($\overline{E}$) is LOW.



FUNCTIONAL DIAGRAM

Package Specifications
See Section 11, Fig. 13

Static Electrical Characteristics (Limits with black dots (•) are tested 100%)

CHARACTERISTICS		TEST CONDITIONS HC/HCT V_{DD}	V_O	I_O	V_{CC} or GND	V_{IN} HC V_{IL} or V_{IH}	V_{IN} HCT V_{IL} or V_{IH}	LIMITS MIN.	LIMITS MAX.	UNITS
Quiescent	25°C	6	—	—	6, 0	—	—	—	8•	μA
Device Current	-55°C / +125°C	6	—	—	6, 0	—	—	—	160•	μA
I_{CC}										

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

HCT INPUT LOADING TABLE

INPUT	UNIT LOAD*
$\overline{E}$	1.5
CP	0.5
All Dn Inputs	0.25

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54HC377/3A
CD54HCT377/3A

Switching Speed (Limits with black dots (•) are tested 100%.)

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-55°C to +125°C				UNITS
			HC		HCT		54HC		54HCT		
		V	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, CP to Q	t_{PLH} t_{PHL}	2	—	175	—	—	—	265	—	—	ns
		4.5	—	35•	—	38•	—	53•	—	57•	
		6	—	30	—	—	—	45	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	75	—	—	—	110	—	—	
		4.5	—	15	—	15	—	22	—	22	
		6	—	13	—	—	—	19	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	pF

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54HC/HCT377	2,5,6,9,12, 15,16,19	1,3,4,7,8,10,11, 13,14,17,18	20	2,5,6,9,12, 15,16,19	10	1,3,4,7,8,11,13, 14,17,18,20
Dynamic	**OPEN**	**GROUND**	**1/2 V_{CC} (3V)**	**V_{CC} (6V)**	**OSCILLATOR**	
					50 kHz	25 kHz
CD54HC/HCT377	—	1,10	2,5,6,9,12,15, 16,19	20	11	3,4,7,8,13,14, 17,18

NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.

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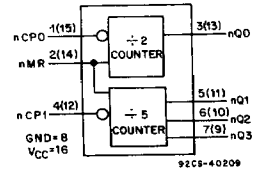
Dual Decade Ripple Counter

CD54HC390/3A
CD54HCT390/3A

The RCA CD54HC390 and CD54HCT390 dual 4-bit decade ripple counters are high-speed silicon-gate CMOS devices and are pin compatible with low-power Schottky TTL (LSTTL). These devices are divided into four separately clocked sections. The counters have two divide-by-2 sections and two divide-by-5 sections. These sections are normally used in a BCD decade or bi-quinary configuration, since they share a common master reset (nMR). If the two master reset inputs (1MR and 2MR) are used to simultaneously clear all 8 bits of the counter, a number of counting configurations are possible within one package. The separate clock inputs ($n\overline{CP0}$ and $n\overline{CP1}$) of each section allow ripple counter or frequency division applications of divide-by-2, 4, 5, 10, 20, 25, 50 or 100. Each section is triggered by the HIGH-to-LOW transition of the input pulses ($n\overline{CP0}$ and $n\overline{CP1}$).

For BCD decade operation, the nQ0 output is connected to the $n\overline{CP1}$ input of the divide-by-5 section. For bi-quinary decade operation, the nQ3 output is connected to the $n\overline{CP0}$ input and nQ0 becomes the decade output.

The master reset inputs (1MR and 2MR) are active-HIGH asynchronous inputs to each decade counter which operates on the portion of the counter identified by the "1" and "2" prefixes in the pin configuration. A HIGH level on the nMR input overrides the clock and sets the four outputs LOW.



FUNCTIONAL DIAGRAM

Package Specifications

See Section 11, Fig. 11